NanoAmp Solutions, Inc.
1982 Zanker Road, San Jose, CA 95112
ph: 408-573-8878, FAX: 408-573-8877
www.nanoamp.com

EM02R2XX Family - Combination SRAM with ROM

Low Power 32Kx8 SRAM with on board 256Kx8 Mask ROM

Overview

The EM02R2XX is an integrated memory device containing both a low power 256 Kbit Static Random Access Memory (organized as 32,768 words by 8 bits), and a 2 Mbit Mask ROM (organized as 262,144 words by 8 bits). It is fabricated using an advanced CMOS process and NanoAmp's high-speed/low-Power circuit technology. This device is designed for low voltage operation and is very suitable for battery powered devices. Low power applications are also well served by this device due to its very low operating and standby current. Also, this device allows the user to make independent requests to the ROM or RAM without incurring unwanted I_{CC} overhead.

Features

- **Extended Operating Voltage Range**
  1.5 to 3.6 V
- **Very Low Standby Voltage**
  1.2 V
- **Extended Temperature Range**
  -20^{o} to $+80^{o}$C
- **Fast Cycle Time**
  100 ns (@ 2.7V)
- **Very Low Operating Current**
  I_{CC} < 1 mA typical at 3V, 1 Mhz
- **Very Low Standby Current**
  I_{SB} = 100 nA typical
- **Available in 32-pin STSOP or TSOP package**

FIGURE 1: Pin Configuration

TABLE 1: Pin Descriptions

Pin Name	Pin Function
A0-A14	Address Inputs
D0-D7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable (Active Low)
$\overline{OE}$	Output Enable (Active Low)
WE	Write Enable (Active Low)
V_{CC}	Power
V_{SS}	Ground
NC	Not Connected (Floating)

FIGURE 2: Operating Envelope

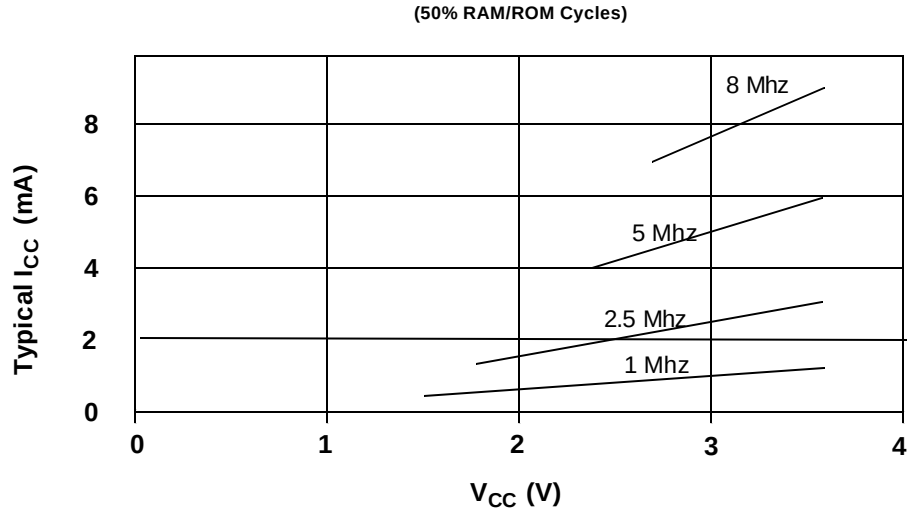

FIGURE 3: Functional Block Diagram

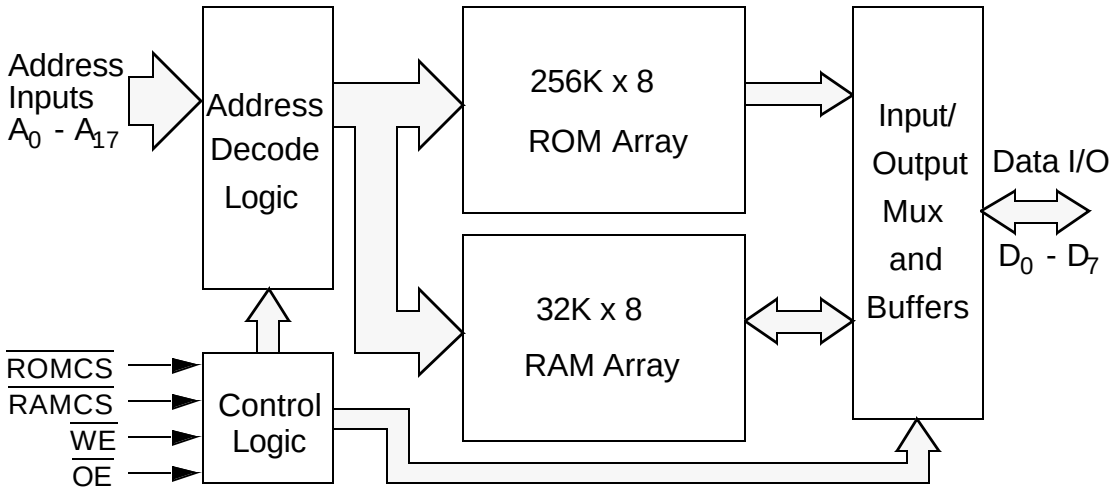

TABLE 2: Functional Description

$\overline{ROMCS}$	$\overline{RAMCS}$	$\overline{WE}$	$\overline{OE}$	D0-D7	MODE	POWER
H	H	X	X	High Z	Standby	Standby
L	H	X	H	High Z	Standby	Standby*
L	H	L	L	High Z	ROM READ**	Active -> Standby
L	H	H	L	Data Out	ROM READ	Active -> Standby
H	L	H	H	High Z	Standby	Standby*
H	L	H	L	Data Out	RAM READ	Active -> Standby
H	L	L	X	Data In	RAM WRITE	Active -> Standby

*The device will consume active power in this mode whenever addresses are changed
** No output is available

TABLE 3: Absolute Maximum Ratings*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 4.6	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–40 to +125	^oC
Operating Temperature - Extended Commercial	T_A	-20 to +80	^oC

*Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 4: Operating Characteristics (Over specified temperature range)

Item	Symbol	Test Conditions	Min.	Typical	Max.	Unit
Supply Voltage	V_{CC}		1.5		3.6	V
Data Retention Supply Voltage	V_{DR}	$\overline{RAMCS} = V_{CC}$ $\overline{ROMCS} = V_{CC}$	1.2		3.6	V
Input High Voltage	V_{IH}		$0.7V_{CC}$		$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}		–0.3		$0.3V_{CC}$	V
Output High Voltage	V_{OH}	I_{OH} = -100 µA	V_{CC}–0.2			V
Output Low Voltage	V_{OL}	I_{OL} = 100 µA			0.2	V
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}			1	µA
Output Leakage Current	I_{LO}	$\overline{OE} = V_{IH}$ or $\overline{RAMCS}$ = 1, $\overline{ROMCS}$ = 1			1	µA
ROM Operating Supply Current (Note 1)	I_{CC1}	$V_{IN} = V_{CC}$ or 0V $\overline{RAMCS}$ = 1, $\overline{ROMCS}$ = 0		0.4 * f * V	0.5 * f * V	mA
RAM Operating Supply Current (Note 1)	I_{CC2}	$V_{IN} = V_{CC}$ or 0V $\overline{RAMCS}$ = 0, $\overline{ROMCS}$ = 1		0.25 * f * V	0.3 * f * V	mA
Standby Current (Note 2)	I_{SB}	$V_{IN} = V_{CC}$ or 0V		0.1	10	µA

Notes:

Note 1. Operating current is a linear function of frequency and voltage. You may calculate operating current using the formula shown with operating frequency (f) expressed in Mhz and operating voltage (V) in volts. Example: Operating at 2 Mhz in the RAM selected mode at 2.0 volts will draw a typical current of 0.25*2*2 = 1.0 mA.

Note 2. This device assumes a standby mode if both $\overline{ROMCS}$ and $\overline{RAMCS}$ are disabled (high). It will also automatically go into a standby mode whenever all input signals are quiescent (not toggling) for more than one cycle time regardless of the states of $\overline{ROMCS}$ and $\overline{RAMCS}$. In order to achieve low standby current all input levels must be within 0.2 volts of either V_{CC} or GND.

TABLE 5: Capacitance*

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 Mhz, T_A = 25°C		5	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 Mhz, T_A = 25°C		5	pF

Note: These parameters are verified in device characterization and are not 100% tested

TABLE 6: Timing Test Conditions

Item	
Input Pulse Level	$0.1V_{CC}$ to $0.9 V_{CC}$
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	$0.5V_{CC}$
Output Load	CL = 30pF
Operating Temperature (Unless otherwise stated)	-20 to +80 °C

TABLE 7: RAM Read Cycle Timing

Item	Symbol	Min/Max	1.5V	1.8V	2.4V	2.7-3.6V	Units
Read Cycle Time	t_{RC}	Min	750	250	150	100	ns
Address-$\overline{\text{RAMCS}}$ Setup Time	t_{ASC}	Min	-80	-40	-25	-15	ns
Address-$\overline{\text{RAMCS}}$ Hold Time	t_{AHC}	Min	600	200	120	75	ns
Address Access Time	t_{AA}	Max	750	250	150	100	ns
RAM Select Access Time	t_{CS}	Max	750	250	150	100	ns
Output Enable to Valid Output	t_{OE}	Max	250	70	50	30	ns
RAM Select to Low-Z output	t_{LZ}	Min	0	0	0	0	ns
Output Enable to Low-Z Output	t_{OLZ}	Min	0	0	0	0	ns
RAM Select to High-Z Output	t_{HZ}	Min	0	0	0	0	ns
		Max	100	50	40	25	
Output Disable to High-Z Output	t_{OHZ}	Min	0	0	0	0	ns
		Max	100	50	40	25	
Output Hold from Address Change	t_{OH}	Min	40	20	15	10	ns

TABLE 8: RAM Write Cycle Timing

Item	Symbol	Min/Max	1.5V	1.8V	2.4V	2.7-3.6V	Unit
Write Cycle Time	t_{WC}	Min	750	250	150	100	ns
Address-$\overline{\text{RAMCS}}$ Setup Time	t_{ASC}	Min	-80	-40	-30	-20	ns
Address-$\overline{\text{RAMCS}}$ Hold Time	t_{AHC}	Min	600	200	120	75	ns
RAM Select to End of Write	t_{CW}	Min	750	250	150	100	ns
Address Valid to End of Write	t_{AW}	Min	750	250	150	100	ns
Address Set-Up Time	t_{AS}	Min	0	0	0	0	ns
Write Pulse Width	t_{WP}	Min	400	150	75	65	ns
Write Recovery Time	t_{WR}	Min	0	0	0	0	ns
Write to High-Z Output	t_{WHZ}	Min	0	0	0	0	ns
		Max	150	70	50	30	
Data to Write Time Overlap	t_{DW}	Min	400	150	75	50	ns
Data Hold from Write Time	t_{DH}	Min	0	0	0	0	ns
End Write to Low-Z Output	t_{OW}	Min	40	20	15	10	ns

TABLE 9: ROM Read Timing

Item	Symbol	Min/Max	1.5V	1.8V	2.4	2.7-3.6V	Unit
Read Cycle Time	t_{RC}	Min	1000	400	200	150	ns
Address-$\overline{\text{ROMCS}}$ Setup Time	t_{ASC}	Min	-80	-40	-25	-15	ns
Address-$\overline{\text{ROMCS}}$ Hold Time	t_{AHC}	Min	750	300	170	120	ns
Address Access Time	t_{ACC}	Max	1000	400	200	150	ns
ROM Select Access Time	t_{CS}	Max	1000	400	200	150	ns
Output Enable Access Time	t_{OE}	Max	250	100	50	30	ns
Output Hold Time	t_{OH}	Min	0	0	0	0	ns
Output Floating Time	t_{DF}	Max	100	50	40	25	ns

FIGURE 4: ROM Read Timing ($\overline{ROMCS}$ = 0)

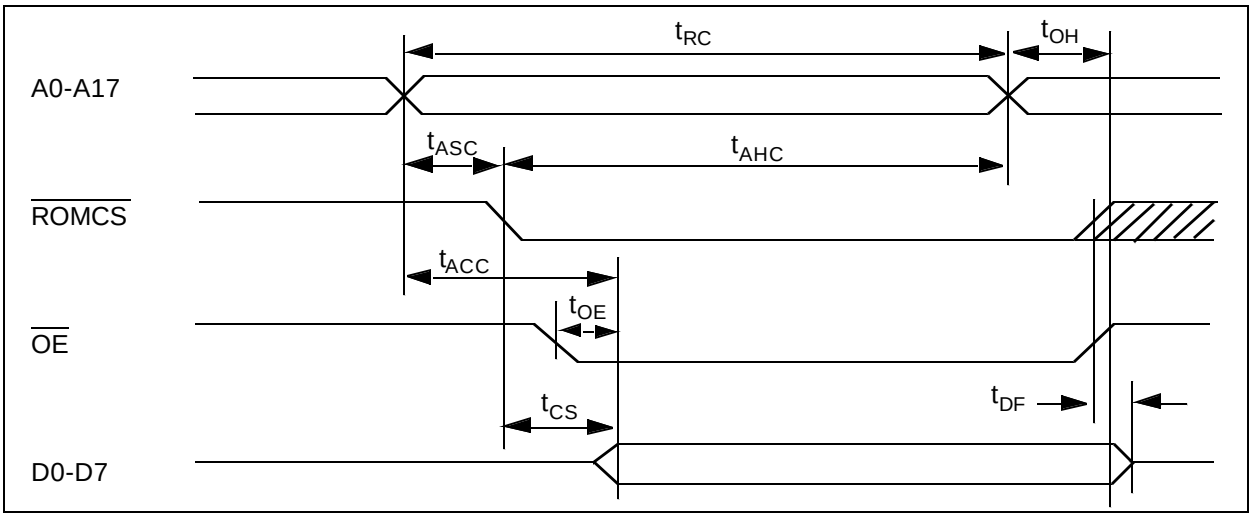

FIGURE 5: RAM Read Cycle Timing ($\overline{WE}$ = V_{IH})

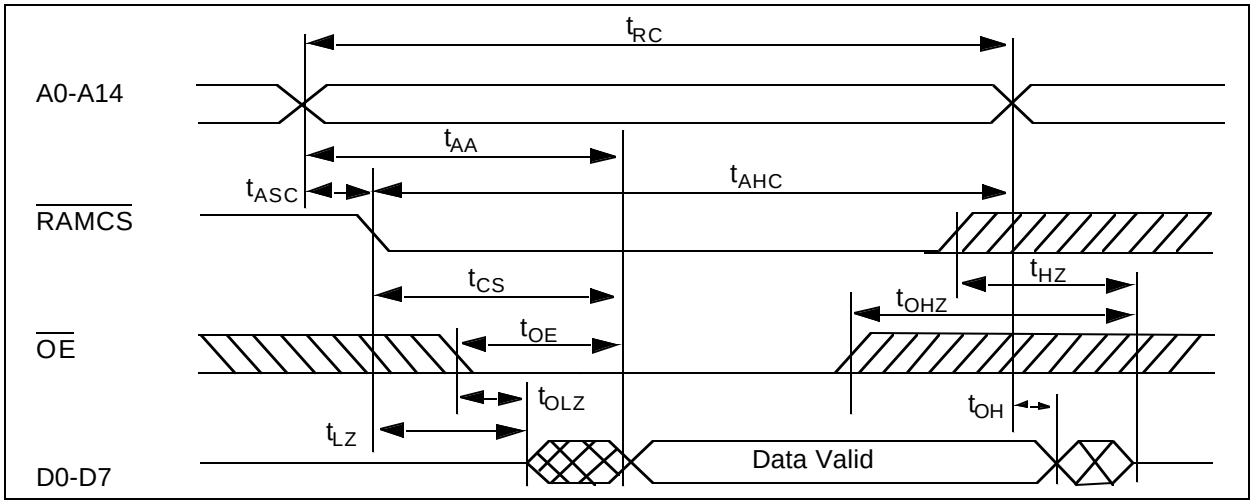

FIGURE 6: RAM Write Cycle Timing ($\overline{OE}$ fixed)

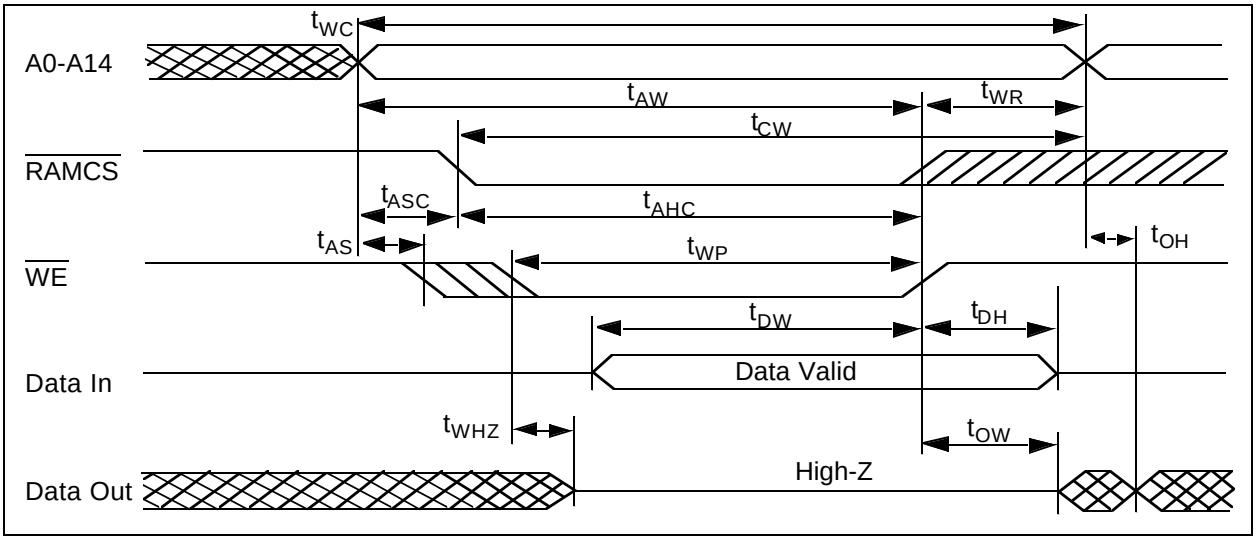

FIGURE 7: RAM Write Cycle Timing ($\overline{OE}$ clock)

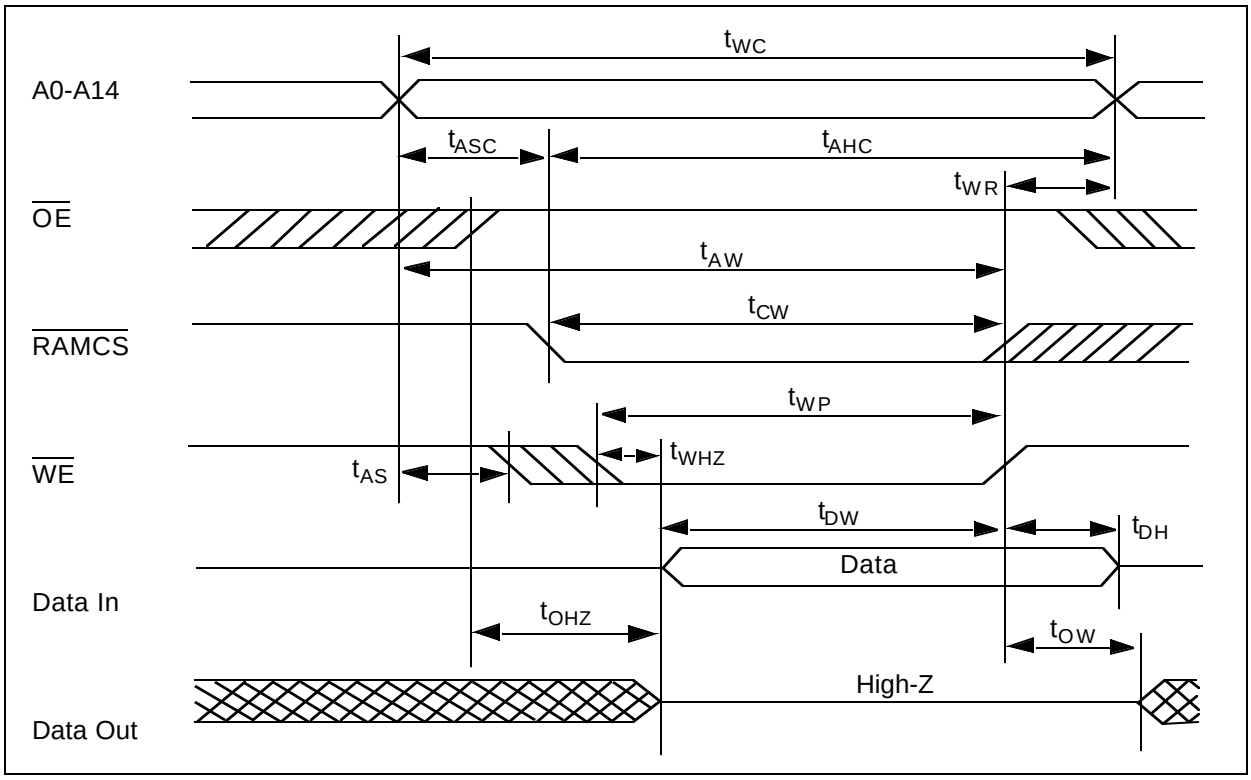

TABLE 10: RAM/ROM Assertion Timing

Item	Symbol	Min	Typ	Max	Unit
Disable $\overline{ROMCS}$ to Enable $\overline{RAMCS}$	t_{ROMRAM}	0			ns
Disable $\overline{RAMCS}$ to Enable $\overline{ROMCS}$	t_{RAMROM}	0			ns

FIGURE 8: RAM/ROM Assertion Timing

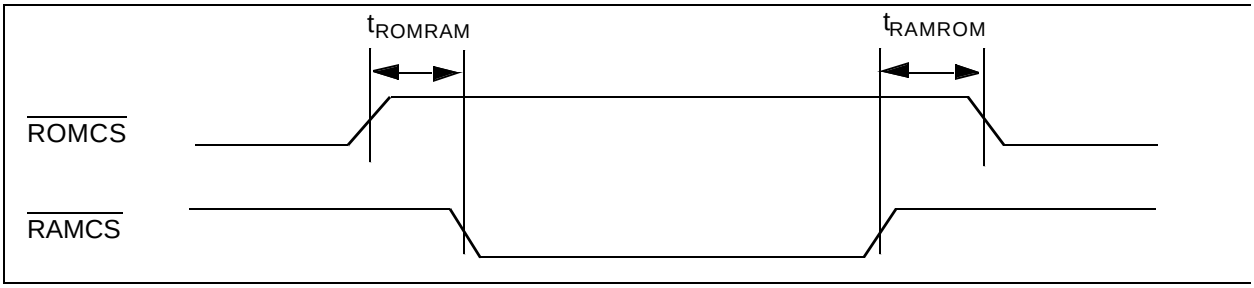

TABLE 11: Data Retention Characteristics (Over full specified temperature range)

Parameter	Symbol	Minimum	Maximum	Unit
Data Retention Set-up Time	t_{SDR}	0		µs
Recovery Time	t_{RDR}	1		µs

FIGURE 9: Data Retention Waveform ($\overline{CS}$ Controlled)

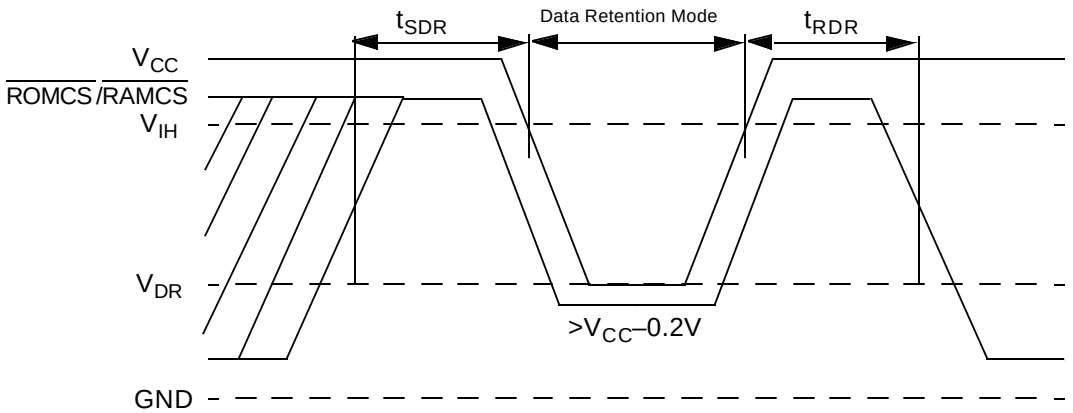

TABLE 12: Ordering Information

Part Number*	Package	Temperature Range	Voltage Range	Speed (@ 2.7V+)
EM02R2XXN	32 pin STSOP	-20 to +80°C	1.5 to 3.6 V	100RAM/150ROM ns
EM02R2XXT	32 pin TSOP	-20 to +80°C	1.5 to 3.6 V	100RAM/150ROM ns

* This part number must appear on your order. The code number is to be inserted in place of the XX.

TABLE 13: Revision History

Revision #	Date	Change Description
01	Nov. 1, 1997	Initial Formal Release
02	Feb 1, 1998	• Miscellaneous Errata Correction • Changed “V” version from 150 to 200
03	Mar 25, 1998	• Changed “L” version to 2.4 volts • Adjusted maximum current per chrz.
04	May 11, 1998	Added Address Setup and Hold Requirements with respect to RAM Chip Select
05	Aug. 1, 1998	Eliminated L,V,U Specification in favor of a single Specification that includes 1.5 to 3.6 volts operation. Extended Temp to 80C Increased twp to 65ns at 2.7 volts.
06	July 8, 1999	Modified Table 2 ($\overline{WE}$ must be high to output ROM data)