Solo Data Sheet

ENT3041 — Wire-Speed Packet Forwarding ASIC for Enterprise Networks

Revision 1.1

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Revision History

Revision	Date	Description of Changes
1.1	10/30/00	Update for Revision EB design: - Subnet broadcasts for Ethernet and OC-3 ports - TTL0/1 handling for Ethernet and OC-3 ports - 6-bit DSCP updating for Ethernet and OC-3 ports - Tx Only IP Address for Ethernet port - Flow Table Layer 1 transaction revision - Layer 2 Tx/Rx Tag mode for Ethernet port - Tx/Rx VLAN mode for Ethernet port - Tx/Rx SNAP mode for Ethernet port - Layer 2 multicast function for Ethernet ports - ARP reply “forward to cpu” function for Ethernet ports

Preface

This document describes the features and functional descriptions for the Entridia ENT3041 Solo™ wire-speed packet forwarding ASIC.

Solo is ideally suited for IP based aggregation systems in Service Provider networks, and is part of Entridia's OPERA™ (Optical Edge Routing Architecture) family of products targeted at high performance MAN/LAN routers. Solo features four 10/100 Ethernet ports and an OC-3c Packet-Over-Sonet (PoS) port by way of Entridia's OCPort™ interface. Solo also offers connectivity to legacy WAN networks by way of Entridia's EdgeStream™ interface and glue-less expansion capability by the OptiStream™ expansion bus.

References

- IEEE Std. 802.3 1998 Edition
- *RMII Specification Revision 1.2*, RMII Consortium, March 20, 1998
- *POS-PHY Saturn Compatible Packet Over SONET Interface Specification (Level2)*, PMC-Sierra Inc. / Saturn Development Group, PMC-971147 Issue 5, December 1998
- IETF Network Management RFCs
  - RFC 1812 "Requirements for IP version 4 Routers"
  - RFC 1213 "Management Information Base for Network Management of TCP/IP based internets: MIB-II"
  - RFC 2474 "Definition of the Differentiated Services Field (DS Field) in the IPv4 and IPv6 Headers"
  - RFC 2475 "An Architecture for Differentiated Services"
- IEEE Std. 802.1Q, December 1998. -- VLAN
- RFC1042 "A Standard for the Transmission of IP Datagrams over IEEE 802 Networks", IEEE 802 Network Working Group, February 1988.
- IEEE Std. 802.2 -- SNAP

Table of Contents

Chapter 1 Functional Description

Entridia's Solo chip is a fully integrated, wire-speed classical IP router chip targeted at high performance routing systems. The architecture of the Solo chip supports Data Link (OSI Layer 2) and Physical (OSI Layer 1) interface technologies, such as 10/100 Mbps Ethernet, Packet-Over-Sonet and ATM at OC-3c rates, DSL, T1/T3, and broadband cable. With aggregate throughput of 1.2 Gbps and guaranteed ingress-to-egress latency of eight microseconds, the Solo chip is ideally suited for ISP and Carrier Access edge routing systems and emerging IP Telephony (Voice-over-IP) systems.

The primary function of the Solo chip is to route IP packets using information contained in the header of each packet and knowledge (routes) of which groups of IP addresses (subnets) are reachable through its network interfaces.

This chapter describes the features and functions supported by the Solo chip.

1.1 Data Link Layer (OSI Layer 2) Frame Processing

The Solo device's data link layer frame processing includes all the traditional Media Access Controller (MAC) functionality for 10/100 Mbps Ethernet media and an OC-3c PoS physical layer.

The following paragraphs describe the functionality of the Ethernet Media Access Interfaces.

Layer 2 Multicast: The transmit side derives the appropriate multicast MAC address for a Class D IP-Multicast address.

IETF RFC826 Ethernet Address Resolution Protocol (ARP): To associate MAC addresses with Network Layer IP addresses, the Solo chip maintains a memory table on each Ethernet Interface that maps MAC addresses to IP addresses.

IP to MAC address translation table: This table supports both static and dynamic entries and is maintained entirely by the Layer 2 Media Access Interface of the Solo chip. The device manages entries in this table by examining the ARP (IETF RFC826) packets that arrive at each of the media access interfaces. Optionally, configuration software running on a companion microprocessor can augment or override this behavior and add static entries to this table.

OC-3c Port: Solo has an OC-3c line-rate port that provides connection to the network. Through the port interface Solo transmits and receives PPP encapsulated IP packets with optional 32-bit tags attached. An external Layer 2 device is required to add the appropriate framing/deframing to PPP packets transmitted from Solo. The maximum packet size for the OC-3c port is 1,536 bytes.

Promiscuous mode: This register-programmable mode is used to examine all incoming frames irrespective of the destination MAC address. This mode is used primarily for testing purposes.

Bridge mode: This register-programmable mode is used to pass the frame data to a companion microprocessor. This mode is used primarily for testing purposes.

Management Information Base (MIB) registers and counters: These registers and counters are maintained on the chip and trigger interrupts on overflows that can be monitored and collected by Management software running on a companion microprocessor.

Glueless Reduced MII (RMII) interface to the physical layer: The RMII can support 10Mb/s and 100Mb/s data rates, provides independent 2 bit wide (di-bit) transmit and receive data paths, and uses TTL-compatible (3.3V CMOS) signal levels.

Support for Subnet Broadcast: The Ethernet ports and OC-3c port treat all incoming packets, that are determined to be addressed to an IP Subnet Broadcast address, as multicast packets. An IP Subnet Broadcast packet is defined as a packet with a IP destination address which matches the network portion of one of 8 IP addresses associated with the network port and the host portion of the Subnet Mask is all 1s.

Support for Tagged/VLAN/SNAP mode packets: The Ethernet ports support alternative Ethernet specific packet formats.

1.2 Network Layer (OSI Layer 3) Packet Processing

Once a Layer 2 frame has been successfully received without CRC or other errors by a Network Interface, the Network Layer processing logic takes over. For IP packets, the Layer 3 processing logic includes the following functions:

- Verify the header checksum of an incoming packet.
- Verify the validity of the IP Time to Live (TTL) field, decrement the TTL field appropriately, and recalculate the IP checksum field.
- Look up the destination interface in the route table (refer to Route Table - Section 1.4) using the destination address and IP type of service field and queue the packet for transmission.
- Prioritize the transmission of packets based on the contents of the IP Type of Service (TOS) field.

- If enabled, search the flow table (refer to Flow Table Section 1.5) for rules that apply to the source and destination IP address, source and destination port (TCP, UDP or other Layer 4 port) of each packet. Then, perform the specified action (forward, drop, or invoke processing hooks in software running on the companion microprocessor).
- Notify the companion microprocessor of IP Multicast, ICMP, and non-IP protocol packets. Permit software running on the microprocessor to determine handling for such packets and queue them for transmission from the appropriate output interface.

1.3 EdgeStream Interface

The EdgeStream Interface is the microprocessor interface of the Solo device. It consists of a 32-bit data bus and a 7-bit address bus.

This interface presents Solo as a memory-like device to the microprocessor. An extensive register map enables software running on the microprocessor to initialize and dynamically re-configure the Solo chip.

This interface also includes an interrupt line, which is used to notify the microprocessor of exception conditions and periodic events. Notification of specific conditions can be masked or enabled by programming appropriate interrupt control registers.

1.4 Route Table

The Solo chip has a built-in 512 entry route table with full support for longest prefix match look up, essential for Classless Interdomain Routing (CIDR) as route lookup can be performed in three cycles using this approach. Solo can guarantee wire-speed processing with deterministic latency. The Solo chip route table also supports using the IP TOS field in making Quality of Service (QOS) policy based destination route selection.

Configuration software running on a companion microprocessor can install static routes (including a default gateway entry) and periodically age and rebuild other entries dynamically as a result of routing protocol messages (such as OSPF and BGP4). Also, the companion microprocessor can maintain very large route tables in system memory and use the on-chip 512 entry table as a cache for frequently used routes.

Lookup Terms		Lookup Result	
DestIP/Tag 32-bit VLSM 32-bit	TOS 8-bit	NextHopIP 32-bit	NextHop Interface Number 8-bit

Table 1.1 Route Table Entry

1.5 Flow Table

The Solo chip has a 256 entry flow table. The flow table maintains filtering rules to determine which types of IP packets a network interface can forward or discard, and which types require further examination by software running on a companion microprocessor.

Each flow table entry can specify a source and destination IP subnet, source and destination port (TCP, UDP or other Layer 4 port) along with an action to take if any or all of these fields match those of the packet being filtered. The action can specify one of the following:

- Forward: Accept the packet, and forward it normally.
- Priority Forward: Accept the packet, and forward it with priority over normal packets.
- Drop: Discard the packet and account for it in the management counters.
- Examine: Accept the packet and notify a companion microprocessor of the match and the starting address of the packet data in the Packet Buffer memory. This enables additional filtering software running on the microprocessor to further process the packet.

Lookup Terms			Lookup Results	
Layer 3 Parameters	Layer 4 Parameters	Chip Interface Number 4-bit	Action 2-bit	Priority 6-bit
See Table 1.3	See Table 1.4			

Table 1.2 Flow Table Entry

DestIP 32-bit	SrcIP 32-bit	Protocol 8-bit	TOS 8-bit
VLSM 32-bit	VLSM 32-bit		

Table 1.3 Layer 3 Parameters

DestPort Number (TCP/UDP)		SrcPort Number (TCP/UDP)	
Lower Limit 16-bit	Upper Limit 16-bit	Lower Limit 16-bit	Upper Limit 16-bit

Table 1.4 Layer 4 Parameters

1.6 Queue Management

The Solo chip architecture implements a hybrid input and output queuing model, which enables extensible end-to-end quality of service in a router system.

The OC-3c port has 8 levels of priority and the Ethernet ports have 2 levels of priority. The priority output queues can be selected based on the type of service, source or destination IP addresses, and TCP, UDP or other Layer 4 ports, or a valid combination of the aforementioned parameters, making it highly flexible for system designers to implement policy-based wire-speed routing rules for the OC-3c port. Solo has a built in weighted round-robin scheduler with user programmable weights.

1.7 Software Interface

Entridia provides complete software drivers and a Service Application Programming Interface (API) to enable system designers to quickly migrate their existing software to the Solo platform.

The software drivers are targeted to the Wind River Systems' VxWorks real-time operating system. However, the drivers use a hardware abstraction model that makes it very easy to port to other real-time operating systems.

To enable quick integration with existing software in routers, the Entridia driver presents the Solo network interface as five independent network devices. The router software that deals with Network Layer communications can treat each of the interfaces as a dedicated Data Link Layer device and interoperate with them without modification.

In addition to the drivers, the Service API is a library of C functions that simplify access to the more advanced features of the Solo chip such as filtering rules and traffic shaping parameters.

1.8 System Integration

The Solo chip is designed to integrate into ISP and Carrier Access edge routing systems without significant modification to the software currently running on those systems, while accelerating their performance and increasing functionality.

The Solo device can handle the following functions, which are currently handled by a microprocessor or discrete programmable logic, without any software intervention:

- Packet forwarding: The Solo chip transfers all packet data into and out of the Packet Buffer memory.

- ARP table management: The Solo chip learns the IP to MAC address mapping, and ages and refreshes the entries at periodic intervals specified in programmable registers.
- ARP protocol handling: A register-programmable Proxy ARP mode enables the Solo chip to respond automatically to ARP requests with appropriate ARP response packets to implement transparent subnet gateways.
- Route look up: The Solo chip searches for the longest prefix match for a destination IP address in the route table.
- Packet filtering rules: The Solo chip forwards or discards packets based on rules in the flow table.
- Packet Buffer management: The Solo chip allocates and reclaims space for the packets in the Packet Buffer memory.
- IP Multicast: The Solo chip manages transmission of multicast packets to all the recipient ports without unnecessary data copying.
- IP based QoS: Priority Scheduling; weighted round-robin.

Chapter 2 Hardware Description

This chapter provides a hardware description of the Solo device. This chapter also describes the Solo chip external signals. It provides detailed pin-out diagrams and describes each of the signals.

The Solo chip integrates four Ethernet ports and one PoS OC-3c port. The device is packaged in a 388-pin SBGA.

The device has three major external interfaces:

- EdgeStream interface
- SRAM interface
- Network interface Ethernet/OC3-c

EdgeStream Interface. This generic memory interface is designed so that system OEMs can manage the Solo chip as a memory mapped device. This interface supports the use of an external CPU. In this way, system integrators can preserve their existing investment in Network Operating System software. In addition, system integrators can further differentiate their products by providing additional policy-based routing, bridging, VLAN, QOS, and/or VPN functionality layered with Solo devices.

SRAM Interface. The synchronous SRAM memory interface operates at 100MHz, and is used to interface with industry standard SRAMs available from various suppliers. The external SRAM is used as a Packet Buffer for storing network packet data in queued data structures. Packets arriving via the Network Interface or the EdgeStream Interface are always buffered in the Packet Buffer to permit additional processing before transmission.

Network Interface. This interface uses a set of four Ethernet ports with an RMII media interface to connect to the PHY and/or PMD device required by the service provided at the physical port, and one OC-3c port using a Packet-Over-Sonet POS-PHY Level 2 interface.

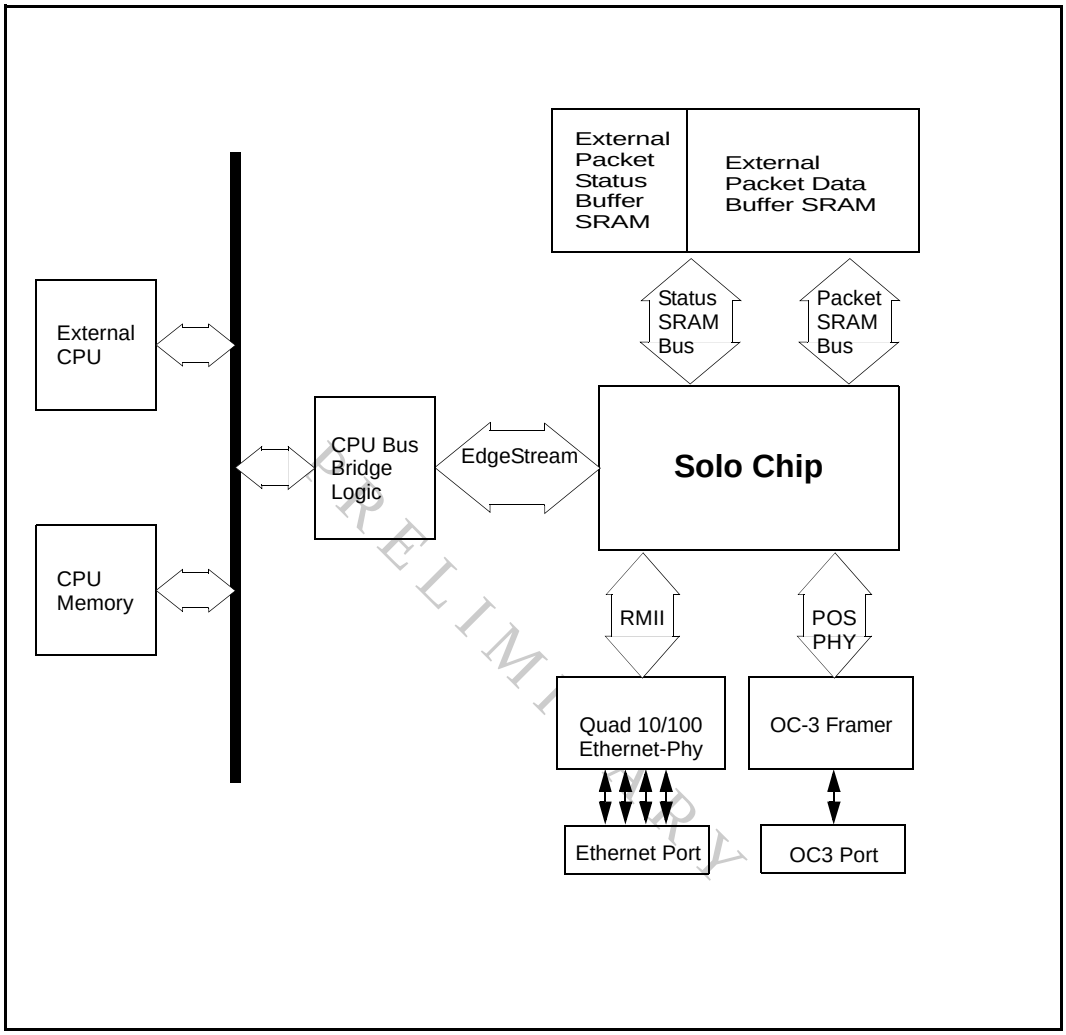

Figure 2.1 Solo System Block Diagram

2.1 Pin-Out

Figure 2.2 is a ball placement diagram of the Solo chip. The labels on the x and y axes provide reference between this diagram and the signal descriptions. The maximum height (above board) of the package including solder balls is 2.33 mm.

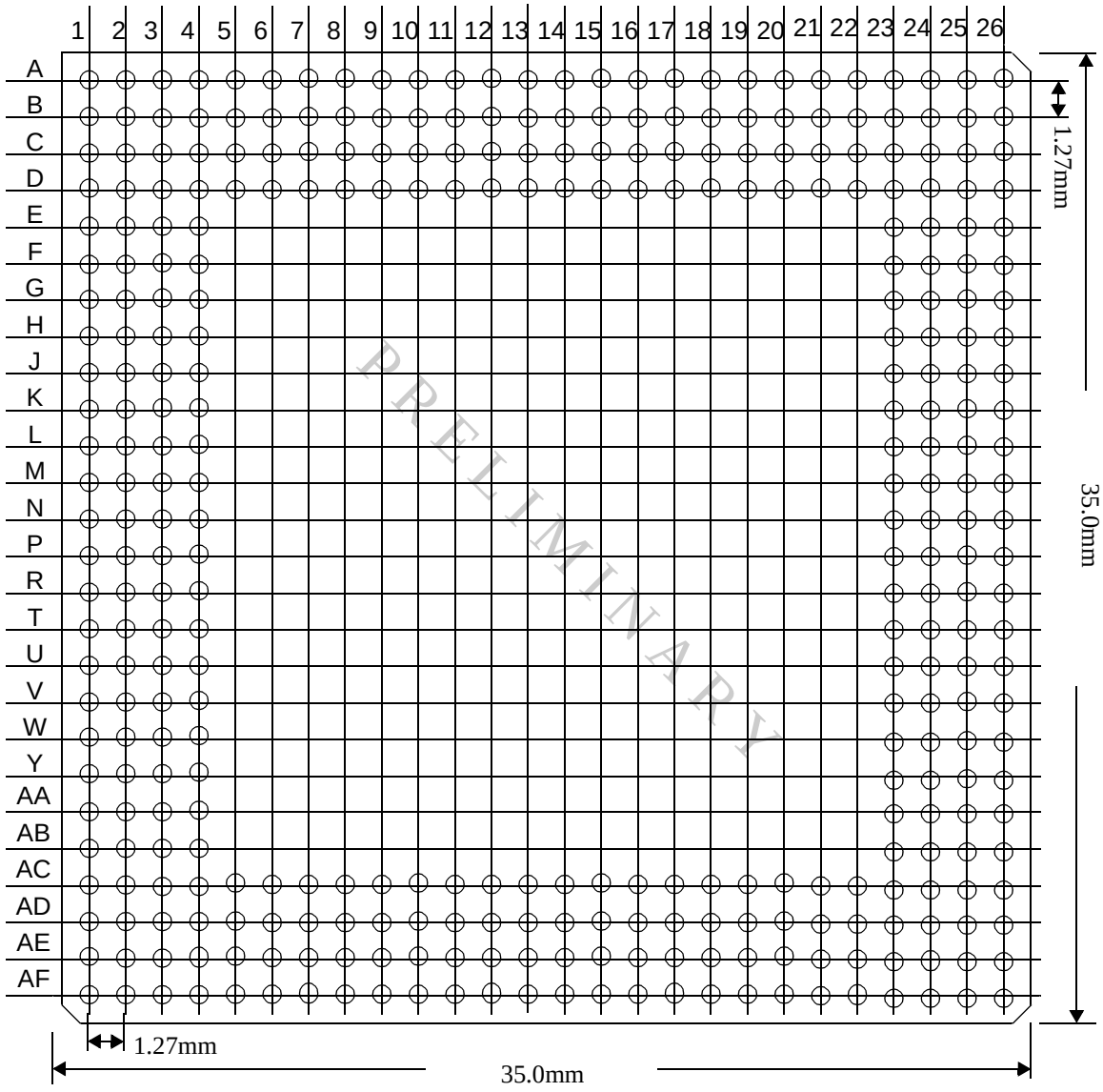

Figure 2.2 Ball Placement Diagram (looking from top, through package)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	VSS	ES_data14	ES_data17	ES_data20	ES_data23	ES_data26	VSS	ES_int#	stataddr0	stataddr2	stataddr5	stataddr8	stataddr11	VSS
B	ES_data12	ES_data13	ES_data16	ES_data19	ES_data22	ES_data25	ES_data28	sysreset#	ES_perr#	stataddr1	stataddr4	stataddr7	stataddr10	stataddr13
C	ES_data10	ES_data11	ES_data15	ES_data18	ES_data21	ES_data24	ES_data27	ES_data29	ES_data30	ES_data31	stataddr3	stataddr6	stataddr9	stataddr12
D	ES_data7	ES_data8	ES_data9	VDD	VDD	VDDIO	VDDIO	VDD	VDD	VDDIO	VDDIO	VDD	VDD	VDDram
E	ES_par1	ES_par3	ES_data6	VDD										
F	ES_par2	ES_par0	ES_addr6	VDDIO										
G	VSS	ES_data1	ES_data0	VDDIO										
H	ES_data4	ES_data3	ES_data2	VDDIO										
J	ES_addr4	ES_addr5	ES_data5	VDD										
K	ES_addr1	ES_addr2	ES_addr3	VDD										
L	ES_clk	ES_oe#	ES_addr0	VDD							VSS	VSS	VSS	VSS
M	n/c	ES_we#	ES_wait	VDDIO							VSS	VSS	VSS	VSS
N	VSS	ES_ce#	tx_pa	VDDIO							VSS	VSS	VSS	VSS
P	tx_prty	scan_en	rx_err	VDD							VSS	VSS	VSS	VSS
R	test1	rx_enb#	rx_val	VDD							VSS	VSS	VSS	VSS
T	test0	tx_data[0]	tx_data[3]	VDDIO							VSS	VSS	VSS	VSS
U	rx_prty	rx_data[1]	rx_data[4]	VDDIO										
V	rx_pa	tx_data[4]	tx_data[7]	VDD										
W	rx_eop	rx_data[3]	rx_data[7]	VDD										
Y	VSS	tx_data[5]	tx_eop	VDDIO										
AA	tx_data[1]	tx_data[6]	crs_dv3	VDDIO										
AB	rx_sop	rx_data[5]	rxd_low3	VDD										
AC	rx_data[0]	rx_data[6]	rxd_high3	VDD	VDD	VDDIO	VDDIO	VDDIO	VDD	VDD	VDD	VDDIO	VDDIO	VDD
AD	tx_data[2]	tx_enb#	tx_en3	VDD	txd_low2	txd_high2	rxd_high1	crs_dv0	tx_en0	mdclk	VDDAF2	bgr_res	Vref	osc25
AE	tx_sop	rx_data[2]	txd_low3'	crs_dv2	tx_en2	crs_dv1	tx_en1	txd_high1	rxd_high0	txd_high0	mdintr_n	VSSAF1	VDDAF1	pktdata63
AF	VSS	nirefclock	txd_high3	rxd_low2	rxd_high2	rxd_low1	VSS	txd_low1	rxd_low0	txd_low0	mdio	VSSAF2	VSS	pktdata62

Table 2.1 Ball Assignment Chart (Left Half)

15	16	17	18	19	20	21	22	23	24	25	26	
stataddr14	stataddr17	stataddr19	stataddr20	statdata5	VSS	statdata10	statdata12	statdata14	test_mode	statclkout	VSS	A
stataddr15	statdata0	statdata1	statdata3	statdata6	statdata8	statdata11	statdata13	statdata15	stat_we#	stat_ce0#	stat_ce1#	B
stataddr16	stataddr18	statdata2	statdata4	statdata7	statdata9	statclkin	stat_oe#	VDD	stat_ce2#	stat_ce3#	pkt_ce0#	C
VDDram	VDD	VDD	VDD	VDDram	VDDram	VDDram	VDD	VDD	pkt_ce1#	pkt_ce2#	pkt_ce3#	D
								VDD	pkt_oe#	pktclkin	pkt_we#	E
								VDDram	pktaddr1	pktaddr0	pktclkout	F
								VDDram	pktaddr3	pktaddr2	VSS	G
								VDD	pktaddr6	pktaddr5	pktaddr4	H
								VDD	pktaddr9	pktaddr8	pktaddr7	J
								VDDram	pktaddr12	pktaddr11	pktaddr10	K
VSS	VSS							VDDram	pktdata0	pktaddr14	pktaddr13	L
VSS	VSS							VDD	pktdata1	pktaddr16	pktaddr15	M
VSS	VSS							VDD	pktdata9	pktdata2	pktaddr17	N
VSS	VSS							VDDram	pktdata10	pktdata4	VSS	P
VSS	VSS							VDDram	pktdata15	pktdata8	pktaddr18	R
VSS	VSS							VDDram	pktdata11	pktaddr19	pktaddr20	T
								VDDram	pktdata16	pktdata3	pktdata5	U
								VDDram	pktdata6	pktdata12	pktdata7	V
								VDDram	pktdata17	pktdata14	pktdata13	W
								VDDram	pktdata35	pktdata18	VSS	Y
								VDDram	pktdata34	pktdata20	pktdata19	AA
								VDD	pktdata33	pktdata22	pktdata21	AB
VDD	VDDIO	VDDIO	VDD	VDD	VDDIO	VDDIO	VDD	VDD	VDD	pktdata24	pktdata23	AC
pktdata61	pktdata58	pktdata55	pktdata52	pktdata49	pktdata47	pktdata44	pktdata41	pktdata38	pktdata32	pktdata26	pktdata25	AD
pktdata60	pktdata57	pktdata54	pktdata51	pktdata48	pktdata46	pktdata43	pktdata40	pktdata37	pktdata30	pktdata28	pktdata27	AE
pktdata59	pktdata56	pktdata53	pktdata50	VSS	pktdata45	pktdata42	pktdata39	pktdata36	pktdata31	pktdata29	VSS	AF

Table 2.2 Ball Assignment Chart (Right Half)

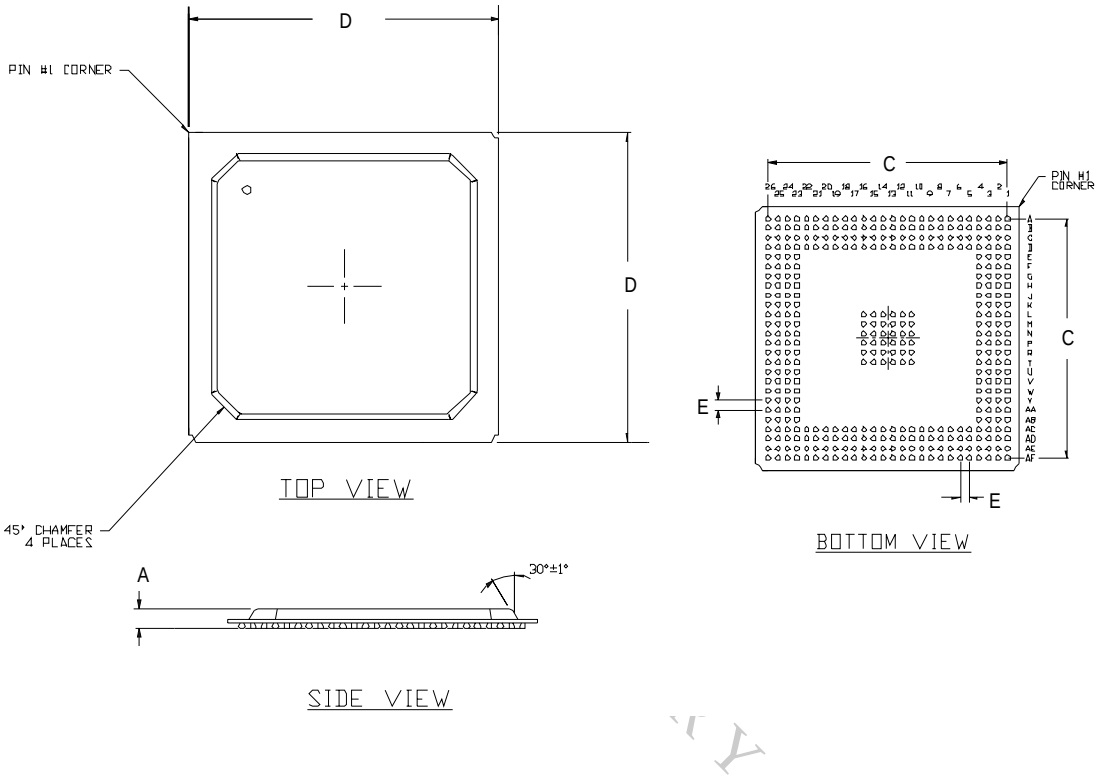

Figure 2.3 Package Dimensions

"A" Max Mounted Pkg Height (mm)	"C" Ball Matrix (mm)	"D,D" Body Size (mm)	"E" Ball Pitch (mm)	Pin Count / Packaging
2.33	31.75 x 31.75	35 x 35	1.27	388 SPBGA

Table 2.3 Package Dimension Details

2.2 Pin Signal Descriptions

The Solo chip pins are grouped as follows:

- EdgeStream Interface Pin Signal Descriptions
- SRAM Interface Pin Signal Descriptions
- Network Interface Pin Signal Descriptions
- Analog, Power, Ground, and Utility Pin Signal Descriptions

The following sections provide signal descriptions for each of these groups of pins.

2.2.1 EdgeStream Interface Pin Signal Descriptions

This section provides a detailed description of the signals for each of the EdgeStream interface pins. For the location of these pins, see cells A18 through D31 in Table 2.1.

Signal Name	Type	Description
ES_Clock	Std TTL [Input]	The Solo chip uses this clock signal to allow burst read/write operations from the packet read and write FIFOs. This clock allows use of a single register access and the subsequent burst read /write of the FIFOs on every leading edge of the clock.
ES_INT#	24 ma [Emulated Open Drain]	The Solo chip asserts this interrupt request signal to indicate that one or more interrupt events have occurred and that the corresponding bits in the Interrupt Register have been set. The Solo chip continues to assert this signal until all interrupt flags are cleared in the respective registers. This signal drives low when an interrupting event occurs. The output emulates an open-drain circuit. When transitioning from low to high (INT cleared), it drives high for a short period before going to a high impedance. This line is not internally pulled up so that it can be OR-tied with INT# pins from multiple Solo devices. An external pull-up resistor is required. This is an active low signal.
ES_PAR[3:0]	24 ma [In/Out]	This parity signal generates a parity bit computed over each byte of the ES_Data[31:0] signals during valid data phases, if the en_prty bit in the ES_ Control register is set (the default after a reset is parity off). The polarity depends on the odd_prty bit in the ES_ Control register. As an input, this line is sampled when the Solo chip is placed in a write cycle and driven when the Solo chip is executing a read cycle. These signals are placed in a high impedance state when the ES_CE# signal is de-asserted or when the ES_OE# signal is high.
ES_PERR#	24 ma [Tri-stated Out]	The Solo chip asserts this Parity Error signal during a write cycle to indicate that a parity error was detected on the ES_Data[31:0] signals. If an error is detected, the write operation is either aborted or goes through anyway, depending on the pewrt_inhibit bit in ES_ Control register (this bit defaults to “write through” after reset). This is an active low signal.
ES_WAIT	24 ma [In/Out]	The Solo chip uses this signal to communicate to an external processor that the register access being processed requires additional cycles to complete. The ES_WAIT signal is active-high.

Table 2.4 EdgeStream Interface Pins

Signal Name	Type	Description
SysReset#	Std TTL [Input]	This System Reset is asserted to perform a hardware reset of the Solo chip. The SysReset# input uses a Schmidt trigger. This is an active low signal.
ES_Addr[6:0]	Std TTL [Input]	These signals provide 7-bit, non-multiplexed address input signals to address the Solo chip registers. Normally, ES_Addr[6:0] should be tied to address pins [8:2] of a 32-bit processor bus. There are two classes of register accesses, direct and indirect. The EdgeStream Interface registers are addressed directly. The registers for the rest of the chip are accessed using an indirect address register (Control Bus Address Register) and an indirect data register (Control Bus Data Register).
ES_CE# ES_WE# ES_OE#	Std TTL [Input]	The external CPU uses the Chip Enable, Write Enable, and Output Enable signals to control the read/write of data from and to the Solo chip. • A write to the Solo chip is accomplished by asserting the chip enable (ES_CE#) and the write enable (ES_WE#) signals while negating the output enable signal (ES_OE#). The pattern on the ES_Data[31:0] pins is then written into the location specified on the address pins (ES_Addr[6:0]) and latched at the location by driving ES_WE# high. • A read from the Solo chip is accomplished by asserting the chip enable (ES_CE#) and output enable (ES_OE#) while negating the write enable (ES_WE#) signals. The contents of the register specified by the address pins appears on the data pins. The ES_Data[31:0] pins are placed in a high impedance state when the ES_CE# signal is negated. If wait states are generated by the Solo chip during the read/write access, the CPU (or any accessing agent) must hold the ES_CE#, ES_WE#, and ES_OE# signal levels constant until the wait is negated. These are active-low signals.
ES_Data[31:0]	24 ma [In/Out]	These signals provide 32-bit, non-multiplexed data signals, used by the external CPU to read/write configuration, status, control, and packet data from or to the Solo chip. These signals are placed in a high impedance state when ES_CE# or ES_OE# signals are de-asserted.

Table 2.4 EdgeStream Interface Pins (continued)

2.2.2 SRAM Interface Pin Signal Descriptions

This section provides a detailed description of the signals for each of the SRAM Interface pins. For the location of these pins, see cells A1 through AD4 in Table 2.1, and A6 -D18 in Table 2.2.

Signal Name	Type	Description
Packet WE#	24 ma [Output]	This packet RAM write enable signal sends a write command (when low) to the packet data SRAM. This signal is asserted in the same cycle as PacketR/W#/ PacketOE# and PacketAddr[20:0] signals, described above. One pin is used for all 64-bit wide RAM devices.
PacketAddr[20:0]	24 ma [Output]	These signals provide 21-bit, non-multiplexed address signals, which the Solo chip outputs to address the SRAM. Since the Solo chip does not access bytes on the data side of the SRAM interface, the “byte access” signals on the SRAM must always be enabled for full access. In conjunction with the eight independent chip-enable signals, these address signals allow the Solo chip to logically address a maximum of 8 Mbytes of memory for packet data while using 256K x 32 SRAMs. For information on the electrical restrictions that limit the amount of RAM that can be connected, see Section 2.3.3, “External SRAM,” on page 26. **Note:** The Synchronous Load (LD#) signal on the SRAM, used to clock in a new address, is permanently enabled when used with the Solo chip.
PacketCE[3:0]#	16 ma [Output]	The Solo chip uses these data buffer chip enable signals to enable the reading and writing of data. To maximize memory cycle time and minimize decode time, four individual PacketCE# signals are available. The decode space enabled by each PacketCE# signal is controlled by setting appropriate bits in the RAM Control Register.
PacketData[63:0]	16 ma [In/Out]	These signals provide 64-bit, non-multiplexed Packet Data signals used by the Solo chip to read and write packet data from and to the SRAM.
PacketR/W# /PacketOE#	24 ma [Output]	This data RAM read/write/output enable signal has a dual function depending on the RAM type specified in the Packet Buffer RAM Control Register. • In RAM mode, this line serves as a Read/Write# signal. It signifies a read cycle when it is high and a write cycle when it drives low.
PktClockIn, StatusClockIn	24 ma [Input]	These clock input signals are connected to the clock output signals. They are available to allow the system designer to match the data signal traces to the clock trace to minimize skew on memory read operations.
PktClockOut, StatusClockOut	24 ma [Output]	These signals provide the SRAM clock. They are 100MHz output from the Solo chip to the SRAM (data and status respectively). They are used to register the address, data, and chip enable inputs on the rising edge. All synchronous outputs meet setup and hold times around the clock’s rising edge.
StatusAddr[20:0]	24 ma [Output]	These signals provide 21 non-multiplexed address signals, which the Solo chip outputs to addresses the Status Buffer. These signals are placed in a high impedance state when the corresponding StatusCE[n]# signals are de-asserted. **Note:** The Synchronous Load (LD#) signal on the SRAM, used to clock in a new address, is permanently asserted when used with the Solo chip.
StatusBW#	24 ma [Output]	The StatusBW# signal is asserted on the same cycle as the StatusAddr[20:0].
StatusCE[3:0]#	16 ma [Output]	The Solo chip uses these status buffer chip enable signals to enable reading or writing of status. To minimize decode time, four StatusCE# signals are available. The decode space enabled by each StatusCE# signal is controlled by setting appropriate bits in the Packet Buffer RAM Control Register.

Table 2.5 SRAM Bus Signal Pins

Signal Name	Type	Description
StatusData [15:0]	16 ma [In/Out]	These signals provide non-multiplexed bidirectional packet status signals, which the Solo chip uses to read and write packet status to the Packet Buffer.
StatusR/W# /StatusOE#	24 ma [Output]	This status buffer read/write/output enable signal has a dual function depending on the RAM type specified in the Packet Buffer RAM Control Register. • In RAM mode, this line serves as a Read/Write# signal. It signifies a read cycle when it is high and a write cycle when it drives low.

Table 2.5 SRAM Bus Signal Pins (continued)

2.2.3 Network Interface Pin Signal Descriptions

This section provides a detailed description of the signals for each of the Network Interface pins. The table below summarizes the pin functions.

Signal Name	Type	Description
Ethernet (RMII) Interface Pins		
CRS_DV[3:0]	Std TTL [Input]	The external RMII PHY asserts these port carrier sense/receive data valid signals when the receive medium for a port is not idle. There are four CRS_DV pins, one for each Network port.
MDClock	8 ma [Output]	This management data clock is a synchronous clock to the MDIO management data input/output serial interface, which may be asynchronous to the transmit and receive clocks.
MDInterrupt#	Std TTL [Input]	This management data interrupt is an active-low input that indicates a change in the Interrupt Status Register of the external PHY device.
MDIO	8 ma [In/Out]	This bi-directional management instruction/data signal may be sourced by the Solo chip, or the external PHY.
NIRefClock	8 ma [Output]	This Network Interface reference clock is a continuous clock that provides the timing reference for the CRS_DV[3:0], RXD_Low/High[3:0], TX_EN[3:0] and TXD_Low/High[3:0] signals. This clock's frequency is 50 MHz.
RXD_Low[3:0] RXD_High[3:0]	Std TTL [Input]	These port receive data signals transition synchronously relative to the NIRefClock. For each clock period in which the corresponding CRS_DV[3:0] signal is asserted, RXD_Low/High receives two bits of recovered data from the RMII Phy. Since the NIRefClock frequency is 10 times the data rate in 10Mb/s mode, the value on RXD_High/Low is sampled every 10th period.
TX_EN [3:0]	8 ma [Output]	These port transmit enable signals indicate that the Solo chip is presenting di-bits on the corresponding TXD_Low/High[3:0] for transmission. These signals transition synchronously with respect to NIRefClock. These signals are asserted synchronously with the first di-bit of the preamble and remain asserted while all di-bits are transmitted. These signals are de-asserted before the first NIRefClock period following the final di-bit of a frame.
TXD_Low[3:0], TXD_High[3:0]	8 ma [Output]	These ports transmit data signals transition synchronously with respect to NIRefClock. When these signals are asserted, the corresponding TXD_High/Low[3:0] di-bits are accepted for transmission by the RMII PHY. • In 100Mbps mode TXD_High/Low[3:0] provides valid data for each NIRefClock period while TX_EN[3:0] is asserted. • In 10Mbps mode, since the NIRefClock frequency is 10 times the data rate, the value on TXD is valid such that TXD_High/Low[3:0] may be sampled every 10th cycle, regardless of the starting cycle within the group, and yield the correct frame data.

Table 2.6 Network Interface Pins

Signal Name	Type	Description
POS-Phy Interface Pins		
RX_Data [7:0]	Std TTL [Input]	OC-3c port Receive Packet Data Bus (8-bit): This bus carries the packet bytes that are read from the FIFO in the external PHY device. The input is valid when RX_Enb# is also asserted at the rising edge of NIRefClock.
RX_Enb#	8 ma [Output]	OC-3c port Read Data Enable: This active-low signal initiates the input data transfer on RX_Data [7:0] bus.
RX_EOP	Std TTL [Input]	OC-3c port Receive End of Packet: This active-high signal marks the end of packet on the RDAT[7:0] bus, when asserted simultaneously with RX_Enb# at the rising edge of NIRefClock.
RX_Err	Std TTL [Input]	OC-3c port Receive Error Indicator: The PHY device uses this active-high signal to indicate that the current packet is aborted and should be discarded. It can be asserted only during the last byte transfer of the packet.
RX_PA	Std TTL [Input]	OC-3c port Receive Packet Data Available: This active-high signal indicates that either some programmable amount of data or an end of packet is available in the Receive FIFO in the PHY.
RX_Prty	Std TTL [Input]	OC-3c port Receive Packet Data Parity: This bit reads the parity (odd or even) for the 8-bit Rx_Data during the data packet reception, if parity check is enabled.
RX_SOP	Std TTL [Input]	OC-3c port Receive Start of Packet: This active-high signal marks the first byte of a packet transfer on RX_Data[7:0] bus, when asserted simultaneously with RX_Enb# at the rising edge of NIRef-Clock.
RX_Val	Std TTL [Input]	OC-3c port Receive Data Valid: This active-high signal indicates the validity of the receive data signals. When RX_Val is high while RX_Enb# is low, the receive signals (RX_Data, RX_SOP, RX_EOP and RX_Err) are valid.
TX_Data [7:0]	8 ma [Output]	OC-3c port Transmit Packet Data Bus (8-bit): This bus carries the packet bytes that are output to the external optical PHY. The output is valid when TX_Enb# is also asserted at the rising edge of NIRef-Clock.
TX_Enb#	8 ma [Output]	OC-3c port Transmit Data Write Enable: This active-low signal indicates the data transmit activity on TX_Data[7:0] bus.
TX_EOP	8 ma [Output]	OC-3c port Transmit End of Packet: This active-high signal marks the end of a packet on TData[7:0] bus. The last byte of the packet is on the bus when this pin and TX_Enb# are both asserted at the rising edge of NIRefClock.
TX_PA	Std TTL [Input]	OC-3c port Transmit Packet Available: This active-high signal indicates that a programmed number of data bytes are available to transfer in the Transmit FIFO when it transitions to high. Once high, it indicates that the Transmit FIFO is not (almost) full.
TX_Prty	8 ma [Output]	OC-3c port Transmit Packet Data Parity: This bit carries the parity (odd or even) for the 8-bit Tx_Data bus during the data packet transmission, if parity generation is enabled.
TX_SOP	8 ma [Output]	OC-3c port Transmit Start of Packet: This active-high signal indicates the first byte of a packet on TX_Data[7:0] bus when asserted TX_Enb# at the rising edge of NIRefClock.

Table 2.6 Network Interface Pins (continued)

2.2.4 Analog, Power, Ground, and Utility Pin Signal Descriptions

This section provides a detailed description of the signals for each of these pins. For the location of these pins, see Table 2.1 and Table 2.2.

Signal Name	Type	Description
Osc25	Analog [Input]	This external reference clock provides the reference timing for the internal clock synthesizer circuit of Solo chip. This 25 MHz clock is used to derive the internal clocks.
BGR_Res	Analog	The band gap reference pin requires a 12.4KΩ 1% resistor to be attached between it and the (analog) ground to insure proper operation of internal current sources.
Vref	Analog	This Receiver Reference Voltage pin must have nominal (2/3 * Vterm) voltage applied to it for interface receivers to operate properly.
Scan_En	Std TTL [Input]	This scan shift enable pin must be grounded for the normal mode of operation.
Test[1:0]	Std TTL [Input]	These test mode selection pins must both be grounded for the normal mode of operation.
Testmode	Std TTL [Input]	This scan test mode pin must be grounded for the normal mode of operation.
VDD	Pwr	These VDD 2.5V power pins drive the core logic.
VDDAF1, VDDAF2	Pwr	This frequency synthesizer power pad must have 3.3V power applied to it to drive internal analog circuitry. A clean, filtered 3.3V should be used.
VDDIO	Pwr	These I/O VDD power pads exclusively for the EdgeStream Interface and RMII transceivers. They should be combined together and shorted to the board 3.3V VDD at one place only.
VDDram	Pwr	These RAM 3.3V power pads are exclusively for SRAM Interface transceivers. They should be combined together and shorted to the board 3.3V VDD at one place only.
VSS[a]	Gnd	These ground pins are for the core logic.
VSSAF1, VSSAF2	Gnd	This frequency synthesizer ground pad is dedicated to the internal analog circuitry.
VSSIO[a]	Gnd	These I/O VSS ground pads are exclusively for EdgeStream Interface and RMII transceivers.
VSSram[a]	Gnd	These RAM ground pads are exclusively for SRAM Interface transceivers.

Table 2.7 Analog, Power, Ground, and Utility Signal Pins

2.3 External Components

This section describes the characteristics and restrictions that apply to the Solo chip's external components. It covers the following topics:

- External reference clock
- Band gap reference
- External SRAM

2.3.1 External Reference Clock

The Solo chip uses one external 25MHz reference clock (Osc25) to generate all other clocks necessary to run the chip, except the ES_Clock (which is supplied from the CPU system, see Table 2.4 on page 19).

The external reference clock may be derived from a discrete oscillator, or from a precision PLL frequency generator. However, it should be free of ripple noise and jitter. The Solo chip's Osc25 pin requires 2.5V CMOS swing instead of 3.3V. If a 5 or 3.3V source is used, perform the level translation before connecting the source to the Solo chip's Osc25 pin.

The Osc25 pin is in location AD1 in Table 2.1. For a description of the Osc25 pin see Table 2.7 on page 24.

2.3.2 Band Gap Reference

A 1% precision resistor provides a reference point for the internal band-gap reference. Place a 12.4KΩ 1% resistor between the BGR_Res pin and the analog ground as illustrated in Figure 2.4.

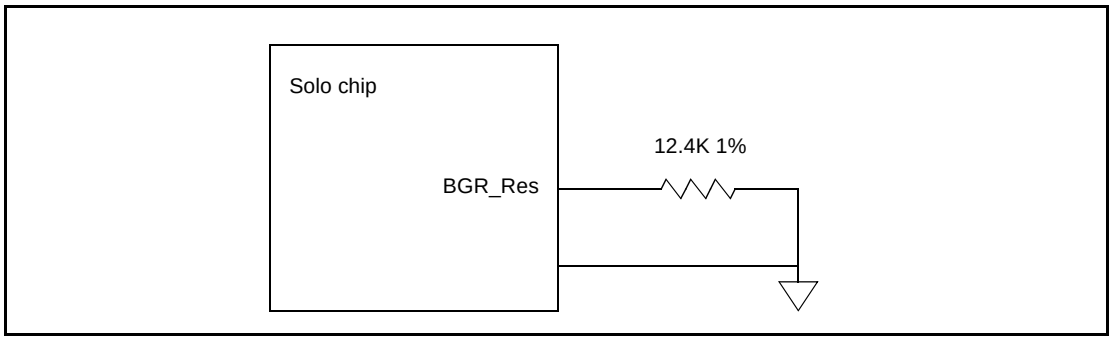

Figure 2.4 Band Gap Reference Resistor

The BGR_Res pin is in location AE2 in Table 2.1. For a description of the BGR_Res pin, see Table 2.7 on page 24.

2.3.3 External SRAM

The Solo chip is designed to work with *pipelined* (recommended) ZBT SRAM for the packet data buffer and the status buffer. It can logically address up to four rows of data RAM devices, up to a 21-bit address range per device, with a maximum addressable RAM capacity of 64MB. In reality, the capacitive loading and RAM availability limit the configuration. Specifically, the Solo chip can directly drive up to eight packet data RAM chips in various configurations, or more if the RAM clock can be buffered-phase locked externally.

Table 2.8 illustrates some of the possible combinations for the memory configurations. In this table:

- A *bank* is a set of RAM chips controlled by the same Pkt_CEx# pin. Since the width of the Packet Data bus is fixed at 64-bit (8-byte), one bank of 256K x 32 bit x 2 chips SRAM represents 256K x 8 = 2MBytes of storage space. Four of these rows comprise the capacity of eight MBytes.
- The Minimum Chip Count column indicates how many SRAM chips are required to implement a “single bank” RAM system (including the status SRAM).
- The Maximum Chip Count column indicates the RAM chip count with maximum allowed number of banks.

Data SRAM Device	Buffer Size	Data SRAM Chip Count	Status SRAM Chip Count	Max.[a] number of banks	Min. Chip Count	Max. Chip Count
128K x 16 e.g., Micron MT55L128L18	1MB x row (2MB Max.)	4 x row	1 x row	2	4 + 1	8 + 2
64K x 32 e.g., Micron MT55L64L32	512KB x row (2MB Max.)	2 x row	1 x row (use 64K x 16)	4	2 + 1	8 + 4
256K x 16 e.g., Micron MT55L256L18	2MB x row (4MB Max.)	4 x row	1 x row	2	4 + 1	8 + 2
128K x 32 e.g., Micron MT55L128L32	1MB x row (4MB Max.)	2 x row	1 x row (use 128K x 16)	4	2 + 1	8 + 4
256K x 32	2M x bank (8MB Max.)	2 x bank	1 x bank (use 256K x 16)	4	2 + 1	8 + 2

Table 2.8 Recommended RAM Configurations

a. Maximum number of banks based on the four-chip loading limit specified below. The device allows up to eight rows of RAMs to be attached, but careful electrical considerations must be made to go beyond this limit.

As indicated in Table 2.8, an independent set of data RAM (64-bit wide) and status RAM (16-bit) is required. For the data port, depending on whether the RAM is 16-bit wide or 32-bit wide, four or two chips per row are needed. Each Solo device can logically support up to eight rows, but the driver electrical properties limit the number of RAMs directly attached to the bus to eight as shown in the table’s Data SRAM Chip Count column.

Note: In general, for a given size RAM, use a 32-bit device to limit the RAM chip count; use

a 16-bit device to maximize the buffer capacity.

The SRAM interface transceiver pads are designed with following loading assumptions:

RAM Control Pin Input Capacitance:	4pF Max
SRAM Data Pin Input Capacitance:	4pF Max
SRAM Address Pin Input Capacitance:	3.5pF Max
Maximum Number of Data SRAMs:	8
PC Board Trace Capacitance Allowance:	3pF / bank Max
Maximum Loading on Address Pins:	34pF Max
Maximum Loading on Data Pins:	23pF Max

The Solo chip can connect more SRAM devices than described above. For example, sixteen 128K x 32 RAMs instead of eight 256K x 32 can be used to get an eight MByte capacity by using PacketAddr[20] as one of the chip enable signals (see Table 2.5 on page 21 for a description of PacketAddr[20]). Since such applications require heavier electrical loading, careful electrical and timing analysis must be followed to insure its proper operation.

The type and size of the RAM chips being using in the Packet Buffer RAM Control register must be programmed. Figure 2.5 illustrates how to program this type of configuration:

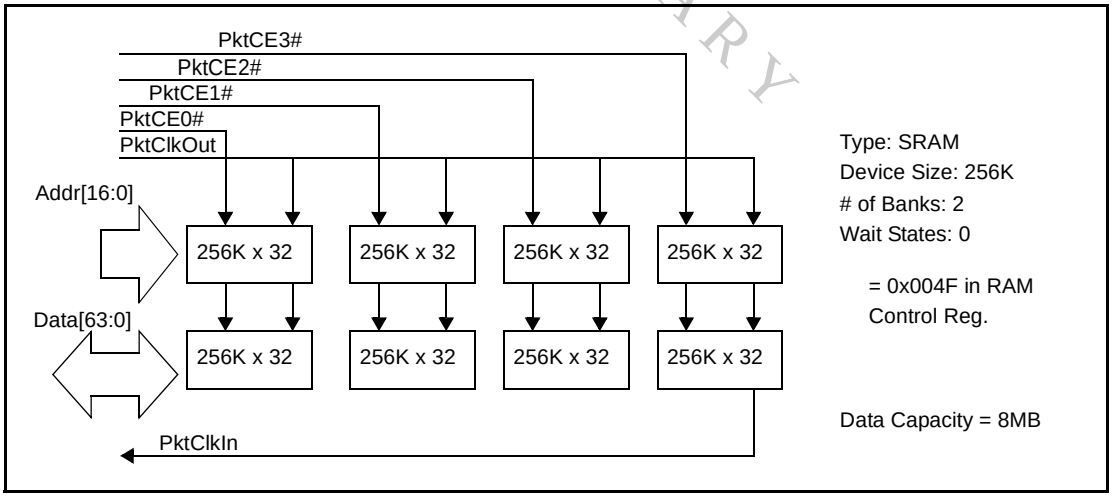

Figure 2.5 RAM Configuration Example

Solo is designed to work with SRAMs of various types rated at 100 MHz or faster. To accommodate cost sensitive applications, the following various programmable parameters are provided to interface to slower RAMs. Contact Entridia for the most current SRAM support information.

Device Types
Pipelined ZBT SRAM is currently recommended for optimal performance, support for alternative types of SRAM will be supported as they become available:

00 Reserved
01 Reserved
10 Reserved
11 Pipeline mode ZBT SRAM

Device Address Space
The number of the column addresses the specified RAM chip has. This defines the size of each RAM bank. Each column is 8-bytes wide (packet) and 2-bytes wide (status).

000 15-bit -- 32K columns
001 16-bit -- 64K columns
010 17-bit -- 128K columns
011 18-bit -- 256K columns
100 19-bit -- 512K columns
101 20-bit -- 1M columns
110 21-bit -- 2M columns

Number of Memory Banks
The number of banks of packet/status RAMs. Each bank is selected by one of the four chip enable (packetCE[3:0]#, statusCE[3:0]#) pins.

0000 Reserved
0001 1 bank
0010 2 banks
0011 3banks
0100 4 banks
0101 - 1111 Reserved

Chip Enable Setup Time (CSS)
When PacketCE[3:0]# / Status_CE[3:0]# and other control pins are negated for a while, some RAM chips enter a sleep mode. They may take some extra time before they wake up, though such timings are often not specified. Solo accommodates such RAM chips by inserting a clock cycle delay between PacketCE[3:0]# / Status_CE[3:0]# assertion to setting of all other address/data/control signals.

0 No extra chip enable setup time is set. PacketCE[3:0]# / Status_CE[3:0]#, address, control and/or data are coincident.
1 One clock delay is inserted between PacketCE[3:0]# / Status_CE[3:0]# assertion from the rest of the control signals.

The RAM interface assumes that a given application uses the same size RAM for data and status storage. For example, if 128K (x16 or x32bit) devices are used for the packet data SRAM, use a 128K x 16 device for the status SRAM.

Actual wiring of RAM interface pins to the RAM devices depends on the type and configuration of the RAM device. Table 2.9 shows wiring examples for cases using RAM using the popular pin-out from those devices by Micron Technology, IDT, and Motorola.

Solo Chip Pin-Out	RAM	
Both Status and Data RAMs		
	$\overline{LD}$ = VSS LBO = VDD CKE = VSS CE2 = VDD CE2 = VSS $\overline{OE}$ = VSS ZZ = VSS	
Status RAMs		
StatusClockOut	CLK	
StatusClockIn	(Clock return from the end of the RAM array)	
StatusCE#	CE	
StatusR/W# / StatusOE#	R/$\overline{W}$	
StatusWE#	 $\overline{WE}$ = VSS $\overline{OE}$ = VSS	
StatusAddr[20:0]	SA, SA1, SA0	
StatusData[7:0] StatusData[15:8]	DQa [7:0] DQb[7:0]	
Packet Data RAMs		
PacketClockOut	CLK	
PacketClockIn	(Clock return from the end of the RAM array)	
PacketCE#	CE	
PacketR/W# / PacketOE#	R/$\overline{W}$	
PacketWE#	 $\overline{WE}$ = VSS $\overline{OE}$ = VSS	
PacketAddr[20:0]	SA, SA1, SA0	
PacketData[63:32] PacketData[31:0]	DQa, DQb, DQc, DQd DQa, DQb, DQc, DQd	

Table 2.9 Device to RAM Wiring Chart

Due to the large capacitive load it represents, the board layout of the RAM array must use a thick trace to allow for a relatively large driving current for each address and data pin, and must have an ample ground and power plane to insure proper de-coupling and minimize the ground bounce potential.

An external clock distributor chip may be used to drive more RAM chips, as shown in Figure 2.6. The Data RAM clock output (PktClockOut) pin has the heaviest load at the highest duty cycle. If that pin can be buffered effectively, the number of RAMs can be doubled. However,

take care to critically analyze the timing margin when designing a system in this way. In this configuration, it is estimated that up to 16 chips can be driven, bringing the total capacity to 16 MB, using 256K x 32 RAM.

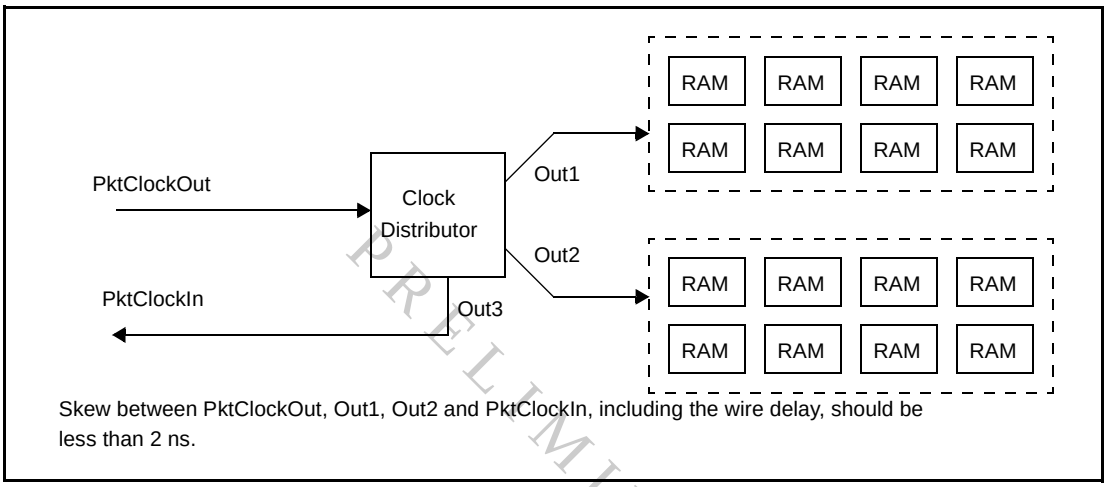

Figure 2.6 External RAM Clock Buffering

Chapter 3 System Interface Operation

This chapter describes the electrical characteristics and timing specifications for the Solo chip.

3.1 Electrical Characteristics

This section describes the following electrical characteristics of the Solo chip:

- The absolute maximum ratings
- Power sequencing for power-up and reset
- D.C. operating characteristics
- I/O pin types and electrical characteristics

3.1.1 Absolute Maximum Ratings

The absolute maximum ratings for the Solo chip are as follows:

Storage Temperature	-55°C to +125C°
Operating Power Supply Voltage (VDD pin)	3.6 V
Input Voltage with Respect to Ground	-0.5V to 5.5V
ESD Immunity	2.0 KV human model

3.1.2 Power Sequencing

The 2.5 V power supply should always be lower than the 3.3 V power supply, even at power-up. For a proper power-up reset, the SysReset# signal must be low until all power-supply voltages reach at least to the lowest “normal” range. Figure 3.1 illustrates the power supply rise curves and the SysReset# signal.

Note: The clock signal Osc25 must be within specified tolerance before the 2.5 V and 3.3 V power supplies reach normal operating range. Thereafter, SysReset# must remain asserted until the power supplies have stabilized for a minimum of 1 millisecond. Solo requires a maximum of 10 microseconds after SysReset# is negated to complete the internal initialization phase. After initialization is complete all generated clocks will be stable and within specified tolerance.

For more information on the SysReset# signal, see Section 2.2.1, “EdgeStream Interface Pin Signal Descriptions,” on page 19.

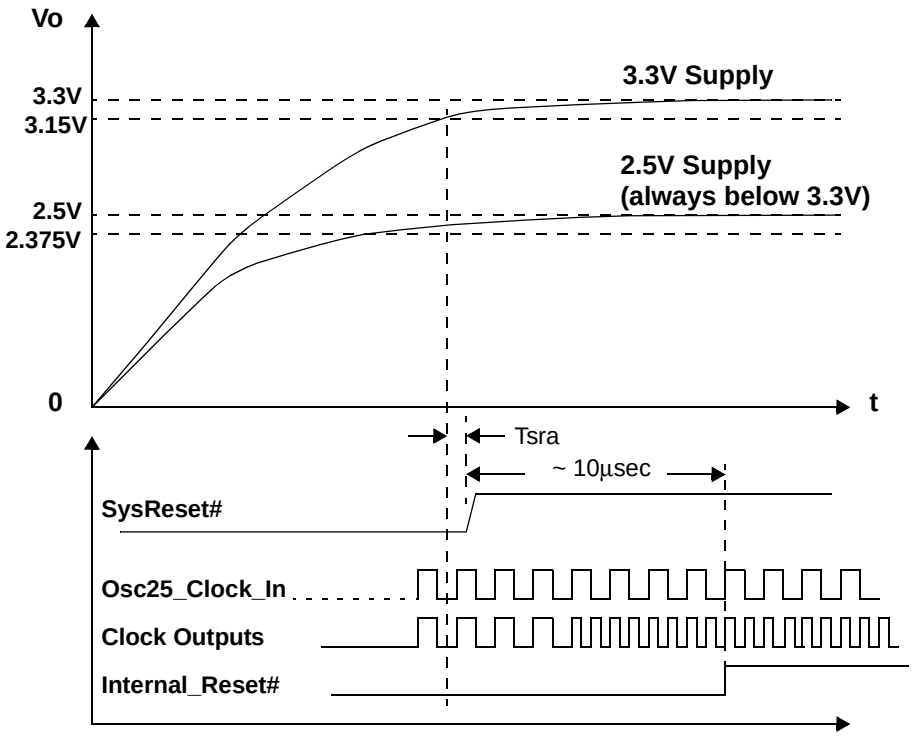

Figure 3.1 Power Supply Rise Curves and System Reset

3.1.3 D.C. Operating Characteristics

Table 3.1 provides a detailed description of the D.C. operating characteristics.

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Condition/Comment
Ta	Operating Ambient Temperature	0		70	°C	
Vdd	Operating Supply Voltages: VDD IOVDD RAMVDD OS_B3V VDDAF1, 2 VDDAB	 2.375 3.15 3.15 3.15 3.15 3.15	 2.5 3.3 3.3 3.3 3.3 3.3	 2.625 3.45 3.45 3.45 3.45 3.45	 V V V V V V	 ±5%
Idd	VDD current[a] IOVDD+RAMVDD+OS_B3V VDDAF1+VDDAF2+VDDAB			2,500 3,000 50	mA mA mA	All outputs high-Z, All inputs negated, osc25 = 25MHz @All xVDD at maximum

Table 3.1 D.C. Operating Characteristics

Pd	Maximum Power Dissipation[b]		8.5	Watt	All outputs active, All inputs active, osc25 = 25MHz @All xVDD at maximum
Iil	Input Leakage Current (All pins w/o pull-ups)	-10	+10	µA	-0.0V ≤ Vi ≤ VDD
Vi(max) Vi(min)	Max. operating input voltage Min. operating input voltage	 0	5.0 3.6 	V V V	“5V tolerant” pins Non-5V tolerant & analog pins all pins
Vih(Osc25) Vil(Osc25)	Input high voltage for Osc25 Input low voltage for Osc25	1.6	 0.9	V V	Osc25 clock input is at 2.5V logic swing.
Vih/Vil Ioh/Iol VHyst	Various I/O parameters (except for Osc25 pin above)				See Table 3.2
Vbgr	Band Gap Reference Voltage	1.23 1.25	1.26	V	At BGR_Res pin, with 12.4KΩ to ground attached
V_{ref}	Bus Termination Voltage	1.35 1.5	1.65	V	

Table 3.1 D.C. Operating Characteristics (continued)

a. Total current through all VDD pins at the specified condition.
b. The package alone is not expected to dissipate this much heat. Heatsink attachment and forced air cooling is required.

3.1.4 I/O Pin Types and Electrical Characteristics

Table 3.2 shows the I/O pin types and electrical characteristics of the Solo chip:

Type	Dir.	V_{Hyst} (min)	V_{ih} / V_{il} (min)(max)	Internal Pullup	I_{oh}	I_{ol}	5V TolIrnt	Tri-State	C_{load}
8 ma	I/O	no	0.65 / 0.35 VDD	no	-8.0mA @Vo ≥ 2.4V	8.0mA @Vo ≤ 0.4V	yes	yes	30pF
16 ma	I/O	no	0.65 / 0.35 VDD	no	-16.0mA @Vo ≥ 2.4V	16.0mA @Vo ≤ 0.4V	yes	yes	
24 ma	I/O	no	0.65 / 0.35 VDD	no	-24mA @Vo ≥ 2.4V	24mA @Vo ≤ 0.4V	yes	yes	
Input Only	I	no	0.65 / 0.35 VDD	no	-	-	yes	n/a	n/a
Hysterisis Input	I	1V	2.15V / 1.05V	no	-	-	yes	n/a	n/a
GTL+ open drain	I/O	no	1.05 / 0.95	no	(Open Drain)	40mA @Vo = 0.5V	no	yes	
Analog	-	n/a	n/a	no	n/a	n/a	no	n/a	

Table 3.2 I/O Pin Types and Electrical Characteristics

3.2 External Timing Specification

Refer to the applicable sections in the Solo Data Book for details on timings for the EdgeStream, Network, and SRAM interfaces.

Chapter 4 Programming Guide

This part of the document describes the function, interface, and implementation of the configuration and management software for the Solo chip. The software components and interfaces described here are defined using WindRiver Corporation's VxWorks Real-Time Operating System (RTOS).

The control software for the Solo chip consists of the following major components:

The Solo device driver: This driver constitutes the low-level software interface to the programmable functions of the Solo device. This component consists of an RTOS-dependent sublayer and a Solo device-dependent sublayer.

The Solo service programming interface: This component consists of a high-level library of C functions that presents an abstraction layer built on top of the facilities provided by the RTOS device driver.

4.1 Theory of Operation

Refer to the Solo Data Book for complete details on the theory of operation for programming the Solo chip. Included in the Data Book is specific information for the following areas of operation.

- Solo Device Configuration
- EdgeStream Interface Operation
  - Accessing the Solo chip
  - EdgeStream Interface Packet Transfers
  - Reading packets from the Solo chip
  - Writing Packets to the Solo chip
  - Multicast Packet Handling
  - Register Read and Write Operations
  - Route Table
  - Filter Table
- Packet Buffer Manager Operation
  - Packet Buffer Organization
  - Packet Buffer Queue Types
  - Using the Queues

- Packet Buffer Operations

- Operation of the Network Interfaces
  - PHY Interface
  - Layer 2 Filtering
  - Layer 3 Functions
  - Packet Receive Process
  - Network Management Process

Chapter 5 Register Reference

5.1 Overview

The Solo chip is mapped into 512 bytes (32-bits wide) of CPU address space. These registers are described in the “EdgeStream Interface Registers” section in the Solo Data Book.

There are several hundred more internal registers to this device. These registers cannot be accessed directly; they are accessed indirectly via the Control Bus Address and Control Bus Data registers (80 and 84 hex respectively). These internal registers are also described in the “Internal Registers” section in the Solo Data Book.