Serenade Data Sheet

ENT3002—Wire-Speed Router IC for Access Networks

Revision 1.2

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Preface

This document describes the design features and functional descriptions for the Entridia Serenade™ wire-speed router IC for Access Networks.

Serenade is ideally suited for IP based aggregation systems in Access networks, and is part of Entridia's OPERA™ (Optical Edge Routing Architecture) family of products targeted at high performance aggregation routers. Serenade incorporates two OC-3c Packet-over-Sonet (PoS) ports via Entridia's OCPort™ interface and offers connectivity to legacy WAN networks via Entridia's EdgeStream™ interface and glueless expansion via the OptiStream™ expansion bus.

References

- *POS-PHY Saturn Compatible Packet Over SONET Interface Specification (Level2),* PMC-Sierra Inc. / Saturn Development Group, PMC-971147 Issue 5, December 1998
- IETF Network Management RFCs
  - RFC 1812 "Requirements for IP version 4 Routers"
  - RFC 1213 "Management Information Base for Network Management of TCP/IP based internets: MIB-II"
  - RFC 2474 "Definition of the Differentiated Services Field (DS Field) in the IPv4 and IPv6 Headers"
  - RFC 2475 "An Architecture for Differentiated Series"

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Chapter 1 Functional Description

Entridia Corporation's Serenade chip is a fully integrated, wire-speed classical IP router chip targeted at high performance routing systems. The architecture of the Serenade chip supports Data Link (OSI Layer 2) and Physical (OSI Layer 1) interface technologies, such as Packet-Over-Sonet and ATM at OC-3c rates, DSL, T1/T3, and broadband cable. A high-speed expansion port on the chip supports cascading four Serenade devices to form large port-count systems. With aggregate throughput of 1.2 Gbps and guaranteed ingress-to-egress latency of eight microseconds, the Serenade chip is ideally suited for converged access aggregation edge routing systems.

The primary function of the Serenade chip is to route IP packets using information contained in the header of each packet and knowledge (routes) of which groups of IP addresses (subnets) are reachable through its network interfaces.

This chapter describes the features and functions supported by the Serenade chip.

1.1 Data Link Layer (OSI Layer 2) Frame Processing

Serenade has two OC-3c line-rate ports that provide the connection to the network. Through these port interfaces Serenade transmits and receives PPP encapsulated IP packets with optional 32-bit tags attached. An external Layer 2 device is required to add the appropriate framing/deframing to PPP packets transmitted from Serenade. The maximum packet size for the OC-3c ports is 1,536 bytes.

1.2 Network Layer (OSI Layer 3) Packet Processing

Once a Layer 2 frame has been successfully received without errors by a Network Interface, the Network Layer processing logic takes over. For IP packets, the Layer 3 processing logic includes the following functions:

- Verify the header checksum of an incoming packet.
- Verify the validity of the IP Time to Live (TTL) field, decrement the TTL field appropriately, and recalculate the IP checksum field.
- Look up destination interface in the route table (refer to Route Table - Section 1.4) using the destination address and IP type of service field and queue the packet for transmission.

- Prioritize the transmission of packets based on the contents of the IP Type of Service (TOS) field.
- If enabled, search the flow table (refer to Flow Table Section 1.5) for rules that apply to the source and destination IP address, source and destination port (TCP, UDP or other Layer 4 port) of each packet. Then, perform the specified action (forward, drop, or invoke processing hooks in software running on the companion microprocessor).
- Notify the companion microprocessor of IP Multicast, ICMP, and non-IP protocol packets. Permit software running on the microprocessor to determine handling for such packets and queue them for transmission from the appropriate output interface.

1.3 EdgeStream Interface

The EdgeStream Interface is the microprocessor interface of the Serenade device. It consists of a 32-bit data bus and a 16-bit address bus.

This interface presents Serenade as a memory-like device to the microprocessor. An extensive register map enables software running on the microprocessor to initialize and dynamically reconfigure the Serenade chip.

This interface also includes an interrupt line, which is used to notify the microprocessor of exception conditions and periodic events. Notification of specific conditions can be masked or enabled by programming appropriate interrupt control registers.

1.4 Route Table

The Serenade chip has a built-in 512 entry route table with full support for longest prefix match look up, essential for Classless Interdomain Routing (CIDR). As route lookup can be performed in three cycles using this approach Serenade can guarantee wire-speed processing with deterministic latency. The Serenade chip route table also supports using the IP TOS field in making Quality of Service (QOS) policy based destination route selection.

The on-chip 512 entry table can be extended at the system level by using a 64K external table memory that communicates with the Serenade chip via the OptiStream Interface or a memory manager like the Entridia ENT2003 Sonata™ controller.

Configuration software running on a companion microprocessor can install static routes (including a default gateway entry) and periodically age and rebuild other entries dynamically as a result of routing protocol messages (such as OSPF and BGP4). Also, the companion microprocessor can maintain very large route tables in system memory and use the on-chip 512 entry table as a cache for frequently used routes.

	Lookup Terms		Lookup Result	
Valid 1-bit	DestIP/Tag 32-bit	TOS 8-bit	NextHopIP 32-bit	NextHop Interface Number 8-bit
	VLSM 32-bit			

Table 1.1 Route Table Entry

1.5 Flow Table

The Serenade chip has a 256 entry flow table that can be extended to 64K flows via off chip memory connected to the OptiStream interface, or by a memory manager like the Entridia ENT2003 Sonata controller. The flow table maintains filtering rules to determine which types of IP packets a network interface can forward or discard, and which types require further examination by software running on a companion microprocessor.

Each flow table entry can specify a source and destination IP subnet, source and destination port (TCP, UDP or other Layer 4 port) along with an action to take if any or all of these fields match those of the packet being filtered. The action can specify one of the following:

- Forward: Accept the packet, and forward it normally.
- Priority Forward: Accept the packet, and forward it with priority over normal packets.
- Drop: Discard the packet and account for it in the management counters.
- Examine: Accept the packet and notify a companion microprocessor of the match and the starting address of the packet data in the Packet Buffer memory. This enables additional filtering software running on the microprocessor to further process the packet.

	Lookup Terms			Lookup Results	
Valid 1-bit	Layer 3 Parameters	Layer 4 Parameters	Chip Interface Number 4-bit	Action 2-bit	Priority 6-bit
	See Table 1.3	See Table 1.4			

Table 1.2 Flow Table Entry

DestIP 32-bit	SrcIP 32-bit	Protocol 8-bit	TOS 8-bit
VLSM 32-bit	VLSM 32-bit		

Table 1.3 Layer 3 Parameters

DestPort Number (TCP/UDP)		SrcPort Number (TCP/UDP)	
Lower Limit 16-bit	Upper Limit 16-bit	Lower Limit 16-bit	Upper Limit 16-bit

Table 1.4 Layer 4 Parameters

1.6 Queue Management

The Serenade chip architecture implements a hybrid input and output queuing model, which enables extensible end-to-end quality of service in a router system.

One OC-3c port has 8 levels of priority and the other port 2 levels of priority. Additional scheduling can be added via the Entridia OptiStream Interface. The priority output queues can be selected based on the type of service, source or destination IP addresses, and TCP, UDP or other Layer 4 ports, or a valid combination of the aforementioned parameters, making it highly flexible for system designers to implement policy-based wire-speed routing rules for the OC-3c ports. Serenade has a built in weighted round-robin scheduler with user programmable weights.

1.7 OptiStream Expansion Bus

The expansion bus of the Serenade chip is an enhanced glueless Gunning Transceiver Logic (GTL+) interface which can operate at frequencies up to 100 Mhz. This 64-bit wide data bus supports a sustained throughput of 6.4 Gbps, allowing the system designers to cascade up to four Serenade devices, thereby forming an 8-port OC3c PoS, wire-speed IP router and the attachment of an external memory manager like the Entridia ENT2003 Sonata controller.

1.8 Software Interface

Entridia provides complete software drivers and a Service Application Programming Interface (API) to enable system designers to quickly migrate their existing software to the Serenade platform.

The software drivers are targeted to the Wind River Systems' VxWorks real-time operating system. However, the drivers use a hardware abstraction model that makes it very easy to port to other real-time operating systems.

To enable quick integration with existing software in routers, the Entridia driver presents the Serenade network interface as two independent network devices. The router software that deals with Network Layer communications can treat each of the interfaces as a dedicated Data Link Layer device and interoperate with them without modification.

In addition to the drivers, the Service API is a library of C functions that simplify access to the more advanced features of the Serenade chip such as filtering rules and traffic shaping parameters.

1.9 System Integration

The Serenade chip is designed to integrate into Access/Service Provider edge routing systems without significant modification to the software currently running on those systems, while accelerating their performance and increasing functionality.

The Serenade device can handle the following functions, which are currently handled by a microprocessor or discrete programmable logic, without any software intervention:

- Packet forwarding: The Serenade chip transfers all packet data into and out of the Packet Buffer memory.
- Route look up: The Serenade chip searches for the longest prefix match for a destination IP address in the route table.
- Packet filtering rules: The Serenade chip forwards or discards packets based on rules in the flow table.
- Packet Buffer management: The Serenade chip allocates and reclaims space for the packets in the Packet Buffer memory.
- IP Multicast: The Serenade chip manages transmission of multicast packets to all the recipient ports without unnecessary data copying.
- IP based QoS: Priority Scheduling; weighted round-robin.

Chapter 2 Hardware Description

This chapter provides a hardware description of the Serenade device. This chapter also describes the Serenade chip external signals. It provides detailed pin-out diagrams and describes each of the signals.

The Serenade chip integrates two PoS OC-3c ports. Multiple Serenade devices can be cascaded together, via OptiStream, to build a policy based, wire-speed router supporting both LAN and WAN protocols. The device is packaged in a 520-pin HPBGA.

The device has four major external interfaces:

- OptiStream interface
- EdgeStream interface
- SRAM interface
- Network OC3-c interface

OptiStream Interface. This proprietary bus operates at frequencies of up to 100 MHz. It is a low voltage swing interface that uses terminated Gunning Transceiver Logic (GTL+) and implements a Time Division Multiplexed (TDM) bus access mechanism. It communicates control information and data between multiple Serenade devices.

In a system where several Serenade devices are cascaded, a single master device is designated to control access to the OptiStream Interface. The total throughput on the bus is divided into single cycle transactions, defined by the system's clock frequency. The master device grants access to the bus sequentially to initiators for a single cycle. If an initiator does not have a transaction pending, bus access is granted to the next pending initiator in sequence. This circuit-switched concept provides guaranteed bandwidth and latency to all packets in the system.

The integrated GTL+ transceivers used on Serenade enable direct interconnection of cascaded Serenade devices, via the OptiStream Interface, without any external support devices. The bus however, must be terminated externally.

The OptiStream interface also allows for expansion of the Route and Flow tables to support 64K flows at full line-rates.

EdgeStream Interface. This generic memory interface is designed so that system OEMs can manage the Serenade chip as a memory mapped device. This interface supports the use of an external CPU. In this way, system integrators can preserve their existing investment in Network Operating System software. In addition, system integrators can further differentiate their products by providing additional policy-based routing, bridging, VLAN, QOS, and/or VPN functionality layered with Serenade devices.

SRAM Interface. The synchronous SRAM memory interface operates at 100MHz, and is used

to interface with industry standard SRAMs available from various suppliers. The external SRAM is used as a Packet Buffer for storing network packet data in queued data structures. Packets arriving via the Network Interface, the OptiStream Interface, or the EdgeStream Interface are always buffered in the Packet Buffer to permit additional processing before transmission.

Network Interface. This interface uses two OC-3c ports using a Packet-Over-Sonet POS-PHY Level 2 interface.

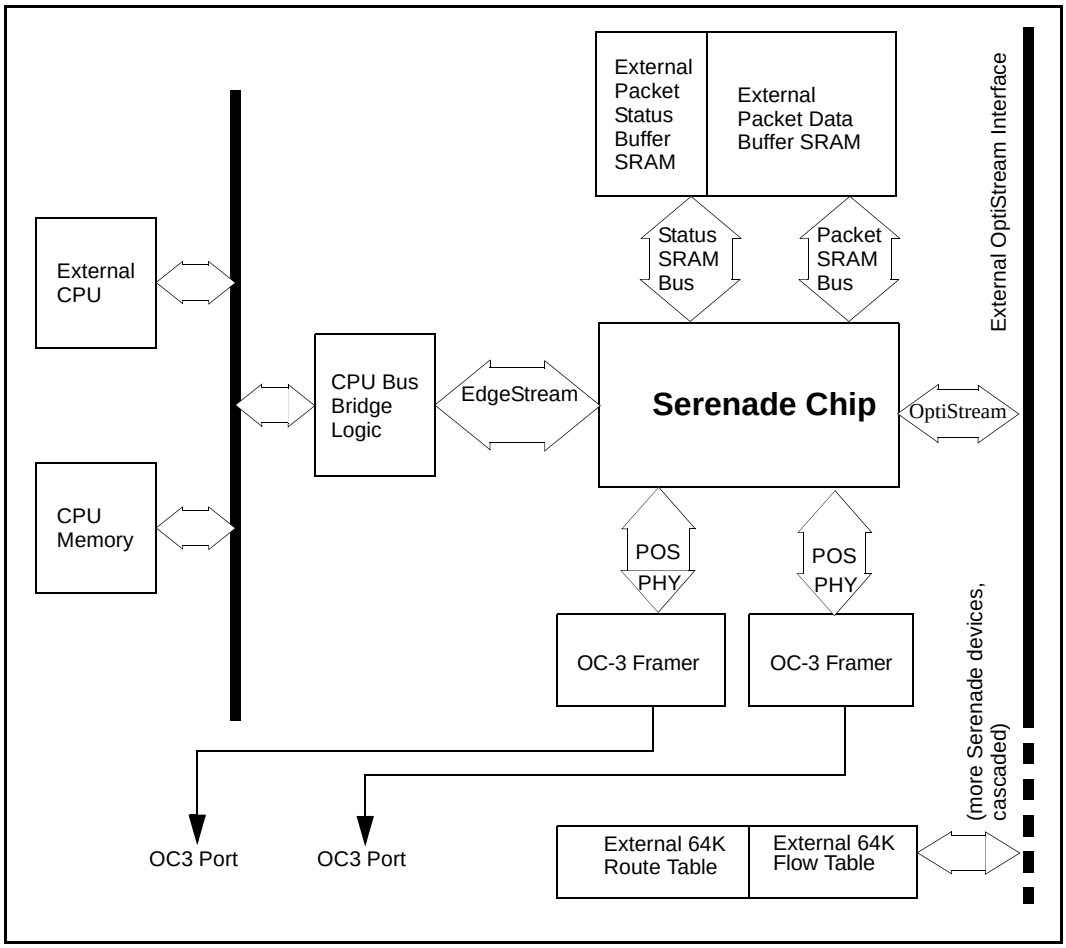

Figure 2.1 Serenade System Block Diagram

2.1 Pin-Out

Figure 2.2 is a ball placement diagram of the Serenade chip. The labels on the x and y axes provide reference between this diagram and the signal descriptions. The maximum height (above board) of the package including solder balls is 1.4mm.

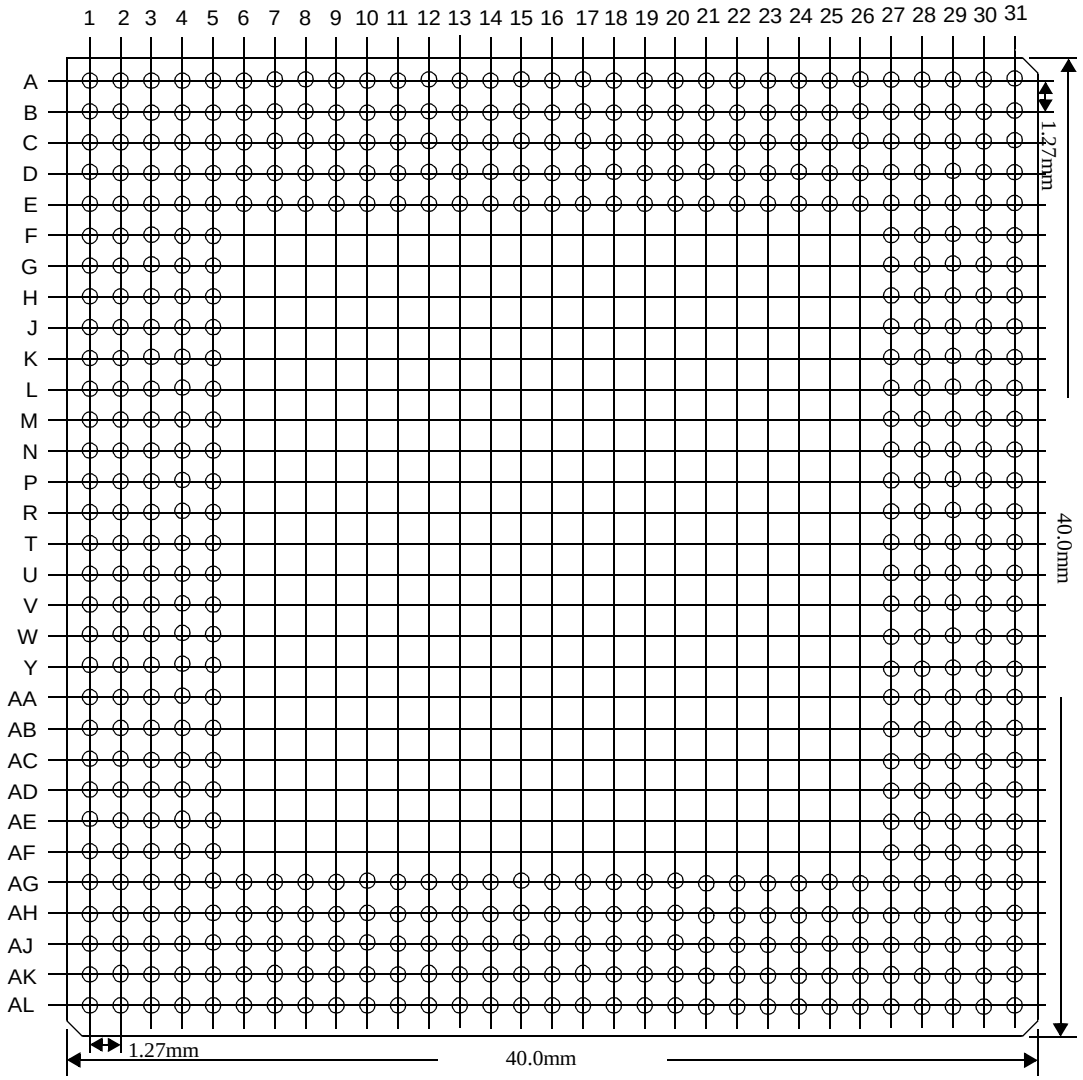

Figure 2.2 Ball Placement Diagram (looking from top, through package)

2.1.1 Package Details

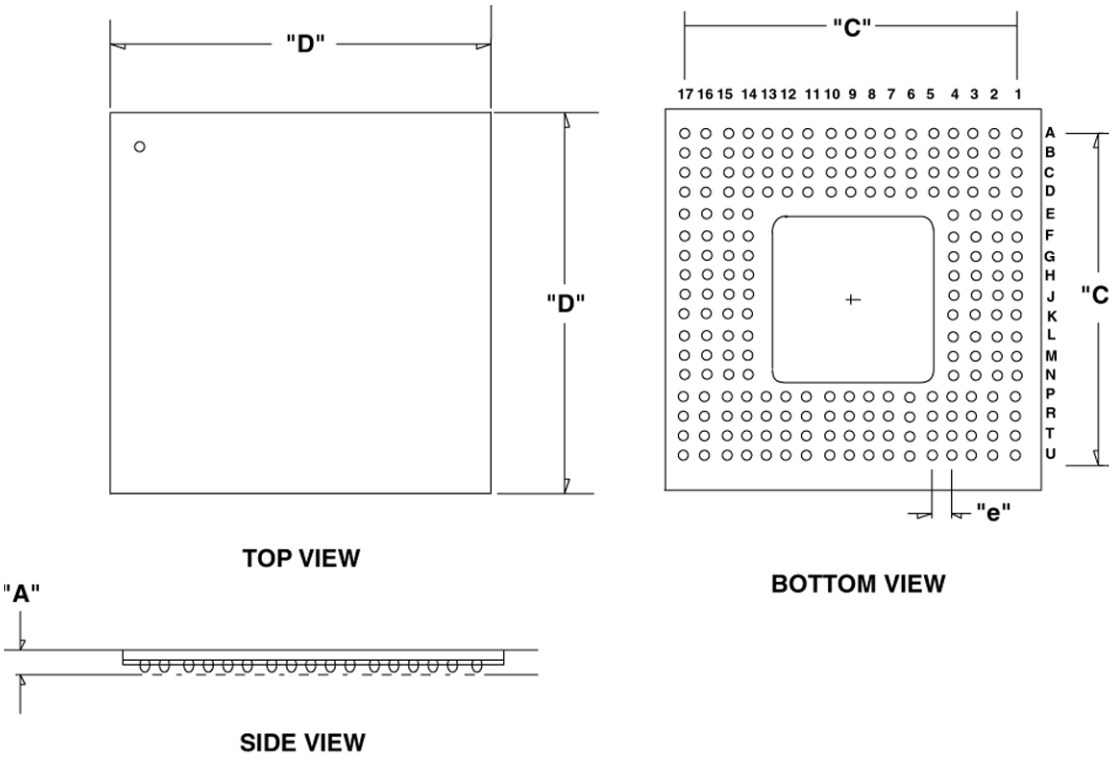

Figure 2.3 Package Dimensions

"D,D" Body Size (mm)	"A" Max Mounted Pkg Height (mm)	"C,C" Ball Matrix (mm)	"E" Ball Pitch (mm)	Pin Count / Packaging
40x40	1.4	31x31	1.27	520 HPBGA

Table 2.1 Package Dimension Details

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	pkt_ce3#	pktce2#	pktce1#	pktce0#	VSS	stat_ce3#	statclkout	statclkin	statdata12	statdata8	statdata4	statdata0	stataddr17	stataddr13	stataddr9	stataddr5
B	pktclkout	pkt_we#	pkt_rwoe#	pktclkin	VSS	VSS	stat_ce0#	statrwoe#	statdata13	statdata9	statdata5	statdata1	stataddr18	stataddr14	stataddr10	stataddr6
C	pktaddr3	pktaddr2	pktaddr1	pktaddr0	VSS	VSS	stat_ce1#	test_mode	statdata14	statdata10	statdata6	statdata2	stataddr19	stataddr15	stataddr11	stataddr7
D	pktaddr7	pktaddr6	pktaddr5	pktaddr4	VSS	VSS	stat_ce2#	stat_bw#	statdata15	statdata11	statdata7	statdata3	stataddr20	stataddr16	stataddr12	stataddr8
E	pktaddr11	pktaddr10	pktaddr9	pktaddr8	VSS	VSS	VSS	VSS	VDDram	VDDram	VDDram	VDDram	VSS	VSS	VSS	VSS
F	pktaddr15	pktaddr14	pktaddr13	pktaddr12	VDDram											
G	pktaddr19	pktaddr18	pktaddr17	pktaddr16	VDDram											
H	pktdata2	pktdata1	pktdata0	pktaddr20	VDDram											
J	pktdata6	pktdata5	pktdata4	pktdata3	VDDram											
K	pktdata10	pktdata9	pktdata8	pktdata7	VSS											
L	pktdata14	pktdata13	pktdata12	pktdata11	VSS											
M	pktdata18	pktdata17	pktdata16	pktdata15	VSS											
N	pktdata22	pktdata21	pktdata20	pktdata19	VSS											
P	pktdata26	pktdata25	pktdata24	pktdata23	VSS											
R	pktdata27	pktdata28	pktdata29	pktdata30	VSS											
T	pktdata31	pktdata32	pktdata33	pktdata34	VSS											
U	pktdata35	pktdata36	pktdata37	pktdata38	VSS											
V	pktdata39	pktdata40	pktdata41	pktdata42	VSS											
W	pktdata43	pktdata44	pktdata45	pktdata46	VDDram											
Y	pktdata47	pktdata48	pktdata49	pktdata50	VDDram											
AA	pktdata51	pktdata52	pktdata53	pktdata54	VDDram											
AB	pktdata55	pktdata56	pktdata57	pktdata58	VDD											
AC	pktdata59	pktdata60	pktdata61	pktdata62	VDD											
AD	osc25	pktdata63	VSSAF1	VDDAF1	VDDAF2											
AE	gtl_vref	bgr_res	VSSAF2	VSSAB	VDDAB											
AF	VSS	VSS	VSS	VSS	VSS											
AG	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDD	OS_3V	OS_3V	VSS	VSS	VSS	VSS
AH	OS_dat0	OS_dat4	OS_dat8	OS_dat12	OS_dat16	OS_dat20	OS_dat24	OS_dat28	OS_dat32	OS_dat36	OS_dat40	OS_dat44	OS_dat48	OS_dat51	OS_dat55	OS_dat62
AJ	OS_dat1	OS_dat5	OS_dat9	OS_dat13	OS_dat17	OS_dat21	OS_dat25	OS_dat29	OS_dat33	OS_dat37	OS_dat41	OS_dat45	OS_dat49	OS_dat52	OS_dat56	OS_dat61
AK	OS_dat2	OS_dat6	OS_dat10	OS_dat14	OS_dat18	OS_dat22	OS_dat26	OS_dat30	OS_dat34	OS_dat38	OS_dat42	OS_dat46	OS_dat50	OS_dat53	OS_dat57	OS_dat60
AL	OS_dat3	OS_dat7	OS_dat11	OS_dat15	OS_dat19	OS_dat23	OS_dat27	OS_dat31	OS_dat35	OS_dat39	OS_dat43	OS_dat47	VSSAB	OS_dat54	OS_dat58	OS_dat59

Figure 2.4 Ball Assignment Chart (Left Half— looking from top, through package)

17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
stataddr4	stataddr0	ES__data31	ES__data27	ES__data23	ES__data19	ES__data15	ES__data11	ES__data7	ES__data3	ES__par3	ES__addr6	ES__addr2	ES__clk	ES__ce#	**A**
stataddr3	ES__perr#	ES__data30	ES__data26	ES__data22	ES__data18	ES__data14	ES__data10	ES__data6	ES__data2	ES__par2	ES__addr5	ES__addr1	ES__wait	tx0_pa	**B**
stataddr2	ES__int#	ES__data29	ES__data25	ES__data21	ES__data17	ES__data13	ES__data9	ES__data5	ES__data1	ES__par1	ES__addr4	ES__addr0	ES__we#	tx0_par	**C**
stataddr1	sysreset#	ES__data28	ES__data24	ES__data20	ES__data16	ES__data12	ES__data8	ES__data4	ES__data0	ES__par0	ES__addr3	ES__oe#	N/C	rx0_err	**D**
VSS	VDD	VDD	VDD	VDDIO	VDDIO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	**E**
										VDD	VDD	VSS	VSS	VSS	**F**
										VDD	scan_en	test1	test0	rx0_par	**G**
										VDD	VDD	rx0_pa	rx0_val	rx0_eop	**H**
										VDD	VDD	rx0_enb#	txd_data0	txd_data1	**J**
										VDDIO	VDDIO	rx0_sop	rx0_data0	rx0_data1	**K**
										VDDIO	VDDIO	tx0_data2	tx0_data3	tx0_data4	**L**
										VSS	VSS	rx0_data2	rx0_data3	rx0_data4	**M**
										VSS	VSS	tx0_data5	tx0_data6	tx0_data7	**N**
										VSS	VSS	rx0_data5	rx0_data6	rx0_data7	**P**
										VSS	VSS	tx0_enb#	tx0_sop	tx0_eop	**R**
										VSS	VSS	VSS	VSS	nirefclk	**T**
										VDD	VDD	rx1_eop	rx1_val	rx1_pa	**U**
										VDD	VDD	tx1_data1	tx1_data0	rx1_enb	**V**
										VDD	VDD	rx1_data1	rx1_data0	rx1_sop	**W**
										VDD	VDD	tx1_data4	tx1_data3	tx1_data2	**Y**
										VDD	VDD	rx1_data4	rx1_data3	rx1_data2	**AA**
										VDD	VDD	tx1_data7	tx1_data6	tx1_data5	**AB**
										VSS	VSS	rx1_data7	rx1_data6	rx1_data5	**AC**
										VSS	VSS	tx1_eop	tx1_sop	tx1_enb	**AD**
										OS_3V	OS_3V	rx1_err	tx1_prty	rx1_prty	**AE**
										VSS	VSS	VSS	VSS	VSS	**AF**
VSS	VSS	VSS	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	**AG**
OS_pktid2	OS_pktid6	OS_pktid10	OS_pktid14	OS_pktid18	OS_pktid22	OS_pktid26	OS_trans3	OS_bsy0#	OS_bsy4#	OS_rq0#	OS_rq4#	OS_gnt0#	OS_gnt4#	OS_parity	**AH**
OS_pktid1	OS_pktid5	OS_pktid9	OS_pktid13	OS_pktid17	OS_pktid21	OS_pktid25	OS_trans2	VSSAB	OS_bsy3#	OS_bsy7#	OS_rq3#	OS_rq7#	OS_gnt3#	OS_gnt7#	**AJ**
OS_pktid0	OS_pktid4	OS_pktid8	OS_pktid12	OS_pktid16	OS_pktid20	OS_pktid24	OS_trans1	OS_trans5	OS_bsy2#	OS_bsy6#	OS_rq2#	OS_rq6#	OS_gnt2#	OS_gnt6#	**AK**
OS_dat63	OS_pktid3	OS_pktid7	OS_pktid11	OS_pktid15	OS_pktid19	OS_pktid23	OS_trans0	OS_trans4	OS_bsy1#	OS_bsy5#	OS_rq1#	OS_rq5#	OS_gnt1#	OS_gnt5#	**AL**

Figure 2.5 Ball Assignment Chart (Right Half— looking from top, through package)

2.2 Pin Signal Descriptions

The Serenade chip pins are grouped as follows:

- OptiStream Interface pins
- EdgeStream Interface pins
- SRAM Interface pins
- Network Interface pins
- Analog, power, ground, and utility pins

The following sections provide signal descriptions for each of these groups of pins.

2.2.1 OptiStream Interface Pin Signal Descriptions

This section provides a detailed description of the signals for each of the OptiStream Interface pins. For the location of these pins, see cells AH1 through AL31 on 12 and 13.

Signal Name	Type	Description
OS_Data[63:0]	GTL+ [In/Out]	An initiator uses these signals to communicate control and data to targets. These signals are driven by initiators and are inputs for targets. They are sampled on every rising edge of the phase and frequency locked, 100MHz internal clock. When the bus is idle, these signals are pulled up to the terminating voltage (V_T).
OS_Trans[5:0]	GTL+ [In/Out]	An initiator uses these signals to define the transaction occurring on the OptiStream Interface to the targets. These transactions are described in the OptiStream Interface Transactions section. These signals are driven by the initiators and are inputs to targets. They are sampled on every rising edge of the phase and frequency locked, 100MHz internal clock. When the bus is idle, these signals are pulled up to the terminating voltage (V_T).
OS_Pktid[26:0]	GTL+ [In/Out]	Each device in the system uses these signals to define a unique identity for each packet. To create this unique identity, the device encodes its identity on OS_Pktid[26:23] and encodes a packet sequence number on OS_Pktid[22:0]. The packet sequence number is the start address of the Packet Buffer assigned to store the packet in the local SRAM. These signals are driven by the initiator and are inputs to targets. They are sampled on every rising edge of the phase and frequency locked, 100MHz internal clock. When the bus is idle, these signals are pulled up to the terminating voltage (V_T).

Table 2.2 OptiStream Interface Pins

Signal Name	Type	Description
OS_Rq[7:0]#	GTL+ [In/Out]	An initiator uses these active low signals to request use of the OptiStream Interface from the master. Each device uses the value in its device ID register to determine which OS_Rq# signal to drive as an output. For instance, if a device ID register is programmed to 01H, the device drives OS_Rq[1]# as an output and floats the other OS_Rq# signals, which are pulled up to the terminating voltage (V_T). These signals are driven active on the rising edge of the clock as soon as an initiator has a transaction pending. The OS_Rq# signal stays active as long as there are transactions pending that require use of the OptiStream Interface. When there are no additional transactions pending that require use of the OptiStream Interface, the OS_Rq# signal is driven inactive when the final transfer is initiated after receiving the OS_Gnt# signal. These signals are driven by the initiators and are inputs to the master. They are sampled on every rising edge of the phase and frequency locked, 100MHz internal clock.
OS_Gnt[7:0]#	GTL+ [In/Out]	The master uses these active low signals to respond to OS_Rq# signals from initiators. Each device uses the value in its device ID register to determine which OS_Gnt# signal to monitor as an input. For instance, if the device ID register is programmed to 02H, the device monitors OS_Gnt[2]# as an input and ignores the other OS_Gnt# signals. These signals are driven active of the rising edge of the clock by the master. This signal communicates to an initiator that the next cycle has been reserved for its use. An initiator checks that its OS_Rq# and OS_Gnt# signals are active before starting a transaction on the OptiStream Interface. The OS_Gnt# signal for a particular initiator can continue to be active for consecutive cycles if no other OS_Rq# signals are active and the corresponding OS_Rq# signal stays active. If other OS_Rq# signals are active, a OS_Gnt# signal is driven inactive on the rising edge of the internal clock one cycle after being driven active. These signals are outputs from the master and are inputs to the initiators. They are sampled on every rising edge of the phase and frequency locked, 100MHz internal clock.
OS_Busy[7:0]#	GTL+ [In/Out]	Each target uses these signals to communicate to initiators that the target is unable to accept data transfer transactions. If the target cannot successfully latch the transaction, it drives OS_Busy# low on the rising edge of the clock. If the target can accept the transaction, the OS_Busy# signal stays at the terminating voltage (V_T). The initiator samples the OS_Busy# in the cycle before the transaction will occur to determine if it will successfully complete.
OS_Parity	GTL+ [In/Out]	The Initiator generates this signal, and the targets check it. This signal is used for OptiStream Interface error detection. It can be programmed to support odd or even parity. If an error occurs, a target registers the error and generates an interrupt to the system via the OptiStream Interface Interrupt register.

Table 2.2 OptiStream Interface Pins (continued)

2.2.2 EdgeStream Interface Pin Signal Descriptions

This section provides a detailed description of the signals for each of the EdgeStream interface pins. For the location of these pins, see cells A18 through D31 on 12 and 13.

Signal Name	Type	Description
ES_Addr[6:0]	Std TTL [Input]	These signals provide 7-bit, non-multiplexed address input signals to address the Serenade chip registers. Normally, ES_Addr[6:0] should be tied to address pins [8:2] of a 32-bit processor bus. There are two classes of register accesses, direct and indirect. The EdgeStream Interface registers are addressed directly. The registers for the rest of the chip are accessed using an indirect address register (Control Bus Address Register) and an indirect data register (Control Bus Data Register).
ES_Data[31:0]	24 ma [In/Out]	These signals provide 32-bit, non-multiplexed data signals, used by the external CPU to read/write configuration, status, control, and packet data from or to the Serenade chip. These signals are placed in a high impedance state when ES_CE# or ES_OE# signals are de-asserted.
ES_Clock	Std TTL [Input]	The Serenade chip uses this clock signal to allow burst read/write operations from the packet read and write FIFOs. This clock allows use of a single register access and the subsequent burst read /write of the FIFOs on every leading edge of the clock.
ES_CE# ES_WE# ES_OE#	Std TTL [Input]	The external CPU uses the Chip Enable, Write Enable, and Output Enable signals to control the read/write of data from and to the Serenade chip. • A write to the Serenade chip is accomplished by asserting the chip enable (ES_CE#) and the write enable (ES_WE#) signals while negating the output enable signal (ES_OE#). The pattern on the ES_Data[31:0] pins is then written into the location specified on the address pins (ES_Addr[6:0]) and latched at the location by driving ES_WE# high. • A read from the Serenade chip is accomplished by asserting the chip enable (ES_CE#) and output enable (ES_OE#) while negating the write enable (ES_WE#) signals. The contents of the register specified by the address pins appears on the data pins. The ES_Data[31:0] pins are placed in a high impedance state when the ES_CE# signal is negated. If wait states are generated by the Serenade chip during the read/write access, the CPU (or any accessing agent) must hold the ES_CE#, ES_WE#, and ES_OE# signal levels constant until the wait is negated. These are active-low signals.
ES_WAIT	24 ma [In/Out]	The Serenade chip uses this signal to communicate to an external processor that the register access being processed requires additional cycles to complete. The ES_WAIT signal is active-high.
ES_PAR[3:0]	24 ma [In/Out]	This parity signal generates a parity bit computed over each byte of the ES_Data[31:0] signals during valid data phases, if the en_prty bit in the ES_ Control register is set (the default after a reset is parity off). The polarity depends on the odd_prty bit in the ES_ Control register. As an input, this line is sampled when the Serenade chip is placed in a write cycle and driven when the Serenade chip is executing a read cycle. These signals are placed in a high impedance state when the ES_CE# signal is de-asserted or when the ES_OE# signal is high.

Table 2.3 EdgeStream Interface Pins

Signal Name	Type	Description
ES_INT#	24 ma [Emulated Open Drain]	The Serenade chip asserts this interrupt request signal to indicate that one or more interrupt events have occurred and that the corresponding bits in the Interrupt Register have been set. The Serenade chip continues to assert this signal until all interrupt flags are cleared in the respective registers. This signal drives low when an interrupting event occurs. The output emulates an open-drain circuit. When transitioning from low to high (INT cleared), it drives high for a short period before going to a high impedance. This line is not internally pulled up so that it can be OR-tied with INT# pins from multiple Serenade devices. An external pull-up resistor is required. This is an active low signal.
ES_PERR#	24 ma [Tri-stated Out]	The Serenade chip asserts this Parity Error signal during a write cycle to indicate that a parity error was detected on the ES_Data[31:0] signals. If an error is detected, the write operation is either aborted or goes through anyway, depending on the pewrt_inhibit bit in ES_ Control register (this bit defaults to “write through” after reset). This is an active low signal.
SysReset#	Std TTL [Input]	This System Reset is asserted to perform a hardware reset of the Serenade chip. The SysReset# input uses a Schmidt trigger. This is an active low signal.

Table 2.3 EdgeStream Interface Pins (continued)

2.2.3 SRAM Interface Pin Signal Descriptions

This section provides a detailed description of the signals for each of the SRAM Interface pins. For pin location, see cells A1 through AD4 and A6 through D18 on 12 and 13.

Signal Name	Type	Description
PktClockOut, StatusClockOut	24 ma [Output]	These signals provide the SRAM clock. They are 100MHz output from the Serenade chip to the SRAM (data and status respectively). They are used to register the address, data, and chip enable inputs on the rising edge. All synchronous outputs meet setup and hold times around the clock’s rising edge.
PktClockIn, StatusClockIn	24 ma [Input]	These clock input signals are connected to the clock output signals. They are available to allow the system designer to match the data signal traces to the clock trace to minimize skew on memory read operations.
PacketAddr[20:0]	24 ma [Output]	These signals provide 21-bit, non-multiplexed address signals, which the Serenade chip outputs to address the SRAM. Since the Serenade chip does not access bytes on the data side of the SRAM interface, the “byte access” signals on the SRAM must always be enabled for full access. In conjunction with the eight independent chip-enable signals, these address signals allow the Serenade chip to logically address a maximum of 8 Mbytes of memory for packet data while using 256K x 32 SRAMs. For information on the electrical restrictions that limit the amount of RAM that can be connected, see Section 2.3.5, “External SRAM,” on page 23. **Note:** The Synchronous Load (LD#) signal on the SRAM, used to clock in a new address, is permanently enabled when used with the Serenade chip.
PacketData[63:0]	24 ma [In/Out]	These signals provide 64-bit, non-multiplexed Packet Data signals used by the Serenade chip to read and write packet data from and to the SRAM.

Table 2.4 SRAM Bus Signal Pins

Signal Name	Type	Description
PacketCE[3:0]#	24 ma [Output]	The Serenade chip uses these data buffer chip enable signals to enable the reading and writing of data. To maximize memory cycle time and minimize decode time, four individual PacketCE# signals are available. The decode space enabled by each PacketCE# signal is controlled by setting appropriate bits in the RAM Parameter Register.
PacketR/W# /PacketOE#	24 ma [Output]	This data RAM read/write/output enable signal has a dual function depending on the RAM type specified in the Packet Buffer RAM Control Register. • In RAM mode, this line serves as a Read/Write# signal. It signifies a read cycle when it is high and a write cycle when it drives low.
PacketWEe#	24 ma [Output]	This packet RAM write enable signal sends a write command (when low) to the packet data SRAM. This signal is asserted in the same cycle as PacketR/W#/ PacketOE# and PacketAddr[20:0] signals, described above. One pin is used for all 64-bit wide RAM devices.
StatusAddr[20:0]	24 ma [Output]	These signals provide 21 non-multiplexed address signals, which the Serenade chip outputs to addresses the Status Buffer. These signals are placed in a high impedance state when the corresponding StatusCE[n]# signals are de-asserted. **Note:** The Synchronous Load (LD#) signal on the SRAM, used to clock in a new address, is permanently asserted when used with the Serenade chip.
StatusData [15:0]	24 ma [In/Out]	These signals provide non-multiplexed bidirectional packet status signals, which the Serenade chip uses to read and write packet status to the Packet Buffer.
StatusCE[3:0]#	24 ma [Output]	The Serenade chip uses these status buffer chip enable signals to enable reading or writing of status. To minimize decode time, four StatusCE# signals are available. The decode space enabled by each StatusCE# signal is controlled by setting appropriate bits in the Packet Buffer RAM Control Register.
StatusBW#	24 ma [Output]	The StatusBW# signal is asserted on the same cycle as the StatusAddr[20:0].
StatusR/W# /StatusOE#	24 ma [Output]	This status buffer read/write/output enable signal has a dual function depending on the RAM type specified in the Packet Buffer RAM Control Register. • In RAM mode, this line serves as a Read/Write# signal. It signifies a read cycle when it is high and a write cycle when it drives low.

Table 2.4 SRAM Bus Signal Pins (continued)

2.2.4 Network Interface Pin Signal Descriptions

This section provides a detailed description of the signals for each of the Network Interface pins. For pin location, see cells B29 through AE31 on 12 and 13.

Signal Name	Type	Description
POS-Phy Interface Pins		
NIRefClock	8 ma [Output]	This Network Interface reference clock is a continuous clock that provides the timing reference for the RXn_Data[7:0] and TX[1:0] Data[7:0] signals. This clock's frequency is 50 MHz.
TX0_Enb# for np0 TX1_Enb# for np1	8 ma [Output]	OC-3c port Transmit Data Write Enable: This active-low signal indicates the data transmit activity on TXn_Data[7:0] bus.

Table 2.5 Network Interface Pins

Signal Name	Type	Description (continued)
TX0_PA for np0 TX1_PA for np1	Std TTL [Input]	OC-3c port Direct Transmit Packet Available: This active-high signal indicates that a programmed number of data bytes are available to transfer in the Transmit FIFO when it transitions to high. Once high, it indicates that the Transmit FIFO is not (almost) full.
TX0_SOP for np0 TX1_SOP for np1	8 ma [Output]	OC-3c port Transmit Start of Packet: This active-high signal indicates the first byte of a packet on TXn_Data[7:0] bus when asserted with TXn_Enb# at the rising edge of NIRefClock.
TX0_EOP for np0 TX1_EOP for np1	8 ma [Output]	OC-3c port Transmit End of Packet: This active-high signal marks the end of a packet on TXn_Data[7:0] bus. The last byte of the packet is on the bus when this pin and TXn_Enb# are both asserted at the rising edge of NIRefClock.
TX0_Data [7:0] for np0 TX1_Data[7:0] for np1	8 ma [Output]	OC-3c port Transmit Packet Data Bus (8-bit): This bus carries the packet bytes that are output to the external optical PHY. The output is valid when TXn_Enb# is also asserted at the rising edge of NIRefClock.
TX0_Par for np0 TX1_Par for np1	8 ma [Output]	OC-3c port Transmit Packet Data Parity: This bit carries the parity (odd or even) for the 8-bit TXn_Data bus during the data packet transmission, if parity generation is enabled.
RX0_Enb# for np0 RX1_Enb# for np1	8 ma [Output]	OC-3c port Read Data Enable: This active-low signal initiates the input data transfer on RXn_Data [7:0] bus.
RX0_Val for np0 RX1_Val for np1	Std TTL [Input]	OC-3c port Receive Data Valid: This active-high signal indicates the validity of the receive data signals. When RXn_Val is high and RXn_Enb# is low, the receive signals (RXn_Data, RXn_SOP, RXn_EOP and RXn_Err) are valid.
RX0_PA for np0 RX1_PA for np1	Std TTL [Input]	OC-3c port Receive Packet Data Available: This active-high signal indicates that either some programmable amount of data or an end of packet is available in the Receive FIFO in the PHY.
RX0_SOP for np0 RX1_SOP for np1	Std TTL [Input]	OC-3c port Receive Start of Packet: This active-high signal marks the first byte of a packet transfer on RXn_Data[7:0] bus, when asserted simultaneously with RXn_Enb# at the rising edge of NIRefClock.
RX0_EOP for np0 RX1_EOP for np1	Std TTL [Input]	OC-3c port Receive End of Packet: This active-high signal marks the end of packet on the RDAT[7:0] bus, when asserted simultaneously with RXn_Enb# at the rising edge of NIRefClock.
RX0_Data [7:0] for np0 RX1_Data[7:0] for np1	Std TTL [Input]	OC-3c port Receive Packet Data Bus (8-bit): This bus carries the packet bytes that are read from the FIFO in the external PHY device. The input is valid when RXn_Enb# is also asserted at the rising edge of NIRefClock.
RX0_Par for np0 RX1_Par for np1	Std TTL [Input]	OC-3c port Receive Packet Data Parity: This bit reads the parity (odd or even) for the 8-bit RXn_Data during the data packet reception, if parity check is enabled.
RX0_Err for np0 RX1_Err for np1	Std TTL [Input]	OC-3c port Receive Error Indicator: The PHY device uses this active-high signal to indicate that the current packet is aborted and should be discarded. It can be asserted only during the last byte transfer of the packet.

Table 2.5 Network Interface Pins (continued)

2.2.5 Analog, Power, Ground, and Utility Pin Signal Descriptions

This section provides a detailed description of the signals for each of these pins.

Signal Name	Type	Description
Osc25	Analog [Input]	This external reference clock provides the reference timing for the internal clock synthesizer circuit of Serenade chip. This 25MHz clock is used to derive the internal clocks. The internally-generated100MHz clock is kept in phase lock with the 25MHz clock input to ensure system synchronization in a application with multiple Serenade devices. This is achieved by the following means: • sharing of the same Osc25 clock source between all Serenade devices involved. • careful board layout to achieve matching traces.
BGR_Res	Analog	The band gap reference pin requires a 12.4KΩ 1% resistor to be attached between it and the (analog) ground to insure proper operation of internal current sources.
GTL_Vref	Analog	This GTL+ Receiver Reference Voltage pin must have nominal (2/3 * Vterm) voltage applied to it for the OptiStream Interface receivers to operate properly.
Testmode	Std TTL [Input]	This scan test mode pin must be grounded for the normal mode of operation.
Scan_En	Std TTL [Input]	This scan shift enable pin must be grounded for the normal mode of operation.
Test[1:0]	Std TTL [Input]	These test mode selection pins must both be grounded for the normal mode of operation.
VDDAF1, VDDAF2	Pwr	This frequency synthesizer power pad must have 3.3V power applied to it to drive internal analog circuitry. A clean, filtered 3.3V should be used.
VDDAB	Pwr	This band gap reference power pad must have 3.3V power applied to it to drive internal analog circuitry. A clean, filtered 3.3V should be used.
VSSAF1, VSSAF2	Gnd	This frequency synthesizer ground pad is dedicated to the internal analog circuitry.
VSSAB	Gnd	This band gap reference ground pad is dedicated to the internal analog circuitry.
VDDOS_3V	Pwr	These OptiStream Interface 3.3V power pads are exclusively for OptiStream Interface transceivers. They should be combined together and shorted to the board 3.3V VDD at one place only.
VDDram	Pwr	These RAM 3.3V power pads are exclusively for SRAM Interface transceivers. They should be combined together and shorted to the board 3.3V VDD at one place only.
VDDIO	Pwr	These I/O VDD power pads exclusively for the EdgeStream Interface transceivers. They should be combined together and shorted to the board 3.3V VDD at one place only.
VDD	Pwr	These VDD 2.5V power pins drive the core logic.
VSS	Gnd	These ground pins are for the digital logic circuits.

Table 2.6 Analog, Power, Ground, and Utility Signal Pins

2.3 External Components

This section describes the characteristics and restrictions that apply to the Serenade chip's external components. It covers the following topics:

- External OptiStream Interface routing

- External reference clock
- Band gap reference
- GTL+ receiver reference
- External SRAM

2.3.1 External OptiStream Bus Routing

Up to four Serenade devices can be tied to the OptiStream bus to form a system of up to eight OC-3c ports. Due to the high speed nature of this bus, some physical restrictions apply.

- The wire length for the OptiStream Interface cannot exceed 8 inches.
- Each OptiStream Interface signal line must be terminated to 1.5V, with a maximum trace length of 8 inches.
- The circuit board wires for OptiStream Interface should run directly underneath the chips without adding any significant stub length.
- The maximum pitch between the devices is two inches. The distance from the edge device to the terminator must be one inch or less. A straight line throughout the trace run is desirable.

Figure 2.6 illustrates these requirements:

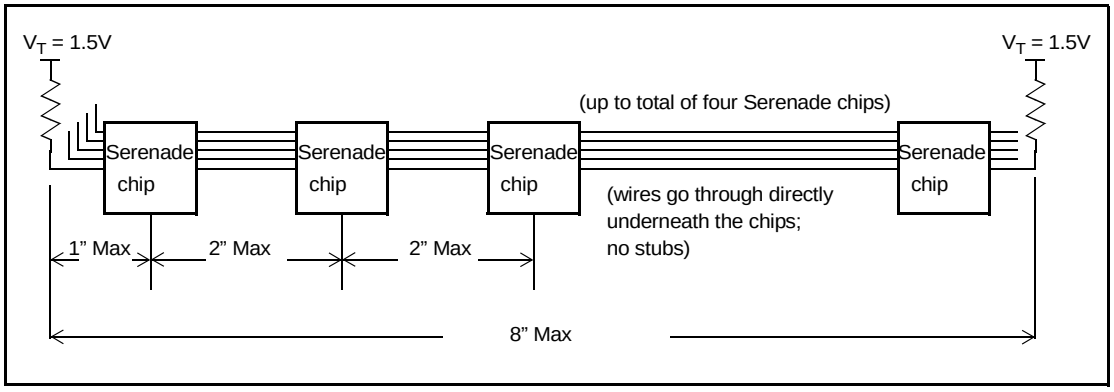

Figure 2.6 OptiStream Interface Wiring

2.3.2 External Reference Clock

The Serenade chip uses one external 25MHz reference clock (Osc25) to generate all other clocks necessary to run the chip, except the ES_Clock (which is supplied from the CPU system, see Table 2.3 on page 16).

The external reference clock may be derived from a discrete oscillator, or from a precision PLL frequency generator. However, it should be free of ripple noise and jitter. The Serenade chip's Osc25 pin requires 2.5V CMOS swing instead of 3.3V. If a 5 or 3.3V source is used, perform the level translation before connecting the source to the Serenade chip's Osc25 pin.

The Osc25 pin is in location AD1 in Figure 2.4 on page 12. For a description of the Osc25 pin see Table 2.6 on page 20.

2.3.3 Band Gap Reference

A 1% precision resistor provides a reference point for the internal band-gap reference. Place a 12.4KΩ 1% resistor between the BGR_Res pin and the analog ground as illustrated in Figure 2.7.

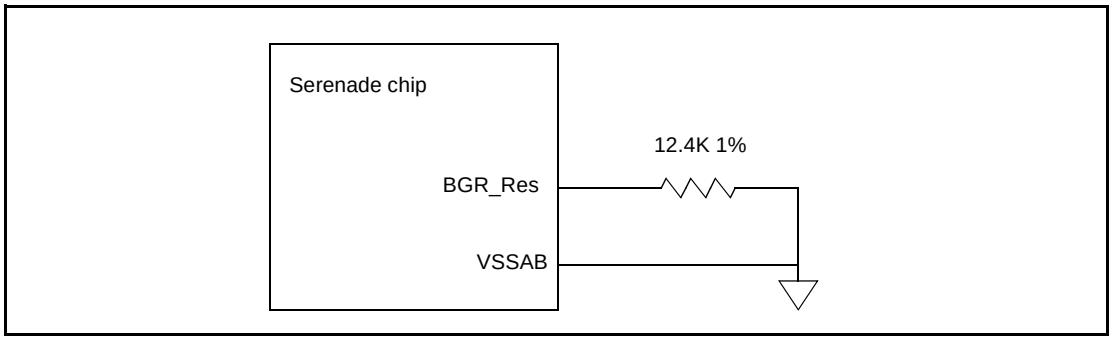

Figure 2.7 Band Gap Reference Resistor

The BGR_Res pin is in location AE2 in Figure 2.4 on page 12. For a description of the BGR_Res pin, see Table 2.6 on page 20.

2.3.4 GTL+ Receiver Reference

To maximize the timing margin on the OptiStream Interface, the receiver is biased at a level where transitions are most quickly detected. To set the appropriate bias level, the GTL_Vref pin should be driven to 2/3 of V_T, the OptiStream Interface termination voltage. This is nomi-

nally 1.0V. Figure 2.8 illustrates this requirement.

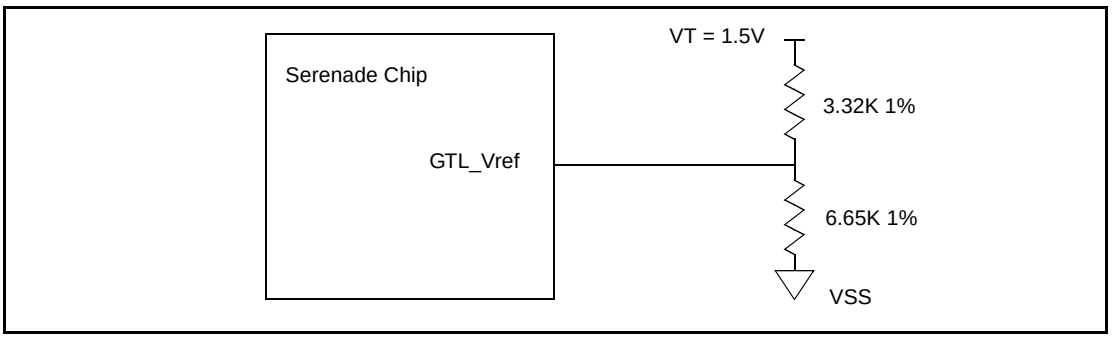

Figure 2.8 GTL+ Receiver Reference Voltage

The GTL_Vref pin is in location AE1 in Figure 2.4 on page 12. For a description of the GTL_Vref pin, see Table 2.6 on page 20.

2.3.5 External SRAM

The Serenade chip is designed to work with pipelined (recommended) ZBT SRAM for the packet data buffer and the status buffer. It can logically address up to four banks of data RAM devices, up to a 21-bit address range per device, with a maximum addressable RAM capacity of 64MB. In reality, the capacitive loading and RAM availability limit the configuration. Specifically, the Serenade chip can directly drive up to eight packet data RAM chips in various configurations, or more if the RAM clock can be buffered-phase locked externally.

Table 2.7 illustrates some of the possible combinations for the memory configurations. In this table:

- A *bank* is a set of RAM chips controlled by the same Pkt_CEx# pin. Since the width of the Packet Data bus is fixed at 64-bit (8-byte), one bank of 256K x 32 bit x 2 chips SRAM represents 256K x 8 = 2MBytes of storage space. Four of these rows comprise the capacity of eight MBytes.
- The Minimum Chip Count column indicates how many SRAM chips are required to implement a “single bank” RAM system (including the status SRAM).
- The Maximum Chip Count column indicates the RAM chip count with maximum allowed number of banks.

Data SRAM Device	Buffer Size	Data SRAM Chip Count	Status SRAM Chip Count	Max.[a] number of banks	Min. Chip Count	Max. Chip Count
128K x 16 e.g., Micron MT55L128L18	1MB x row (2MB Max.)	4 x row	1 x row	2	4 + 1	8 + 2
64K x 32 e.g., Micron MT55L64L32	512KB x row (2MB Max.)	2 x row	1 x row (use 64K x 16)	4	2 + 1	8 + 4
256K x 16 e.g., Micron MT55L256L18	2MB x row (4MB Max.)	4 x row	1 x row	2	4 + 1	8 + 2
128K x 32 e.g., Micron MT55L128L32	1MB x row (4MB Max.)	2 x row	1 x row (use 128K x 16)	4	2 + 1	8 + 4
256K x 32	2M x bank (8MB Max.)	2 x bank	1 x bank (use 256K x 16)	4	2 + 1	8 + 2

Table 2.7 Recommended RAM Configurations

a. Maximum number of banks based on the four-chip loading limit specified below. The device allows up to eight rows of RAMs to be attached, but careful electrical considerations must be made to go beyond this limit.

As indicated in Table 2.7, an independent set of data RAM (64-bit wide) and status RAM (16-bit) is required. For the data port, depending on whether the RAM is 16-bit wide or 32-bit wide, four or two chips per row are needed. Each Serenade device can logically support up to eight rows, but the driver electrical properties limit the number of RAMs directly attached to the bus to eight as shown in the table's Data SRAM Chip Count column.

Note: In general, for a given size RAM, use a 32-bit device to limit the RAM chip count; use a 16-bit device to maximize the buffer capacity.

The SRAM interface transceiver pads are designed with following loading assumptions:

RAM Control Pin Input Capacitance:	4pF Max
SRAM Data Pin Input Capacitance:	4pF Max
SRAM Address Pin Input Capacitance:	3.5pF Max
Maximum Number of Data SRAMs:	8
PC Board Trace Capacitance Allowance:	3pF / bank Max
Maximum Loading on Address Pins:	34pF Max
Maximum Loading on Data Pins:	23pF Max

The Serenade chip can connect more SRAM devices than described above. For example, sixteen 128K x 32 RAMs instead of eight 256K x 32 can be used to get an eight MByte capacity by using PacketAddr[20] as one of the chip enable signals (see Table 2.4 on page 17 for a description of PacketAddr[20]). Since such applications require heavier electrical loading, careful electrical and timing analysis must be followed to insure its proper operation.

The type and size of the RAM chips being using in the Packet Buffer RAM Control register must be programmed. Figure 2.9 illustrates how to program this type of configuration:

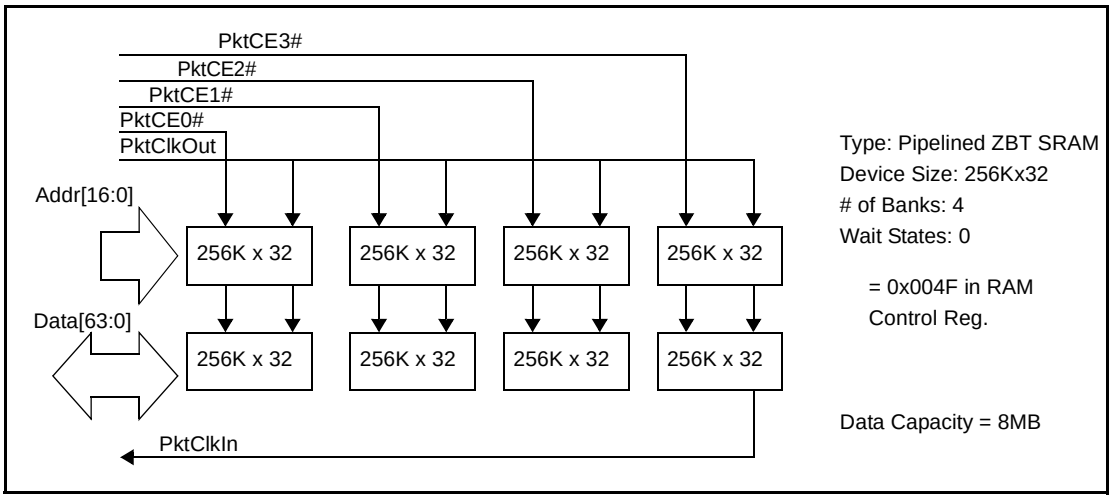

Figure 2.9 RAM Configuration Example

Serenade is designed to work with SRAMs of various types rated at 100MHz or faster. To accommodate cost sensitive applications, the following various programmable parameters are provided to interface to slower RAMs. Contact Entridia for the most current SRAM support information:

Device Types
Pipelined ZBT SRAM is currently recommended for optimal performance for Serenade:

00 Reserved
01 Reserved
10 Reserved
11 Pipeline mode ZBT SRAM

Device Address Space
The number of the column address the specified RAM chip has. This defines the size of each RAM bank. Each column is 8-bytes wide (packet) and 2-bytes wide (status).

000 15-bit -- 32K columns
001 16-bit -- 64K columns
010 17-bit -- 128K columns
011 18-bit -- 256K columns
100 19-bit -- 512K columns
101 20-bit -- 1M columns
110 21-bit -- 2M columns

Number of Memory Banks

The number of banks of packet/status RAMs. Each bank is selected by one of the four chip enable (packetCE[3:0]#, statusCE[3:0]#) pins.

0000	Reserved
0001	1 bank
0010	2 banks
0011	3banks
0100	4 banks
0101 - 1111	Reserved

Chip Enable Setup Time (CSS)

When PacketCE[3:0]#/StatusCE[3:0]# and other control pins are negated for a while, some RAM chips enter a sleep mode. They may take some extra time before they wake up, though such timings are often not specified. Serenade accommodates such RAM chips by inserting a clock cycle delay between PacketCE[3:0]#/StatusCE[3:0]# assertion to setting of all other address/data/control signals.

0 No extra chip enable setup time is set. PacketCE[3:0]#/StatusCE[3:0]#, address, control and/or data are coincident.
1 One clock delay is inserted between PacketCE[3:0]#/StatusCE[3:0]# assertion from the rest of the control signals.

The RAM interface assumes that a given application uses the same size RAM for data and status storage. For example, if 128K (x16 or x32bit) devices are used for the packet data SRAM, use a 128K x 16 device for the status SRAM.

Actual wiring of RAM interface pins to the RAM devices depends on the type and configuration of the RAM device. Table 2.8 shows wiring examples for cases using RAM using the popular pin-out from those devices by Micron Technology, IDT, and Motorola.

Serenade Chip Pin-Out	RAM	
Both Status and Data RAMs		
	$\overline{LD}$ = VSS LBO = VDD CKE = VSS CE2 = VDD CE2 = VSS $\overline{OE}$ = VSS ZZ = VSS	
Status RAMs		
StatusClockOut	CLK	

Table 2.8 Device to RAM Wiring Chart

Serenade Chip Pin-Out	RAM	
StatusClockIn	(Clock return from the end of the RAM array)	
StatusCE#	CE	
StatusR/W# / StatusOE#	R/$\overline{W}$	
StatusWE#		
	$\overline{WE}$ = VSS	
	$\overline{OE}$ = VSS	
StatusAddr[20:0]	SA, SA1, SA0	
StatusData[7:0] StatusData[15:8]	DQa [7:0] DQb[7:0]	
Packet Data RAMs		
PacketClockOut	CLK	
PacketClockIn	(Clock return from the end of the RAM array)	
PacketCE#	CE	
PacketR/W# / PacketOE#	R/$\overline{W}$	
PacketWE#		
	$\overline{WE}$ = VSS	
	$\overline{OE}$ = VSS	
PacketAddr[20:0]	SA, SA1, SA0	
PacketData[63:32] PacketData[31:0]	DQa, DQb, DQc, DQd DQa, DQb, DQc, DQd	

Table 2.8 Device to RAM Wiring Chart (continued)

Due to the large capacitive load it represents, the board layout of the RAM array must use a thick trace to allow for a relatively large driving current for each address and data pin, and must have an ample ground and power plane to insure proper de-coupling and minimize the ground bounce potential.

An external clock distributor chip may be used to drive more RAM chips, as shown in Figure 2.10. The Data RAM clock output (PktClockOut) pin has the heaviest load at the highest duty cycle. If that pin can be buffered effectively, the number of RAMs can be doubled. However, take care to critically analyze the timing margin when designing a system in this way. In this configuration, it is estimated that up to 16 chips can be driven, bringing the total capacity to 16MB, using 256K x 32 RAM.

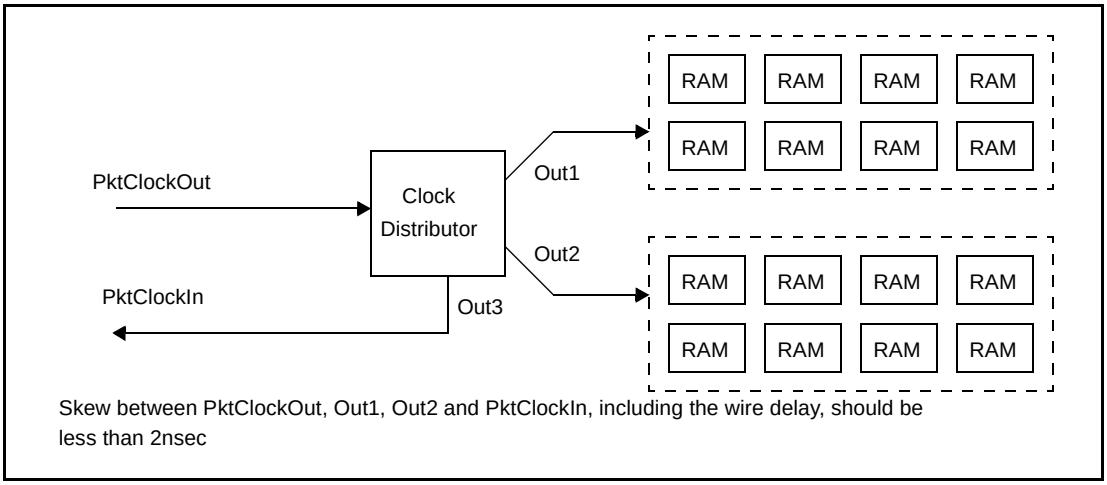

Figure 2.10 External RAM Clock Buffering

Chapter 3 System Interface Operation

This chapter describes the electrical characteristics and timing specifications for the Serenade chip.

3.1 Electrical Characteristics

This section describes the following electrical characteristics of the Serenade chip:

- The absolute maximum ratings
- Power sequencing for power-up and reset
- D.C. operating characteristics
- I/O pin types and electrical characteristics

3.1.1 Absolute Maximum Ratings

The absolute maximum ratings for the Serenade chip are as follows:

Storage Temperature	-55°C to +125C°
Operating Power Supply Voltage (VDD pin)	3.6 V
Input Voltage with Respect to Ground	-0.5V to 5.5V
ESD Immunity	2.0 KV human model

3.1.2 Power Sequencing

The 2.5 V power supply should always be lower than the 3.3 V power supply, even at power-up. For a proper power-up reset, the SysReset# signal must be low until all power-supply voltages reach at least to the lowest “normal” range. Figure 3.1 illustrates the power supply rise curves and the SysReset# signal.

Note: The clock signal Osc25 must be within specified tolerance before the 2.5 V and 3.3 V power supplies reach normal operating range. Thereafter, SysReset# must remain asserted until the power supplies have stabilized for a minimum of 1 millisecond. Serenade requires a maximum of 10 microseconds after SysReset# is negated to complete the internal initialization phase. After initialization is complete all generated clocks will be stable and within specified tolerance.

For more information on the SysReset# signal, see Table 2.3 on page 16.

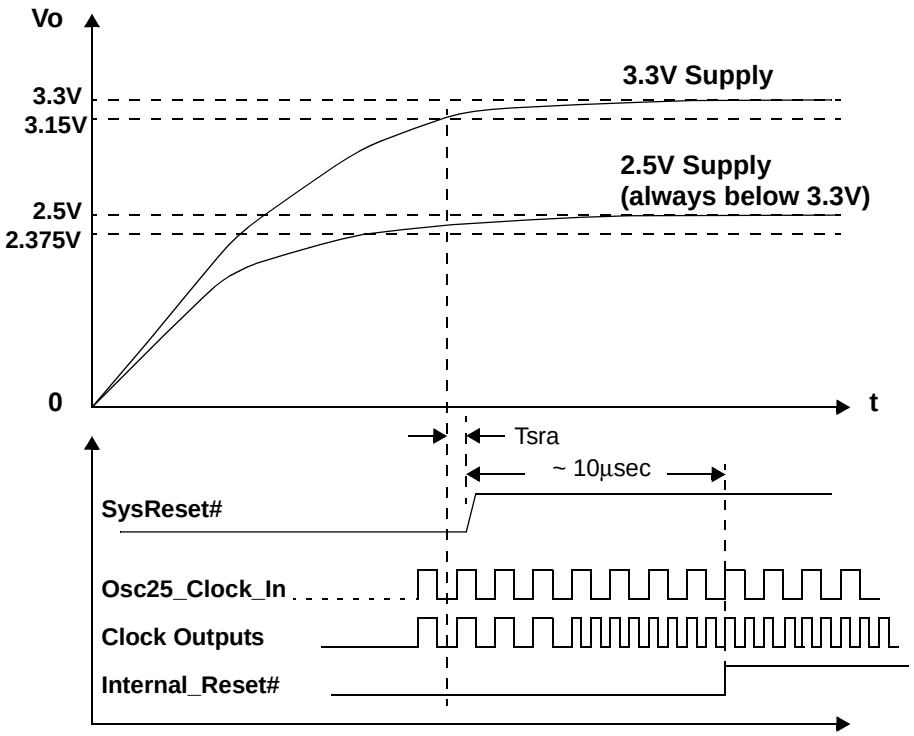

Figure 3.1 Power Supply Rise Curves and System Reset

3.1.3 D.C. Operating Characteristics

Table 3.1 provides a detailed description of the D.C. operating characteristics.

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Condition/Comment
Ta	Operating Ambient Temperature	0		70	°C	
Vdd	Operating Supply Voltages:					
	VDD	2.375	2.5	2.625	V	±5%
	IOVDD	3.15	3.3	3.45	V	
	RAMVDD	3.15	3.3	3.45	V	
	MXB3V	3.15	3.3	3.45	V	
	VDDAF1, 2	3.15	3.3	3.45	V	
	VDDAB	3.15	3.3	3.45	V	
Idd	VDD current[a]			TBD	mA	All outputs high-Z, All inputs negated, osc25 = 25MHz @All xVDD = 3.3 V / 2.5 V
	IOVDD+RAMVDD+MXB3V			TBD	mA	
	VDDAF1+VDDAF2+VDDAB			TBD	mA	

Table 3.1 D.C. Operating Characteristics

Pd	Maximum Power Dissipation[b]		8.5	Watt	All outputs active, All inputs active, osc25 = 25MHz @All xVDD at maximum
Iil	Input Leakage Current (All pins w/o pull-ups)	-10	+10	µA	-0.0V ≤ Vi ≤ VDD
Vi(max) Vi(min)	Max. operating input voltage Min. operating input voltage	 0	5.0 3.6 	V V V	“5V tolerant” pins Non-5V tolerant & analog pins all pins
Vih(Osc25) Vil(Osc25)	Input high voltage for Osc25 Input low voltage for Osc25	1.6	 0.9	V V	Osc25 clock input is at 2.5V logic swing.
Vih/Vil Ioh/Iol VHyst	Various I/O parameters (except for Osc25 pin above)				See Table 3.2
Vbgr	Band Gap Reference Voltage	1.23	1.25 1.26	V	At BGR_Res pin, with 12.4KΩ to ground attached
V_T	OptiStream Bus Termination Voltage	1.35	1.5 1.65	V	

Table 3.1 D.C. Operating Characteristics (continued)

a. Total current through all VDD pins at the specified condition.
b. The package alone is not expected to dissipate this much heat. Heatsink attachment and forced air cooling is required.

3.1.4 I/O Pin Types and Electrical Characteristics

Table 3.2 shows the I/O pin types and electrical characteristics of the Serenade chip:

Type	Dir.	V_{Hyst} (min)	V_{ih} / V_{il} (min) (max)	Internal Pullup	I_{oh}	I_{ol}	5V Tolrnt	Tri-State	C_{load}
low drive	I/O	no	0.65/0.35 VDD	no	-8.0mA @Vo=2.4V	8.0mA @Vo=0.4V	yes	yes	30pF
high drive	I/O	no	0.65/0.35 VDD	no	-24mA @Vo=2.4V	24mA @Vo=0.4V	yes	yes	
input only	I	no	0.65/0.35 VDD	no	-	-	yes	n/a	n/a
hysterisis input	I	1V	2.15V/ 1.05V	no	-	-	yes	n/a	n/a
GTL open drain	I/O	no	1.05/0.95	no	(Open Drain)	40mA @Vo=0.5V	no	yes	
analog	-	n/a	n/a	no	n/a	n/a	no	n/a	

Table 3.2 I/O Pin Types and Electrical Characteristics

3.2 External Timing Specification

Refer to the applicable sections in the Serenade Data Book for details on timings for the EdgeStream, Network, OptiStream, and SRAM interfaces.

Chapter 4 Programming Guide

This part of the document describes the function, interface, and implementation of the configuration and management software for the Serenade chip. The software components and interfaces described here are defined using WindRiver Corporation's VxWorks Real-Time Operating System (RTOS).

The control software for the Serenade chip consists of the following major components:

The Serenade device driver: This driver constitutes the low-level software interface to the programmable functions of the Serenade device. This component consists of an RTOS-dependent sublayer and a Serenade device-dependent sublayer.

The Serenade service programming interface: This component consists of a high-level library of C functions that presents an abstraction layer built on top of the facilities provided by the RTOS device driver.

4.1 Theory of Operation

Refer to the Serenade Data Book for complete details on the theory of operation for programming the Serenade chip. Included in the Data Book is specific information for the following areas of operation.

- Serenade Device Configuration
- OptiStream Interface Operation
  - OptiStream Interface Physical Characteristics
  - Inter-Serenade Packet Transfer
  - External Route / Filter Table Support
  - Multicast Transaction Handling
- OptiStream Interface Chip ID Assignment
  - Internal OptiStream Transactions
  - Transaction Flow Management
  - OptiStream Bus Arbitration Protocol
  - GTL Driver Slew Rate
  - OptiStream Port Transactions
  - External Scheduler Support

- Packet Forwarding Process using External Scheduler
- Inter-chip Data Transfer Prioritization using External Scheduler
- Physical Requirements for External Units
- OptiStream Transactions to support External Scheduler

- EdgeStream Interface Operation
  - Accessing the Serenade chip
  - EdgeStream Interface Packet Transfers
  - Reading packets from the Serenade chip
  - Writing Packets to the Serenade chip
  - Multicast Packet Handling
  - Register Read and Write Operations
  - Route Table
- Packet Buffer Manager Operation
  - Packet Buffer Organization
  - Packet Buffer Queue Types
  - Using the Queues
  - Packet Buffer Operations
- Operation of the Network Interface
  - PHY Interface
  - Layer 2 Filtering
  - Layer 3 Functions
  - Packet Receive Process
  - Network Management Process

Chapter 5 Register Reference

5.1 Overview

The Serenade chip is mapped into 512 bytes (32-bit wide) of CPU address space. These registers are described in the “EdgeStream Interface Registers” section in the Serenade Data Book.

There are several hundred more internal registers to this device. These registers cannot be accessed directly; they are accessed indirectly via the Control Bus Address and Control Bus Data registers (80 and 84 hex respectively). These internal registers are also described in the “Internal Registers” section in the Serenade Data Book.

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