DTC114EM3T5G Series

Digital Transistors (BRT)

NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The digital transistor contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. The digital transistor eliminates these individual components by integrating them into a single device. The use of a digital transistor can reduce both system cost and board space. The device is housed in the SOT−723 package which is designed for low power surface mount applications.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- The SOT−723 Package can be Soldered using Wave or Reflow.
- Available in 4 mm, 8000 Unit Tape & Reel
- These are Pb−Free Devices

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

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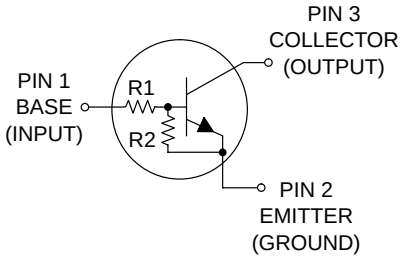
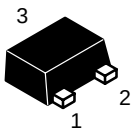
NPN SILICON DIGITAL TRANSISTORS



MARKING DIAGRAM



CASE 631AA
SOT−723
Style 1

XX = Specific Device Code
(See Marking Table on page 2)
M = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page of this data sheet.

DEVICE MARKING AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Package	Shipping†
DTC114EM3T5G	8A	10	10	SOT−723 (Pb−Free)	8000/Tape & Reel
DTC124EM3T5G	8B	22	22		
DTC144EM3T5G	8C	47	47		
DTC114YM3T5G	8D	10	47		
DTC114TM3T5G	94	10	∞		
DTC143TM3T5G	8F	4.7	∞		
DTC123EM3T5G	8H	2.2	2.2		
DTC143EM3T5G	8J	4.7	4.7		
DTC143ZM3T5G*	8K	4.7	47		
DTC124XM3T5G*	8L	22	47		
DTC123JM3T5G	8M	2.2	47		
DTC115EM3T5G	8N	100	100		
DTC144WM3T5G*	8P	47	22		

*Available upon request

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation, FR−4 Board (Note 1) @ T_A = 25°C Derate above 25°C	P_D	 260 2.0	 mW mW/°C
Thermal Resistance, Junction−to−Ambient (Note 1)	$R_{\theta JA}$	480	°C/W
Total Device Dissipation, FR−4 Board (Note 2) @ T_A = 25°C Derate above 25°C	P_D	 600 4.8	 mW mW/°C
Thermal Resistance, Junction−to−Ambient (Note 2)	$R_{\theta JA}$	205	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

1. FR−4 @ Minimum Pad
2. FR−4 @ 1.0 × 1.0 Inch Pad

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Base Cutoff Current (V_{CB} = 50 V, I_E = 0)		I_{CBO}	−	−	100	nAdc
Collector−Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)		I_{CEO}	−	−	500	nAdc
Emitter−Base Cutoff Current	DTC114EM3T5G	I_{EBO}	−	−	0.5	mAdc
(V_{EB} = 6.0 V, I_C = 0)	DTC124EM3T5G		−	−	0.2	
	DTC144EM3T5G		−	−	0.1	
	DTC114YM3T5G		−	−	0.2	
	DTC114TM3T5G		−	−	0.9	
	DTC143TM3T5G		−	−	1.9	
	DTC123EM3T5G		−	−	2.3	
	DTC143EM3T5G		−	−	1.5	
	DTC143ZM3T5G		−	−	0.18	
	DTC124XM3T5G		−	−	0.13	
	DTC123JM3T5G		−	−	0.2	
	DTC115EM3T5G		−	−	0.05	
	DTC144WM3T5G		−	−	0.13	
Collector−Base Breakdown Voltage (I_C = 10 μA, I_E = 0)		$V_{(BR)CBO}$	50	−	−	Vdc
Collector−Emitter Breakdown Voltage (Note 3) (I_C = 2.0 mA, I_B = 0)		$V_{(BR)CEO}$	50	−	−	Vdc
ON CHARACTERISTICS (Note 3)						
DC Current Gain	DTC114EM3T5G	h_{FE}	35	60	−	
(V_{CE} = 10 V, I_C = 5.0 mA)	DTC124EM3T5G		60	100	−	
	DTC144EM3T5G		80	140	−	
	DTC114YM3T5G		80	140	−	
	DTC114TM3T5G		160	350	−	
	DTC143TM3T5G		160	350	−	
	DTC123EM3T5G		8.0	15	−	
	DTC143EM3T5G		15	30	−	
	DTC143ZM3T5G		80	200	−	
	DTC124XM3T5G		80	150	−	
	DTC123JM3T5G		80	140	−	
	DTC115EM3T5G		80	150	−	
	DTC144WM3T5G		80	140	−	
Collector−Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.3 mA) (I_C = 10 mA, I_B = 5 mA) DTC123EM3T5G (I_C = 10 mA, I_B = 1 mA) DTC143TM3T5G/DTC114TM3T5G/ DTC143EM3T5G/DTC143ZM3T5G/DTC124XM3T5G		$V_{CE(sat)}$	−	−	0.25	Vdc
Output Voltage (on)		V_{OL}				Vdc
(V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	DTC114EM3T5G		−	−	0.2	
	DTC124EM3T5G		−	−	0.2	
	DTC114YM3T5G		−	−	0.2	
	DTC114TM3T5G		−	−	0.2	
	DTC143TM3T5G		−	−	0.2	
	DTC123EM3T5G		−	−	0.2	
	DTC143EM3T5G		−	−	0.2	
	DTC143ZM3T5G		−	−	0.2	
	DTC124XM3T5G		−	−	0.2	
	DTC123JM3T5G		−	−	0.2	
(V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ)	DTC144EM3T5G		−	−	0.2	
(V_{CC} = 5.0 V, V_B = 5.5 V, R_L = 1.0 kΩ)	DTC115EM3T5G		−	−	0.2	
(V_{CC} = 5.0 V, V_B = 4.0 V, R_L = 1.0 kΩ)	DTC144WM3T5G		−	−	0.2	
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ) (V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ) DTC143TM3T5G DTC143ZM3T5G DTC114TM3T5G		V_{OH}	4.9	−	−	Vdc

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Resistor	DTC114EM3T5G	R1	7.0	10	13	kΩ
	DTC124EM3T5G		15.4	22	28.6	
	DTC144EM3T5G		32.9	47	61.1	
	DTC114YM3T5G		7.0	10	13	
	DTC114TM3T5G		7.0	10	13	
	DTC143TM3T5G		3.3	4.7	6.1	
	DTC123EM3T5G		1.5	2.2	2.9	
	DTC143EM3T5G		3.3	4.7	6.1	
	DTC143ZM3T5G		3.3	4.7	6.1	
	DTC124XM3T5G		15.4	22	28.6	
	DTC123JM3T5G		1.54	2.2	2.86	
	DTC115EM3T5G		70	100	130	
	DTC144WM3T5G		32.9	47	61.1	
Resistor Ratio	DTC114EM3T5G/DTC124EM3T5G/DTC144EM3T5G/ DTC115EM3T5G	R_1/R_2	0.8	1.0	1.2	
	DTC114YM3T5G		0.17	0.21	0.25	
	DTC143TM3T5G/DTC114TM3T5G		–	–	–	
	DTC123EM3T5G/DTC143EM3T5G		0.8	1.0	1.2	
	DTC143ZM3T5G		0.055	0.1	0.185	
	DTC124XM3T5G		0.38	0.47	0.56	
	DTC123JM3T5G		0.038	0.047	0.056	
	DTC144WM3T5G		1.7	2.1	2.6	

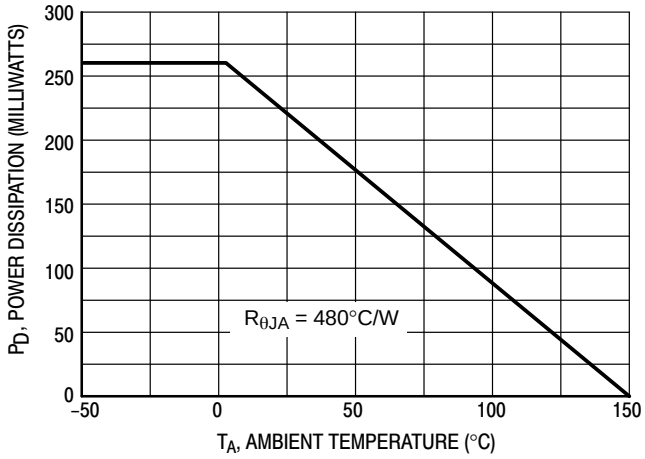


Figure 1. Derating Curve

TYPICAL ELECTRICAL CHARACTERISTICS − DTC114EM3T5G

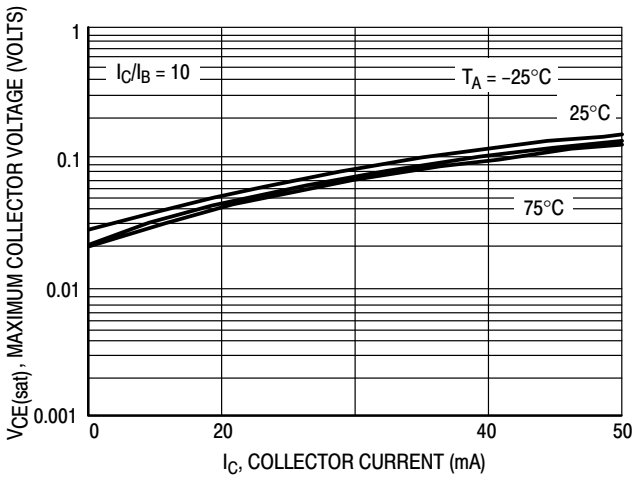


Figure 2. $V_{CE(sat)}$ versus I_C

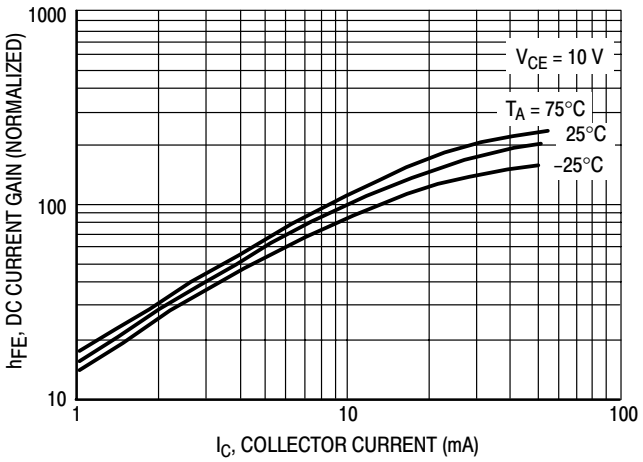


Figure 3. DC Current Gain

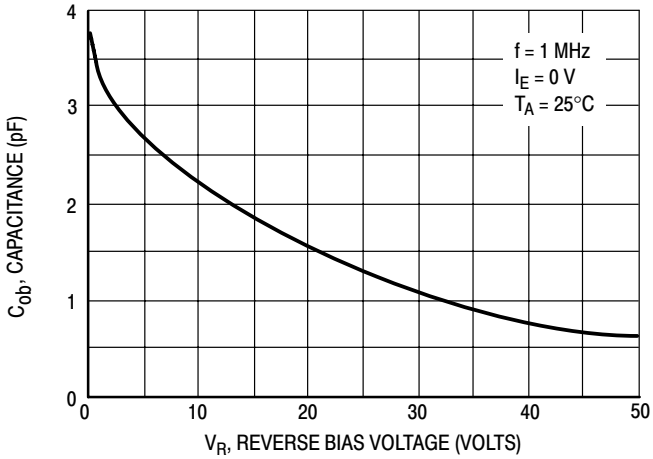


Figure 4. Output Capacitance

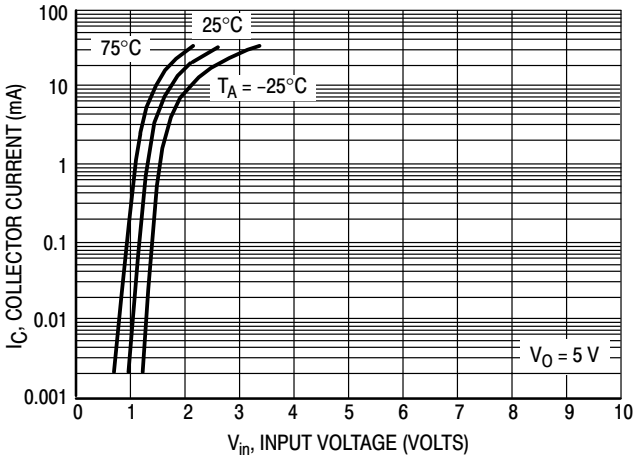


Figure 5. Output Current versus Input Voltage

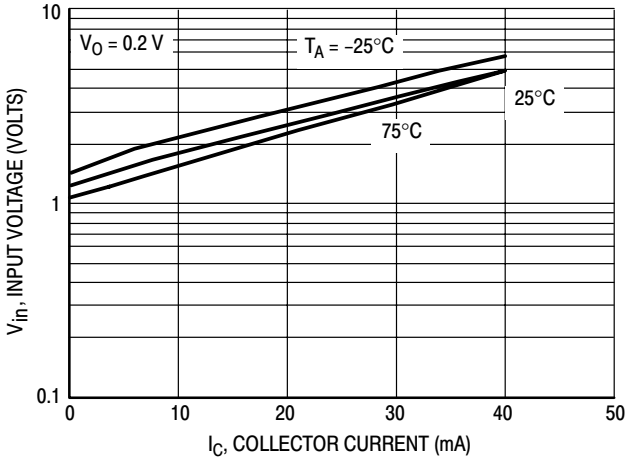


Figure 6. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS − DTC124EM3T5G

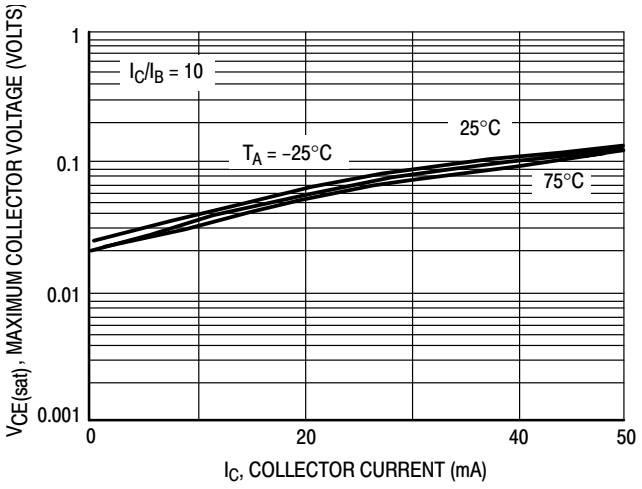


Figure 7. $V_{CE(sat)}$ versus I_C

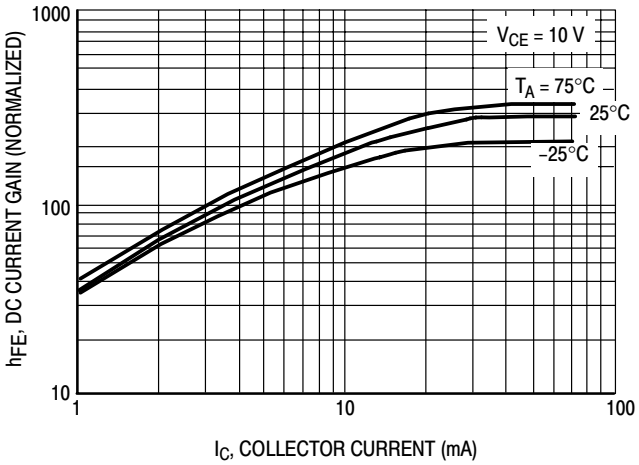


Figure 8. DC Current Gain

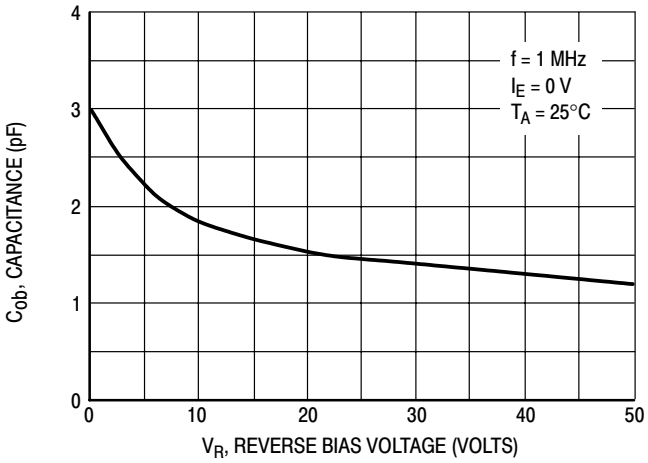


Figure 9. Output Capacitance

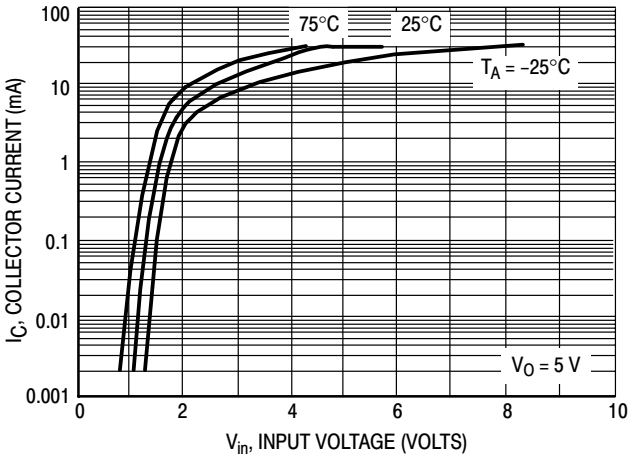


Figure 10. Output Current versus Input Voltage

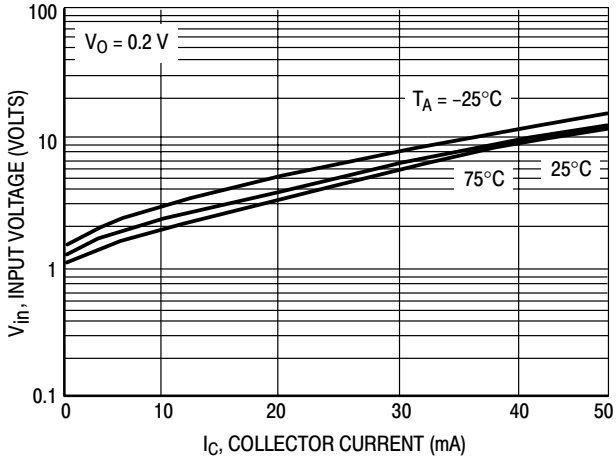


Figure 11. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS − DTC144EM3T5G

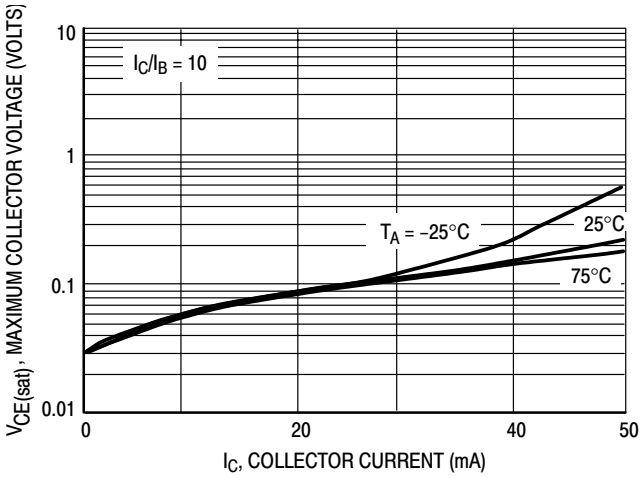


Figure 12. $V_{CE(sat)}$ versus I_C

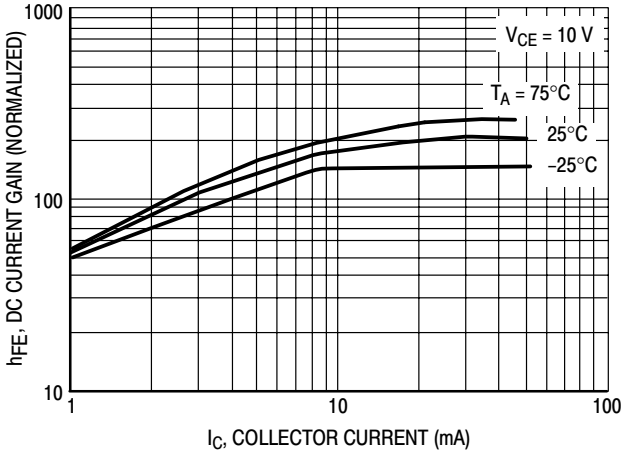


Figure 13. DC Current Gain

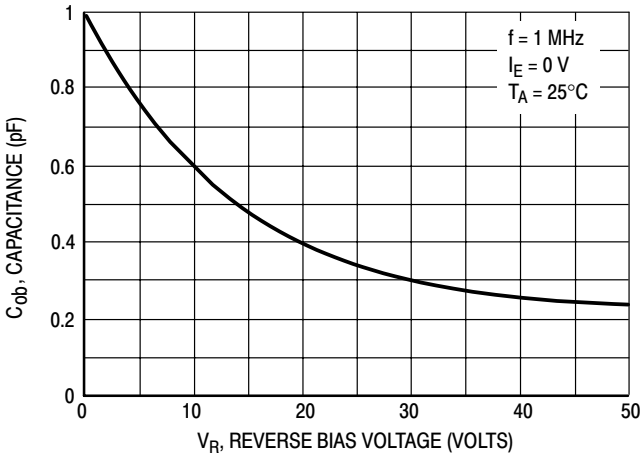


Figure 14. Output Capacitance

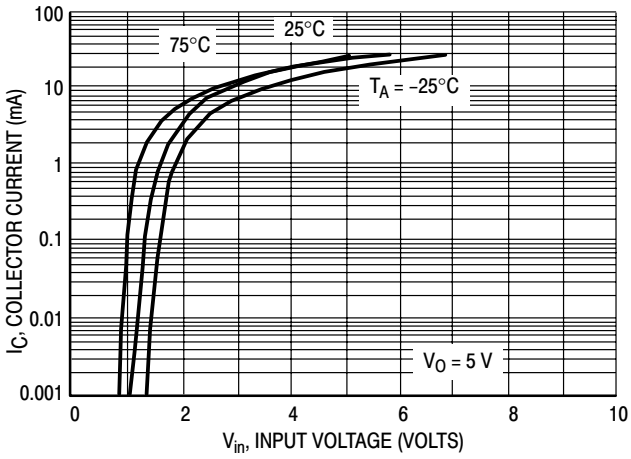


Figure 15. Output Current versus Input Voltage

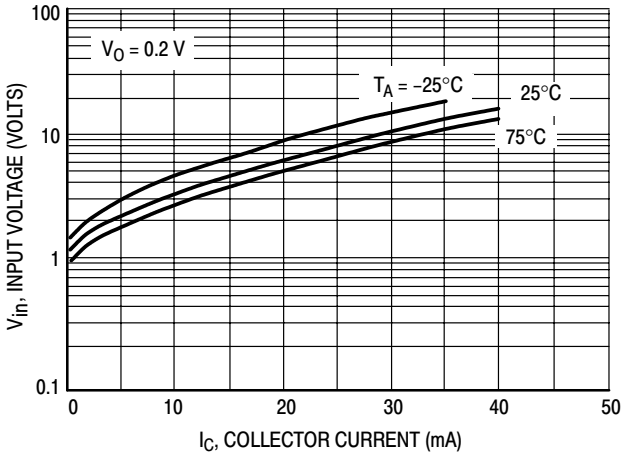


Figure 16. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS − DTC114YM3T5G

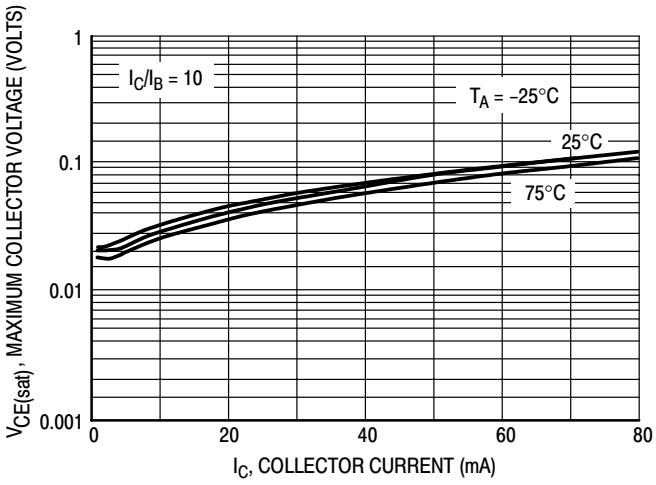


Figure 17. $V_{CE(sat)}$ versus I_C

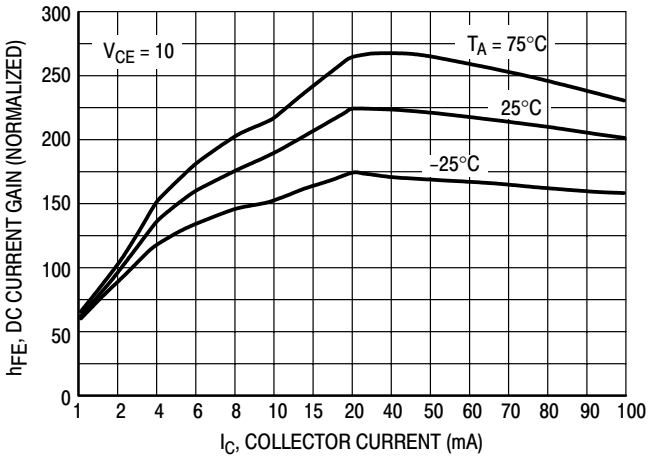


Figure 18. DC Current Gain

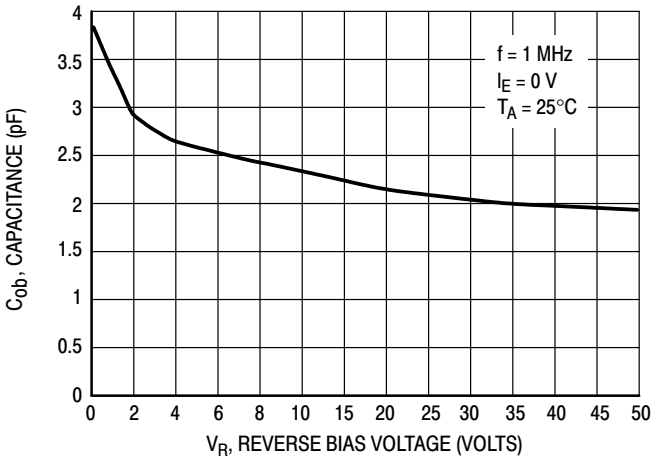


Figure 19. Output Capacitance

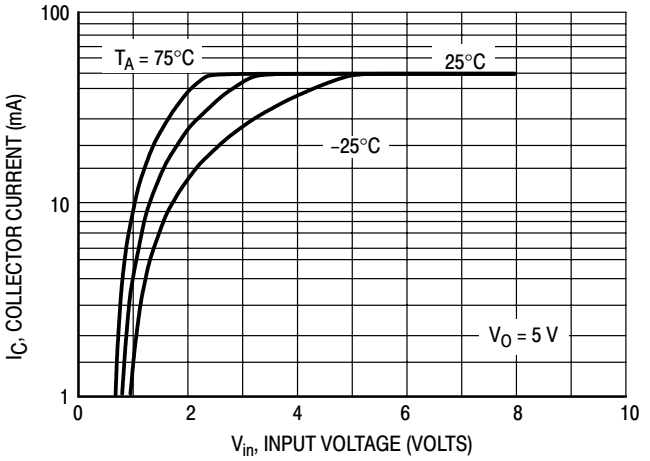


Figure 20. Output Current versus Input Voltage

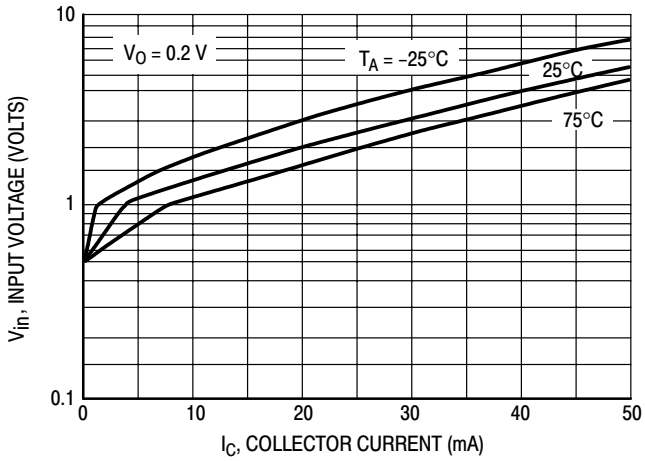


Figure 21. Input Voltage versus Output Current

TYPICAL APPLICATIONS FOR NPN BRTs

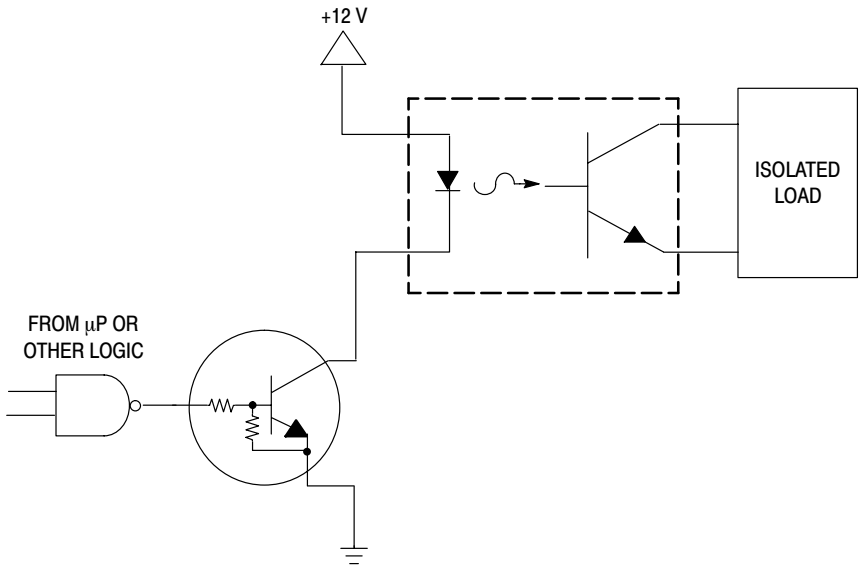


Figure 22. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

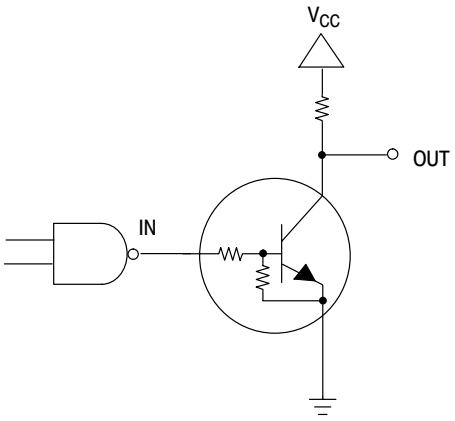


Figure 23. Open Collector Inverter: Inverts the Input Signal

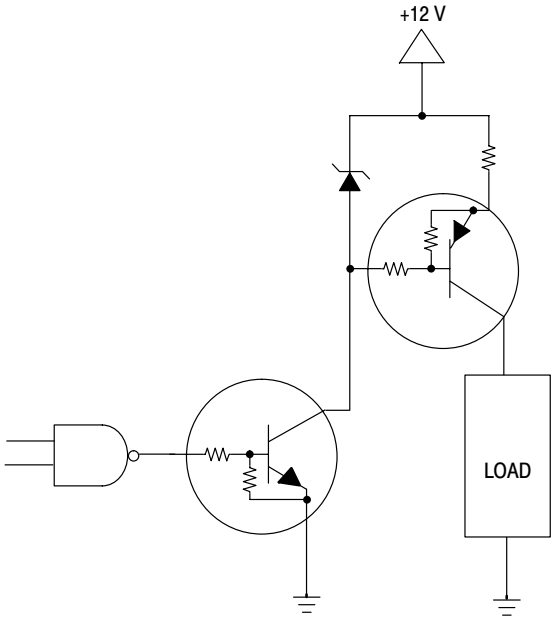
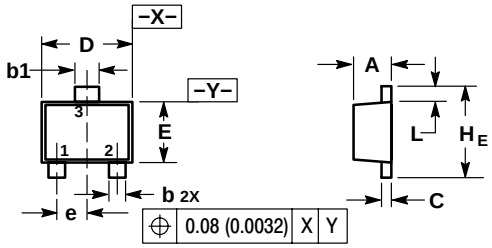


Figure 24. Inexpensive, Unregulated Current Source

PACKAGE DIMENSIONS

SOT−723
CASE 631AA−01
ISSUE A

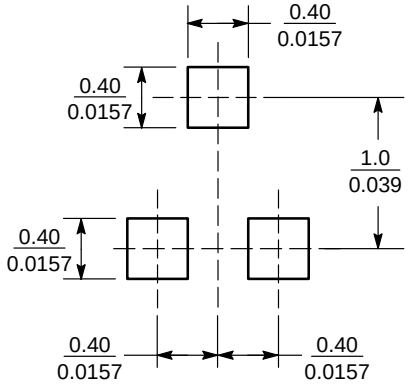


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.50	0.55	0.018	0.020	0.022
b	0.15	0.20	0.27	0.0059	0.0079	0.0106
b1	0.25	0.3	0.35	0.010	0.012	0.014
C	0.07	0.12	0.17	0.0028	0.0047	0.0067
D	1.15	1.20	1.25	0.045	0.047	0.049
E	0.75	0.80	0.85	0.03	0.032	0.034
e	0.40 BSC			0.016 BSC		
H_E	1.15	1.20	1.25	0.045	0.047	0.049
L	0.15	0.20	0.25	0.0059	0.0079	0.0098

SOLDERING FOOTPRINT*



SCALE 20:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

SOT−723

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.

DTC114EM3/D