

## 16-Channel Wideband Video Multiplexers

### FEATURES

- Crosstalk:  $-100\text{ dB}$  @  $5\text{ MHz}$
- $300\text{ MHz}$  Bandwidth
- Low Input and Output Capacitance
- Low Power:  $75\text{ }\mu\text{W}$
- Low  $r_{DS(on)}$ :  $50\text{ }\Omega$
- On-Board Address Latches
- Disable Output

### BENEFITS

- High Video Quality
- Reduced Insertion Loss
- Reduced Input Buffer Requirements
- Minimizes Power Consumption
- Simplifies Bus Interface

### APPLICATIONS

- Video Switching/Routing
- High Speed Data Routing
- RF Signal Multiplexing
- Precision Data Acquisition
- Crosspoint Arrays
- FLIR Systems

### DESCRIPTION

The DG535/536 are 16-channel multiplexers designed for routing one of 16 wideband analog or digital input signals to a single output. They feature low input and output capacitance, low on-resistance, and n-channel DMOS "T" switches, resulting in wide bandwidth, low crosstalk and high "off" isolation. In the on state, the switches pass signals in either direction, allowing them to be used as multiplexers or as demultiplexers.

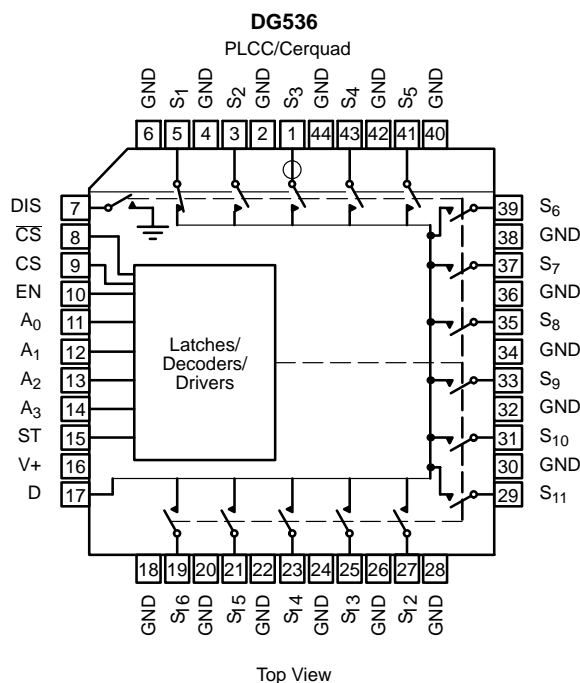
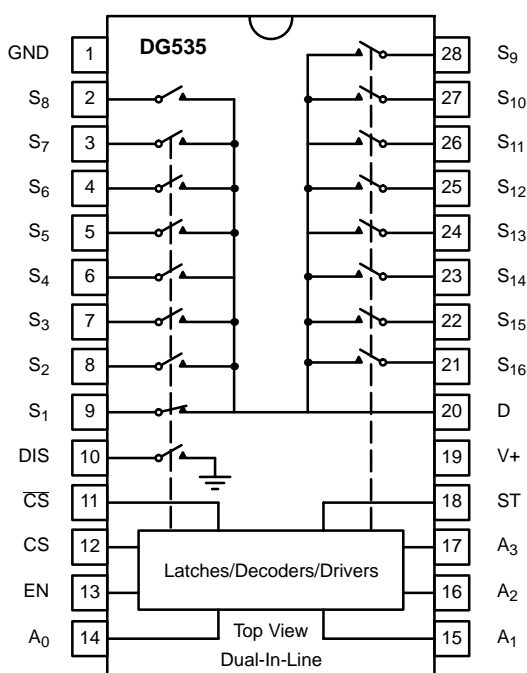
On-chip address latches and decode logic simplify microprocessor interface. Chip Select and Enable inputs simplify addressing in large matrices. Single-supply operation

and a low  $75\text{-}\mu\text{W}$  power consumption vastly reduces power supply requirements.

These devices are built on a proprietary D/CMOS process which creates low-capacitance DMOS FETs and high-speed, low-power CMOS logic on the same substrate.

For more information please refer to Vishay Siliconix Application Note AN501 (FaxBack document number 70608).

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



**TRUTH TABLES AND ORDERING INFORMATION**

ORDERING INFORMATION		
Temperature Range	Package	Part Number
-40 to 85°C	28-Pin Plastic DIP	DG535DJ
	44-Pin PLCC	DG536DN
-55 to 125°C	28-Pin Sidebrazed	DG535AP
		DG535AP/883
	44-Pin Cerquad	DG536AM/883

TRUTH TABLE									
EN	CS	$\overline{CS}$	ST <sup>a</sup>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Channel Selected	Disable <sup>b</sup>
0	X	X	1	X	X	X	X	None	High Z
X	0	X							
X	X	1							
1	1	0	1	0	0	0	0	S <sub>1</sub>	Low Z
				0	0	0	1	S <sub>2</sub>	
				0	0	1	0	S <sub>3</sub>	
				0	0	1	1	S <sub>4</sub>	
				0	1	0	0	S <sub>5</sub>	
				0	1	0	1	S <sub>6</sub>	
				0	1	1	0	S <sub>7</sub>	
				0	1	1	1	S <sub>8</sub>	
				1	0	0	0	S <sub>9</sub>	
				1	0	0	1	S <sub>10</sub>	
				1	0	1	0	S <sub>11</sub>	
				1	0	1	1	S <sub>12</sub>	
				1	1	0	0	S <sub>13</sub>	
				1	1	0	1	S <sub>14</sub>	
				1	1	1	0	S <sub>15</sub>	
				1	1	1	1	S <sub>16</sub>	
X	X	X	0	X	X	X	X	Maintains previous switch condition	High Z or Low Z

Logic "0" =  $V_{AL} \leq 4.5\text{ V}$   
 Logic "1" =  $V_{AH} \geq 10.5\text{ V}$   
 X = Don't Care

Notes:

- Strobe input (ST) is level triggered.
- Low Z, High Z = impedance of Disable Output to GND. Disable output sinks current when any channel is selected.

**ABSOLUTE MAXIMUM RATINGS**

V <sub>+</sub> to GND	-0.3 V to +18 V
Digital Inputs	(GND - 0.3 V) to (V <sub>+</sub> plus 2 V) or 20 mA, whichever occurs first
V <sub>S</sub> , V <sub>D</sub>	(GND - 0.3 V) to V <sub>+</sub> plus 2 V) or 20 mA, whichever occurs first
Current (any terminal) Continuous	20 mA
Current (S or D) Pulsed 1 ms 10% duty cycle	40 mA
Storage Temperature (A Suffix)	-65 to 150°C
(D Suffix)	-65 to 125°C
Power Dissipation (Package) <sup>a</sup>	
28-Pin Plastic DIP <sup>b</sup>	625 mW

28-Pin Sidebrazed <sup>c</sup>	1200 mW
44-Pin PLCC <sup>d</sup>	450 mW
44-Pin Cerquad <sup>e</sup>	825 mW

Notes:

- All leads soldered or welded to PC board.
- Derate 8.6 mW/°C above 75°C.
- Derate 16 mW/°C above 75°C.
- Derate 6 mW/°C above 75°C.
- Derate 11 mW/°C above 75°C.



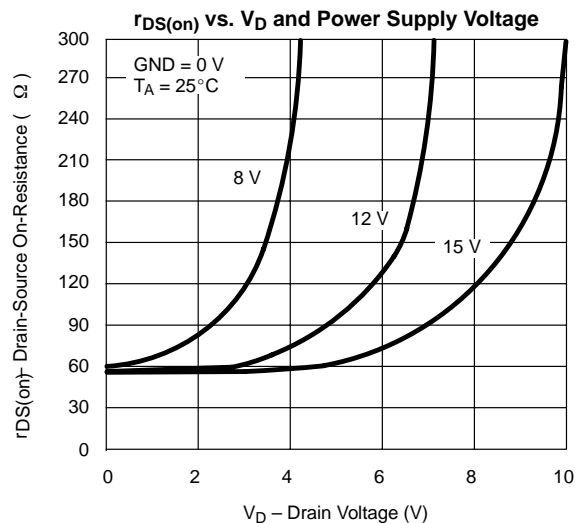
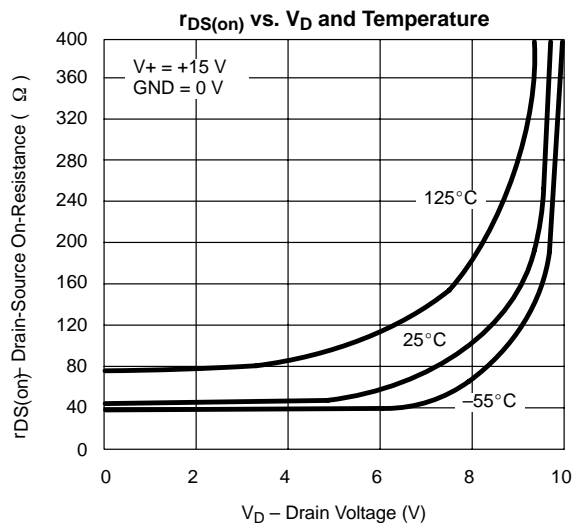
SPECIFICATIONS <sup>a</sup>										
Parameter	Symbol	Test Conditions Unless Otherwise Specified  V <sub>+</sub> = 15 V, ST, CS = 10.5 V CS = 4.5 V, V <sub>A</sub> = 4.5 or 10.5 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix –55 to 125°C		D Suffix –40 to 85°C		Unit	
					Min <sup>c</sup>	Max <sup>c</sup>	Min <sup>c</sup>	Max <sup>c</sup>		
Analog Switch										
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		0	10	0	10	V	
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = –1 mA, V <sub>D</sub> = 3 V EN = 10.5 V Sequence Each Switch On	Room Full	55		90 120		90 120	Ω	
Resistance Match	Δr <sub>DS(on)</sub>		Room			9		9		
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = 3 V, V <sub>D</sub> = 0 V, EN = 4.5 V	Room Full		–10 –100	10 100	–10 –100	10 100	nA	
Drain On Leakage Current	I <sub>D(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = 3 V, EN = 10.5 V	Room Full		–10 –1000	10 1000	–10 –100	–10 –100		
Disable Output	R <sub>DISABLE</sub>	I <sub>DISABLE</sub> = 1 mA, EN = 10.5 V	Room Full	100		200 250		200 250	Ω	
Digital Control										
Input Voltage High	V <sub>AIH</sub>		Full		10.5		10.5		V	
Input Voltage Low	V <sub>AIL</sub>		Full			4.5		4.5		
Address Input Current	I <sub>AI</sub>	V <sub>A</sub> = GND or V <sub>+</sub>	Room Full	<0.01	–1 –100	1 100	–1 –100	1 100	μA	
Address Input Capacitance	C <sub>A</sub>		Full	5					pF	
Dynamic Characteristics										
On State Input Capacitance <sup>e</sup>	C <sub>S(on)</sub>	V <sub>D</sub> = V <sub>S</sub> = 3 V	PLCC	Room	32		45		45	pF
			Cerquad	Room	35					
			DIP	Room	40		55		55	
Off State Input Capacitance <sup>e</sup>	C <sub>S(off)</sub>	V <sub>S</sub> = 3 V	PLCC	Room	2		8		8	
			Cerquad	Room	5					
			DIP	Room	3					
Off State Output Capacitance <sup>e</sup>	C <sub>D(off)</sub>	V <sub>D</sub> = 3 V	PLCC	Room	8		20		20	
			Cerquad	Room	12					
			DIP	Room	9					
Multiplexer Switching Time	t <sub>TRANS</sub>	See Figure 4	Full			300		300	ns	
Break-Before-Make Interval	t <sub>OPEN</sub>		Full		25		25			
EN, CS, CS, ST, t <sub>ON</sub>	t <sub>ON</sub>	See Figure 2 and 3	Full			300		300		
EN, CS, CS, ST, t <sub>OFF</sub>	t <sub>OFF</sub>	See Figure 2	Full			150		150		
Charge Injection	Q	See Figure 5	Room	–35					pC	
Single-Channel Crosstalk	XTALK(SC)	R <sub>IN</sub> = 75 Ω R <sub>L</sub> = 75 Ω f = 5 MHz See Figure 9	PLCC	Room	–100					dB
			Cerquad	Room	–93					
			DIP	Room	–60					
Chip Disabled Crosstalk	XTALK(CD)	R <sub>IN</sub> = R <sub>L</sub> = 75 Ω f = 5 MHz EN = 4.5 V See Figure 8	PLCC	Room	–85					
			Cerquad	Room	–84					
			DIP	Room	–60					

**SPECIFICATIONS<sup>a</sup>**

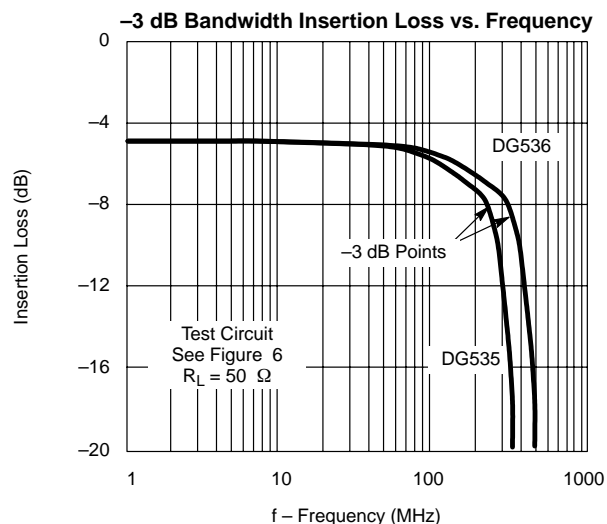
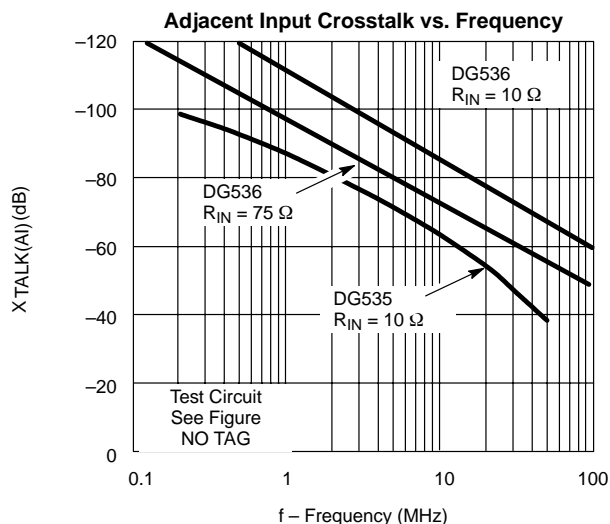
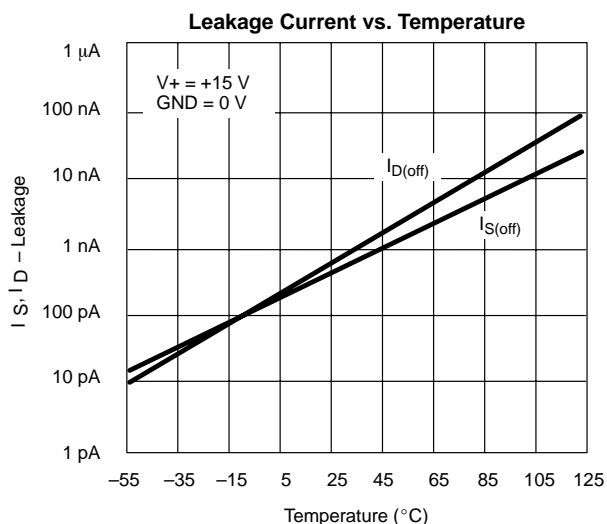
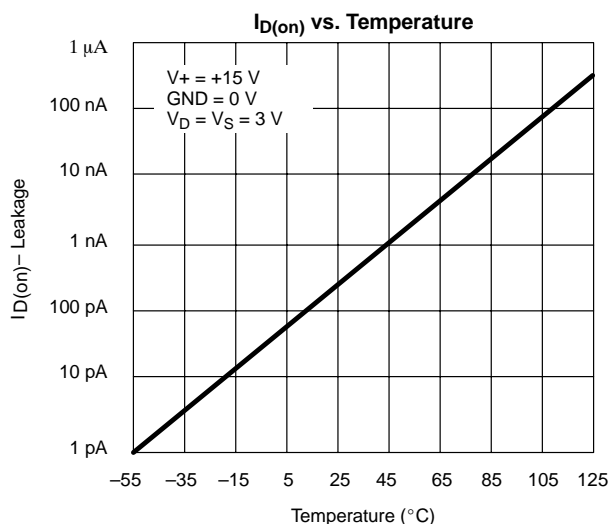
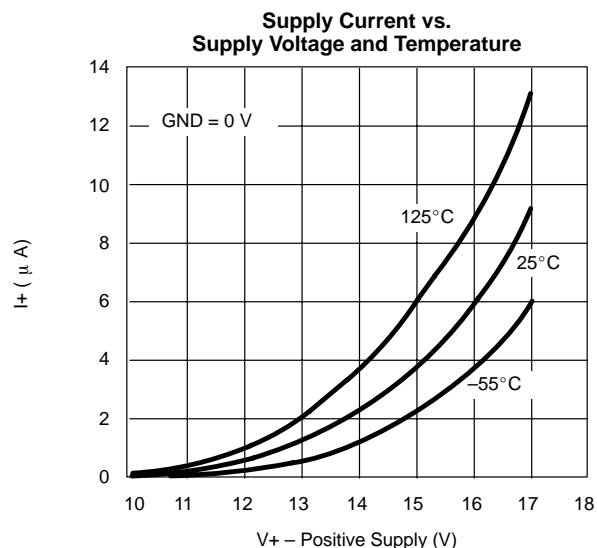
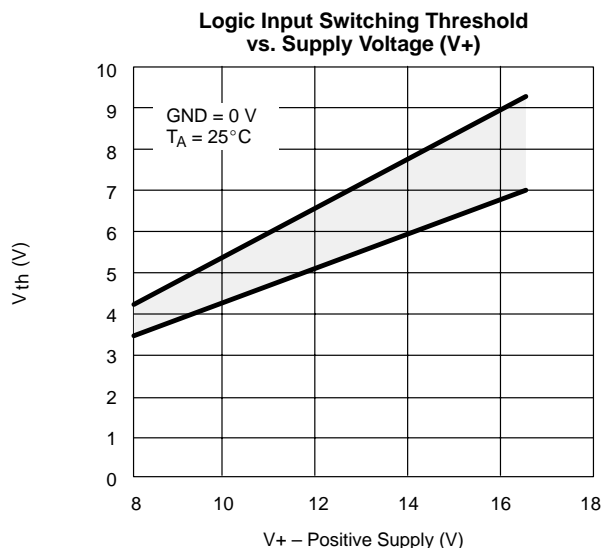
Parameter	Symbol	Test Conditions Unless Otherwise Specified  V+ = 15 V, ST, CS = 10.5 V CS = 4.5 V, VA = 4.5 or 10.5 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix –55 to 125°C		D Suffix –40 to 85°C		Unit	
					Min <sup>c</sup>	Max <sup>c</sup>	Min <sup>c</sup>	Max <sup>c</sup>		
Dynamic Characteristics (Cont'd)										
Adjacent Input Crosstalk	XTALK(AI)	RIN = 10 Ω RL = 10 kΩ f = 5 MHz See Figure NO TAG	PLCC	Room	–92				dB	
			Cerquad	Room	–87					
			DIP	Room	–72					
All Hostile Crosstalk <sup>e</sup>	XTALK(AH)	RIN = 10 Ω RL = 10 kΩ f = 5 MHz See Figure 7	PLCC	Room	–74	–60	–60			
			Cerquad	Room	–74					
			DIP	Room	–60					
Bandwidth	BW	RL = 50 Ω, See Figure 6		Room	500				MHz	
Power Supplies										
Positive Supply Current	I+	Any One ChanngeI Selected with All Logic Inputs at GND or V+		Room Full	5		50 100		50 100	μA
Supply Voltage Range	V+			Full		10	16.5	10	16.5	V
Minimum Input Timing Requirements										
Strobe Pulse Width	tSW	See Figure 1		Full		200		200		ns
A0, A1, A2, A3 CS, CS, EN Data Valid to Strobe	tDW			Full		100		100		
A0, A1, A2, A3 CS, CS, EN Data Valid after Strobe	tWD			Full		50		50		

## Notes:

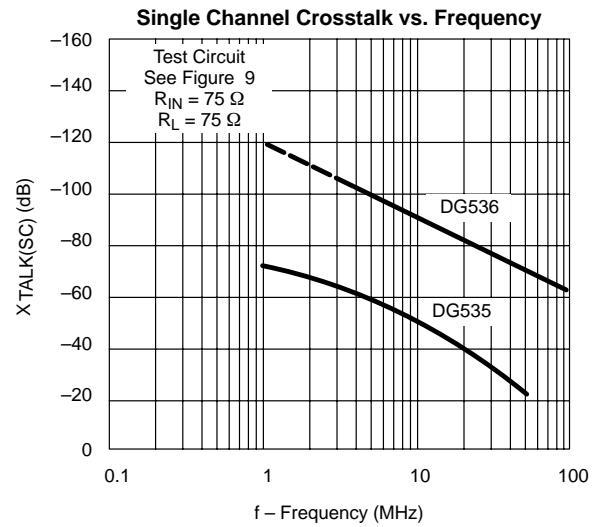
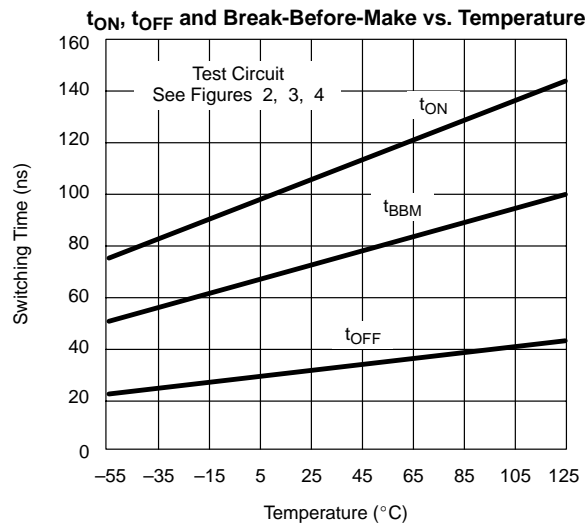
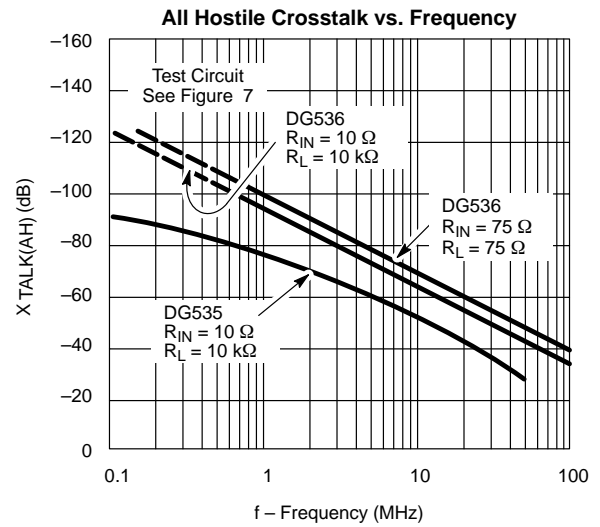
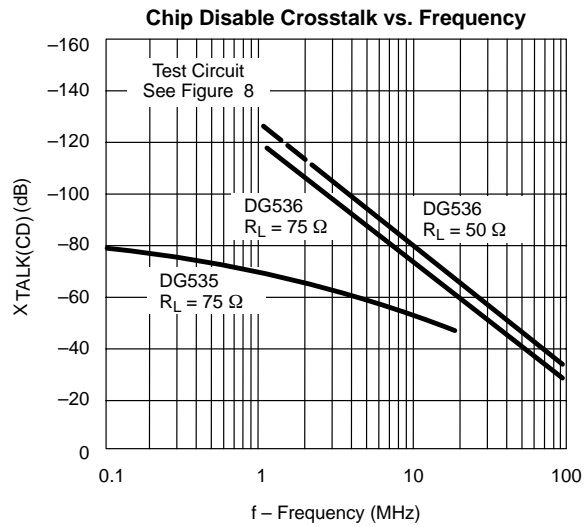
- a. Refer to PROCESS OPTION FLOWCHART.  
b. Room = 25°C, Full = as determined by the operating temperature suffix.  
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.  
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.  
e. Guaranteed by design, not subject to production test.  
f.  $V_A$  = input voltage to perform proper function.

**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

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**INPUT TIMING REQUIREMENTS**

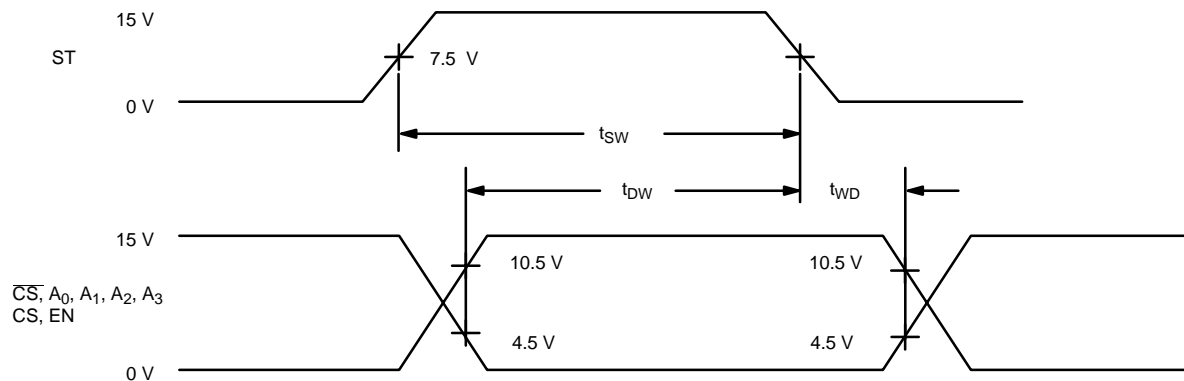
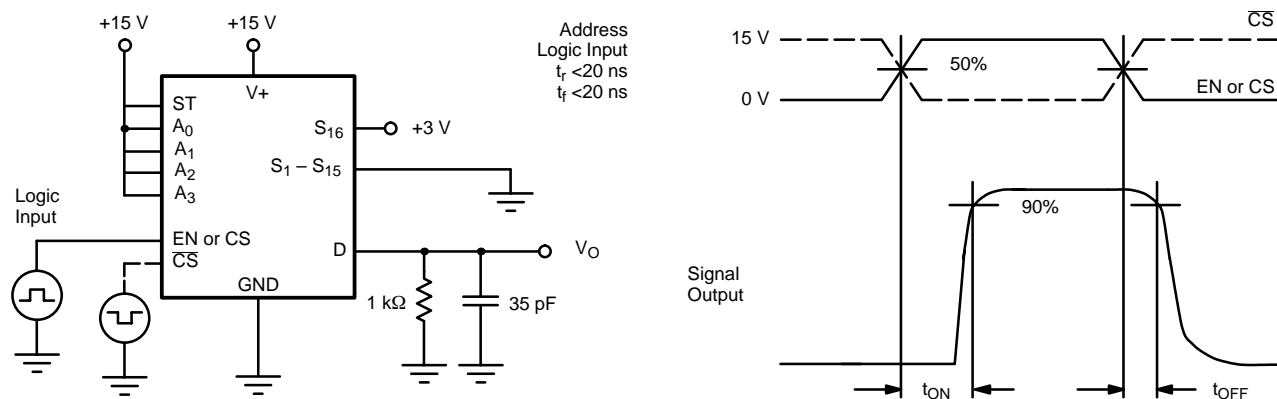
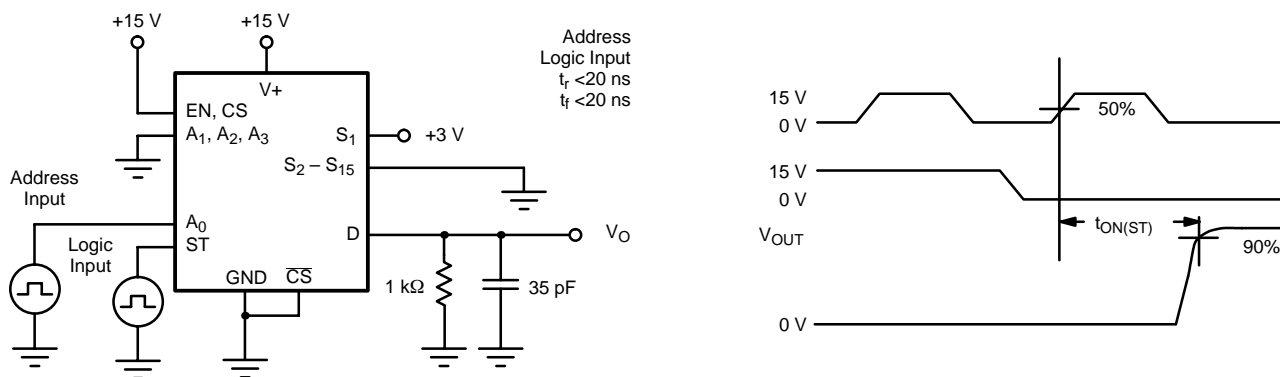


FIGURE 1.

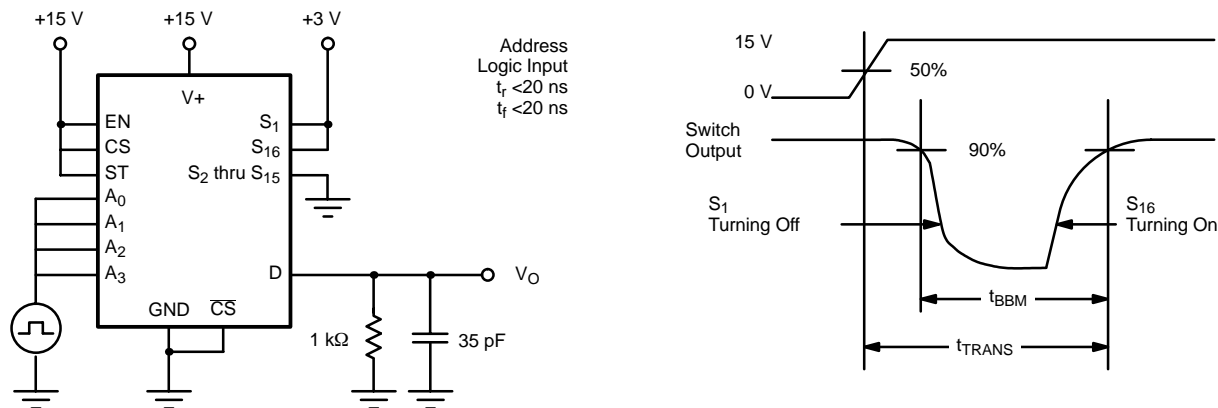
## TEST CIRCUITS



**FIGURE 2.** EN, CS,  $\overline{CS}$ , Turn On/Off Time

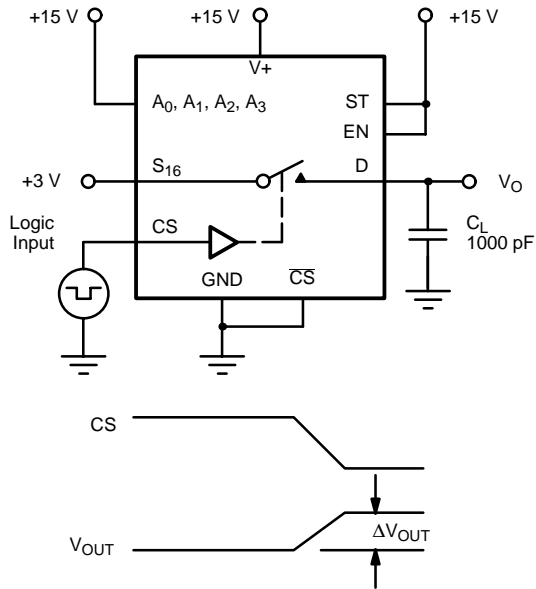


**FIGURE 3.** Strobe ST Turn On Time



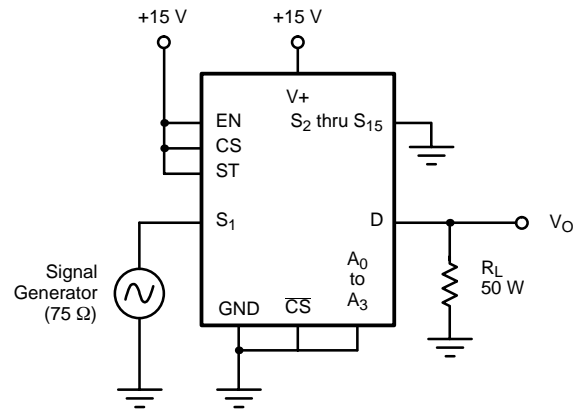
**FIGURE 4.** Transition Time and Break-Before-Make Interval

**TEST CIRCUITS**

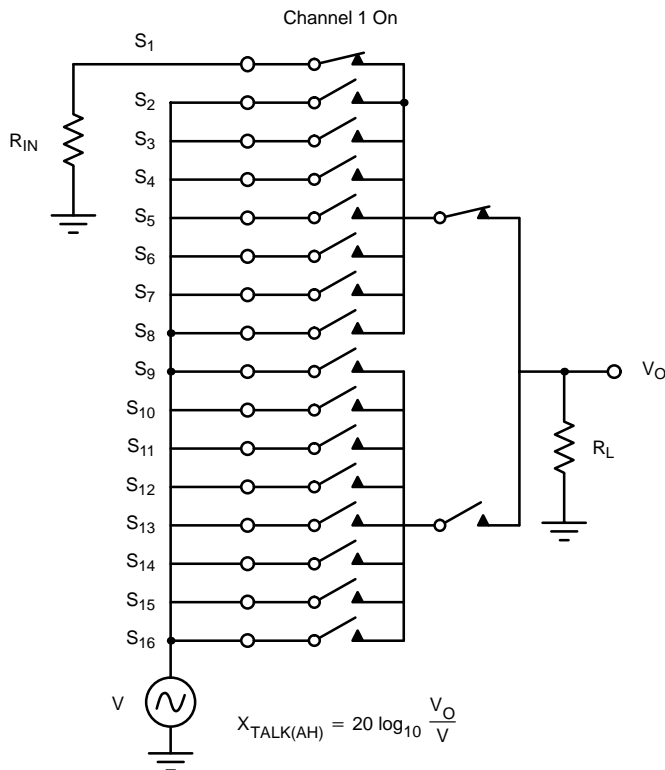


$\Delta V_{OUT}$  is the measured voltage error due to charge injection.  
The charge injection in Coulombs is  $Q = C_L \times \Delta V_{OUT}$

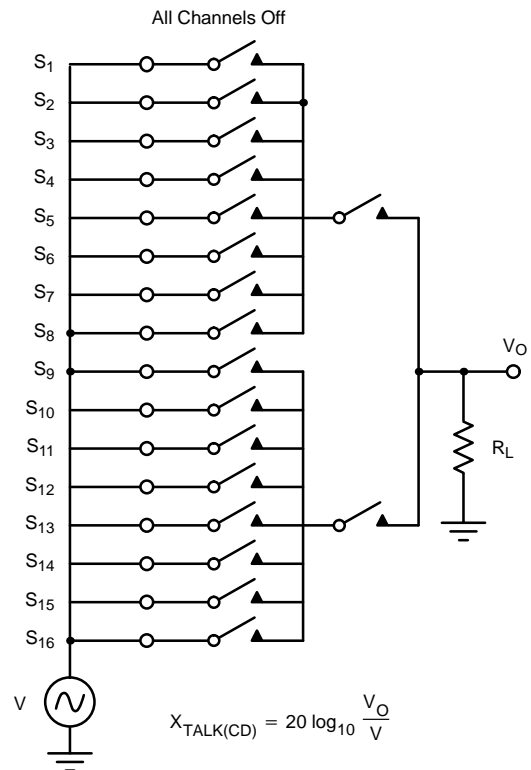
**FIGURE 5.** Charge Injection



**FIGURE 6.** Bandwidth



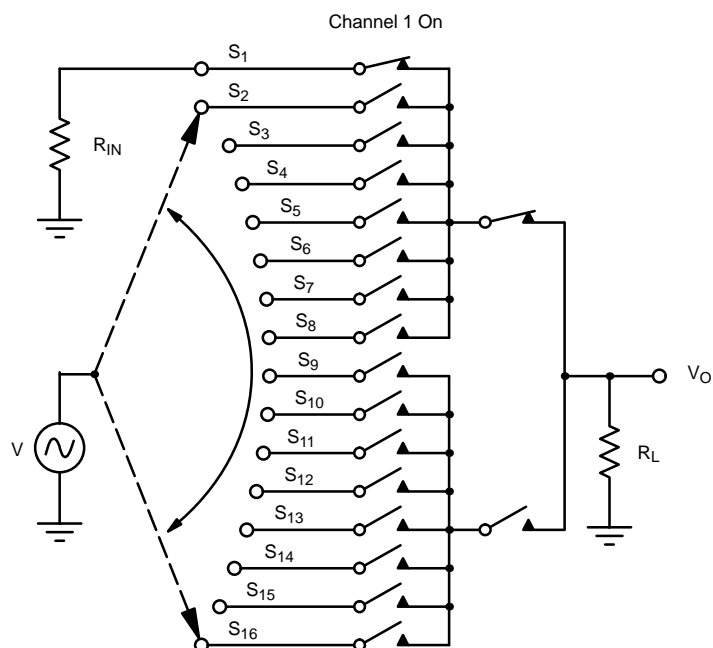
**FIGURE 7.** All Hostile Crosstalk



**FIGURE 8.** Chip Disabled Crosstalk



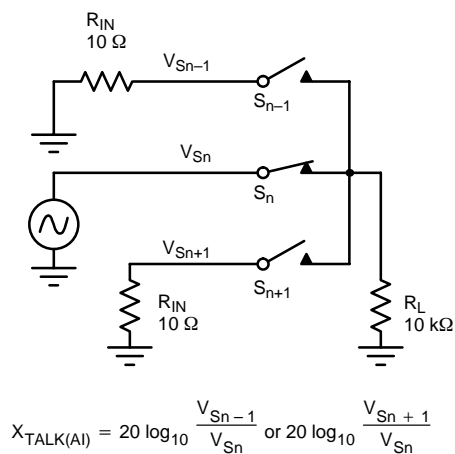
**TEST CIRCUITS**



Notes:

- Any individual channel between  $S_2$  and  $S_{16}$  can be selected
- $X_{TALK(SC)} = 20 \log_{10} \frac{V_O}{V}$  is scanned sequentially from  $S_2$  to  $S_{16}$

**FIGURE 9.** Single Channel Crosstalk



$$X_{TALK(AI)} = 20 \log_{10} \frac{V_{S_{n-1}}}{V_{S_n}} \text{ or } 20 \log_{10} \frac{V_{S_{n+1}}}{V_{S_n}}$$

**FIGURE 10.** Adjacent Input Crosstalk

PIN DESCRIPTION	
Symbol	Description
$S_1$ thru $S_{16}$	Analog inputs/outputs
D	Multiplexer output/demultiplexer input
DIS	Open drain low impedance to analog ground when any channel is selected
$\overline{CS}$ , CS, EN	Logic inputs to selected desired multiplexer(s) when using several multiplexers in a system
$A_0$ thru $A_3$	Binary address inputs to determine which channel is selected
ST	Strobe input that latches $A_0$ , $A_1$ , $A_2$ , $A_3$ , $\overline{CS}$ , CS, EN
V+	Positive supply voltage input
GND	Analog signal ground and most negative potential <b>All ground pins should be connected externally to ensure dynamic performance</b>

### DETAILED DESCRIPTION

The DG535/536 are 16-channel single-ended multiplexers with on-chip address logic and control latches.

The multiplexer connects one of sixteen inputs ( $S_1, S_2$  through  $S_{16}$ ) to a common output (D) under the control of a 4-bit binary address ( $A_0$  to  $A_3$ ). The specific input channel selected for each address is given in the Truth Table.

All four address inputs have on-chip data latches which are controlled by the Strobe (ST) input. These latches are transparent when Strobe is high but they maintain the chosen address when Strobe goes low. To facilitate easy microprocessor control in large matrices a choice of three independent logic inputs (EN, CS and  $\overline{CS}$ ) are provided on chip. These inputs are gated together (see Figure NO TAG) and only when  $EN = CS = 1$  and  $\overline{CS} = 0$  can an output switch be selected. This necessary logic condition is then latched-in when Strobe (ST) goes low.

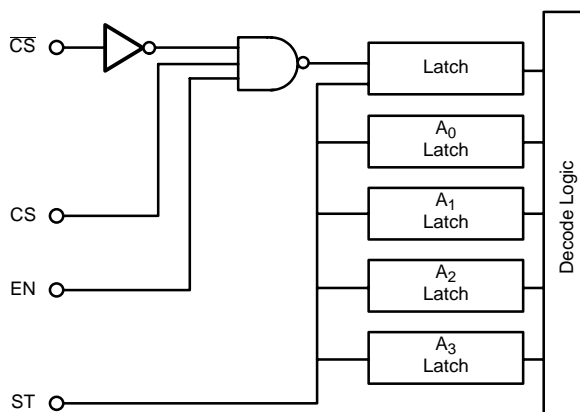


FIGURE 11.  $\overline{CS}$ , CS, EN, ST Control Logic

Break-before-make switching prevents momentary shorting when changing from one input to another.

The devices feature a two-level switch arrangement whereby two banks of eight switches (first level) are connected via two series switches (second level) to a common DRAIN output.

In order to improve crosstalk all sixteen first level switches are configured as "T" switches (see Figure NO TAG).

With this method  $SW_2$  operates out of phase with  $SW_1$  and  $SW_3$ . In the on condition  $SW_1$  and  $SW_3$  are closed with  $SW_2$  open whereas in the off condition  $SW_1$  and  $SW_3$  are open and  $SW_2$  closed. In the off condition the input to  $SW_3$  is effectively the isolation leakage of  $SW_1$  working into the on-resistance of  $SW_2$  (typically 200  $\Omega$ ).

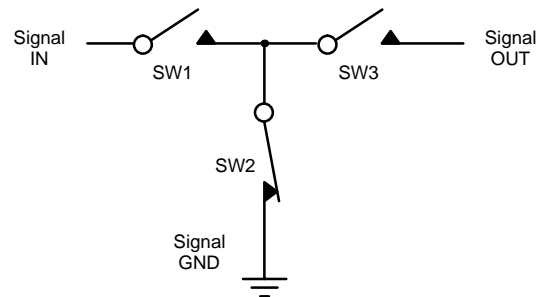


FIGURE 12. "T" Switch Arrangement

The two second level series switches further improve crosstalk and help to minimize output capacitance.

The DIS output can be used to signal external circuitry. DIS is a high impedance to GND when no channel is selected and a low impedance to GND when any one channel is selected.

The DG535/536 have extensive applications where any high frequency video or digital signals are switched or routed. Exceptional crosstalk and bandwidth performance is achieved by using n-channel DMOS FETs for the "T" and series switches.

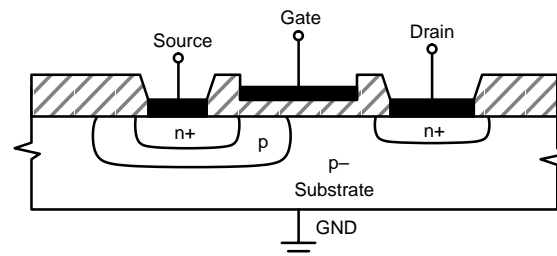


FIGURE 13. Cross-Section of a Single DMOS Switch

It can clearly be seen from Figure NO TAG that there exists a PN junction between the substrate and the drain/source terminals.

Should a signal which is negative with respect to the substrate (GND pin) be connected to a source or drain terminal, then the PN junction will become forward biased and current will flow between the signal source and GND. This effective shorting of the signal source to GND will not necessarily cause any damage to the device, provided that the total current flowing is less than the maximum rating, (i.e., 20 mA).

### DETAILED DESCRIPTION

Since no PN junctions exist between the signal path and  $V+$ , positive overvoltages are not a problem, unless the breakdown voltage of the DMOS drain terminal (see Figure NO TAG) (+18 V) is exceeded. Positive overvoltage conditions must not exceed +18 V with respect to the GND pin. If this condition is possible (e.g. transients in the signal), then a diode or Zener clamp may be used to prevent breakdown.

The overvoltage conditions described may exist if the supplies are collapsed while a signal is present on the inputs. If this condition is unavoidable, then the necessary steps outlined above should be taken to protect the device.

### DC Biasing

To avoid negative overvoltage conditions and subsequent distortion of ac analog signals, dc biasing may be necessary. Biasing is not required, however, in applications where signals are always positive with respect to the GND or substrate connection, or in applications involving multiplexing of low level (up to  $\pm 200$  mV) signals, where forward biasing of the PN substrate-source/drain terminals would not occur.

Biasing can be accomplished in a number of ways, the simplest of which is a resistive potential divider and a few dc blocking capacitors as shown in Figure NO TAG.

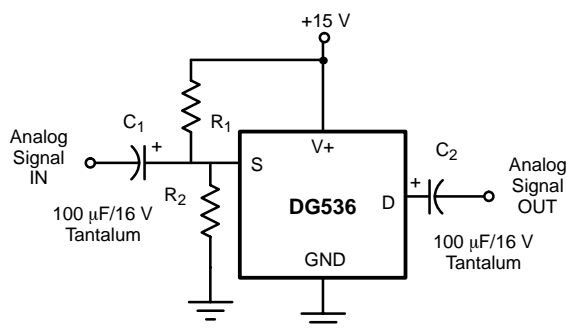


FIGURE 14. Simple Bias Circuit

$R_1$  and  $R_2$  are chosen to suit the appropriate biasing requirements. For video applications, approximately 3 V of bias is required for optimal differential gain and phase performance. Capacitor  $C_1$  blocks the dc bias voltage from

being coupled back to the analog signal source and  $C_2$  blocks the dc bias from the output signal. Both  $C_1$  and  $C_2$  should be tantalum or ceramic disc type capacitors in order to operate efficiently at high frequencies. Active bias circuits are recommended if rapid switching time between channels is required.

An alternative method is to offset the supply voltages (see Figure NO TAG).

Decoupling would have to be applied to the negative supply to ensure that the substrate is well referenced to signal ground. Again the capacitors should be of a type offering good high frequency characteristics.

Level shifting of the logic signals may be necessary using this offset supply arrangement.

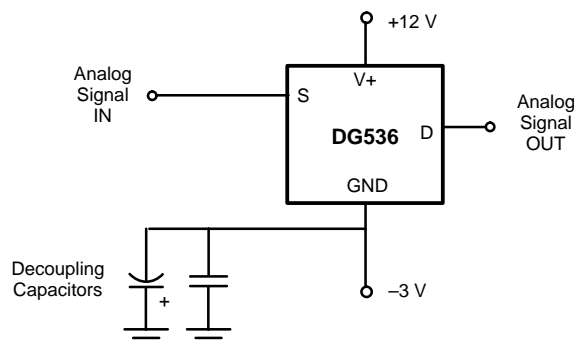


FIGURE 15. DG536 with Offset Supply

TTL to CMOS level shifting is easily obtained by using a MC14504B.

### Circuit Layout

Good circuit board layout and extensive shielding is essential for optimizing the high frequency performance of the DG536. Stray capacitances on the PC board and/or connecting leads will considerably degrade the ac performance. Hence, signal paths must be kept as short as practically possible, with extensive ground planes separating signal tracks.