National Semiconductor

MILITARY DATA SHEET

MNDS16F95-X REV 0A0

Original Creation Date: 01/26/96
Last Update Date: 01/30/96
Last Major Revision Date: 01/26/96

DIFFERENTIAL BUS TRANSCEIVER

General Description

The DS16F95 Differential Bus Transceiver is a monolithic integrated circuit designed for bidirectional data communication on balanced multipoint bus transmission lines. The Transceiver meets EIA standard RS-485 as well as RS-422A.

The DS16F95 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS16F95 features lower power, extended temperature range, and improved specifications.

The DS16F95 combines a TRI-STATE differential input line receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active Enable that can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or when Vcc = 0V. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive and negative current-limiting and thermal shutdown for protection from line fault conditions.

The DS16F95 can be used in transmission line applications employing the DS96F172 and DS96F174 quad differential line drivers and the DS96F173 and DS96F175 quad differential line receivers.

Industry Part Number

DS16F95

NS Part Numbers

DS16F95E/883 *
DS16F95J/883 **
DS16F95W-SMD ***
DS16F95W/883

Prime Die

M176

Controlling Document

5962-89615012A*,PA**,HA**

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Meets EIA Standard RS-422A and RS-485
- Meets SCSI specifications
- Designed for multipoint transmission
- Wide positive and negative input/output bus voltage ranges
- Thermal shutdown protection
- Driver positive and negative current-limiting
- High impedance receiver input
- Receiver input hysteresis of 50mV typical
- Operates from single 5.0V supply
- Low power 28mA max
- Pin compatible with DS3695 and SN75176A

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature Range	
Ceramic DIP	-65 C to +175 C
Lead Temperature	
Ceramic DIP (Soldering, 60 sec.)	300 C
Maximum Power Dissipation at 25 C (Note 2)	
Ceramic J Package	1300mW
Ceramic E Package	1800mW
Ceramic W Package	TBD
Supply Voltage	7.0V
Differential Input Voltage	+15V/-10V
Enable Input Voltage	5.5V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: *Derate J package 8.7mW/ C above 25 C. *Derate E package 8.7mW/ C above 25 C. *Derate W package 12.5mW/ C above 25 C.

Recommended Operating Conditions

	Min.	Typ.	Max.	Units
Supply Voltage (Vcc)	4.5	5.0	5.50	V
Voltage at Any Bus Terminal (Separately or Common Mode) (Vi or Vcm)	-7.0		12	V
Differential Input Voltage (Vid)	-7.0		±12	V
Output Current HIGH (Ioh)	Min.	Typ.	Max.	Units
Driver			-60	mA
Receiver			-400	uA
Output Current LOW (Iol)	Min.	Typ.	Max.	Units
Driver			60	mA
Receiver			16	mA
Operating Temperature (TA)	Min.	Typ.	Max.	Units
	-55	+25	+125	C

Electrical Characteristics

DC PARAMETES: ELECTRICAL CHARACTERISTICS FOR DRIVER

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5.5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vod1	Differential Vout	Vcc = 5.5V, Io = 0A, Vin = .8V				6	V	1, 2, 3
		Vcc = 5.5V, Io = 0A, Vin = 2V				6	V	1, 2, 3
Vod2	Differential Vout	Vcc = 4.5V, RL = 100 Ohms			2		V	1, 2, 3
		Vcc = 4.5V, RL = 54 Ohms			1.5		V	1, 2, 3
Delta Vod	Change In Differential Vout	Vcc = 4.5V, RL = 100 Ohms	1		-200	200	mV	1, 2, 3
		Vcc = 4.5V, RL = 54 Ohms	1		-200	200	mV	1, 2, 3
Delta Voc	Change In Common Mode Vout	Vcc = 4.5V, RL = 100 Ohms	1		-200	200	mV	1, 2, 3
		Vcc = 4.5V, RL = 54 Ohms	1		-200	200	mV	1, 2, 3
Voc	Common Mode Vout	RL = 100 Ohms				3	V	1, 2, 3
		RL = 54 Ohms				3	V	1, 2, 3
Iih	Logical "1" Input Current	Vi = 2.4V				20	uA	1, 2, 3
Io	Output Current	Output Disable, Vo = 12V				1	mA	1, 2, 3
		Output Disable, Vo = -7V	2		-.8		mA	1, 2, 3
		Vcc = 0, Output Disable, Vo = 12V				1	mA	1, 2, 3
		Vcc = 0, Output Disable, Vo = -7V	2		-.8		mA	1, 2, 3

Electrical Characteristics

DC PARAMETES: ELECTRICAL CHARACTERISTICS FOR DRIVER(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5.5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ios	Output Short Circuit	Vin = 3V, Vout = Vcc				150	mA	1, 2, 3
		Vin = 3V, Vout = -7V	2		-250		mA	1, 2, 3
		Vin = 3V, Vout = 0V	2		-150		mA	1, 2, 3
		Vin = 3V, Vout = 12V				250	mA	1, 2, 3
		Vin = 0V, Vout = 12V				250	mA	1, 2, 3
		Vin = 0V, Vout = Vcc				150	mA	1, 2, 3
		Vin = 0V, Vout = -7V	2		-250		mA	1, 2, 3
		Vin = 0V, Vout = 0V	2		-150		mA	1, 2, 3
Voh	Logical "1" Output Voltage	Vcc = 4.5V, Io = -20mA			3		V	1, 2, 3
Vol	Logical "0" Output Voltage	Vcc = 4.5V, Io = 20mA				2	V	1, 2, 3
Vod3	Differential Vout	Vcm = -7V to 12V			1		V	1, 2, 3

Electrical Characteristics

DC PARAMETES: ELECTRICAL CHARACTERISTICS FOR RECEIVER

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5.5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Voh	Logical "1" Output Voltage	Vcc = 4.5V, Vid = 200mV, Ioh = -400uA			2.5		V	1, 2, 3
Vol	Logical "0" Output Voltage	Vcc = 4.5V, Vid = -200mV, Iol = 8mA				.45	V	1, 2, 3
		Vcc = 4.5V, Vid = -200mV, Iol = 16mA				.5	V	1, 2, 3
Ii	Line Input Current	Untested Input = 0V, Vi = 12V				1	mA	1, 2, 3
		Untested Input = 0V, Vi = -7V	2		-.8		mA	1, 2, 3
		Vcc = 0V, Untested Input = 0V, Vi = 12V	2			1	mA	1, 2, 3
		Vcc = 0V, Untested Input = 0V, Vi = -7V			-.8		mA	1, 2, 3
Iih	Logical "1" Input Current	Vi = 2.7V (Receiver)				20	uA	1, 2, 3
Rin	Input Resistance	Untested Input = 0V, Vi = 12V	3		10		K Ohms	1, 2, 3
		Untested Input = 0V, Vi = -7V	3		10		K Ohms	1, 2, 3
		Vcc = 0V, Untested Input = 0V, Vi = 12V	3		10		K Ohms	1, 2, 3
		Vcc = 0V, Untested Input = 0V, Vi = -7V	3		10		K Ohms	1, 2, 3
Ioz	High Impedance State	Vi = .4V			-20	20	uA	1, 2, 3
		Vi = 2.4V			-20	20	uA	1, 2, 3
Ios	Output Short Circuit	Vin = 1V, Vout = 0V			-85	-15	mA	1, 2, 3
Vth	Differential Input High Threshold	Vcc = 4.5V, Vo = 2.5V, Vcm = 12V & 0V & -7V, Io = -.4mA				.2	V	1, 2, 3
		Vcc = 5.5V, Vo = 2.5V, Vcm = 12V & 0V & -7V, Io = -.4mA				.2	V	1, 2, 3
Vtl	Differential Input Low Threshold	Vcc = 4.5V, Vo = .5V, Vcm = 12V & 0V & -7V, Io = 8mA			-.2		V	1, 2, 3
		Vcc = 5.5V, Vo = .5V, Vcm = 12V & 0V & -7V, Io = 8mA			-.2		V	1, 2, 3

Electrical Characteristics

DC PARAMETES: ELECTRICAL CHARACTERISTICS FOR RECEIVER(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5.5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vth+ - (Vth-)	Hyteresis	Vcc = 4.5V, Vcm = 0V			35		mV	1, 2, 3
		Vcc = 5.5V, Vcm = 0V			35		mV	1, 2, 3

DC: ELECTRICAL CHARACTERISTICS FOR BOTH DRIVER AND RECEIVER

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5.5V

Icc	Supply Current Icc Both Disable	Re = 2V, De = .8V				25	mA	1, 2, 3
Icc	Supply Current Icc Both Enable	Re =.8V, De = 2V				28	mA	1, 2, 3
Vic	Input Clamp Volt	Ii = -18mA			-1.3		V	1, 2, 3
Vih	Logical "1" Input Voltage				2		V	1, 2, 3
Vil	Logical "0" Input Voltage					.8	V	1, 2, 3
Vih	Logical "1" Enable Input Voltage				2		V	1, 2, 3
Vil	Logical "0" Enable Input Voltage					.8	V	1, 2, 3
Iil	Logical "0" Input Current	Vi = .4V	2		-50		uA	1, 2, 3

Electrical Characteristics

AC PARAMETERS: ELECTRICAL CHARACTERISTICS OF DRIVER

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V, PRR = 1MHz, Tr ≤ Tf ≤ 6nS, 50% duty cycle, AMP = 3V, VLo = 0V, Zout = 50 Ohms

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tdd	Differential Output Delay Time	RL = 60 Ohms	6		8	25	nS	9
			6		8	30	nS	10, 11
tTD	Differential Output Transition Time	RL = 60 Ohms	5, 6		8	25	nS	9
			5, 6		8	30	nS	10, 11
tPLH	Propagation Delay Time Low to High	RL = 27 Ohms			6	18	nS	9
					6	25	nS	10, 11
tPHL	Propagation Delay Time high to Low	RL = 27 Ohms			6	18	nS	9
					6	25	nS	10, 11
tPZH	Output Enable Time to H	RL = 110 Ohms				35	nS	9
						45	nS	10, 11
tPZL	Output Enable Time to L	RL = 110 Ohms				40	nS	9
						50	nS	10, 11
tPHZ	Output Disable Time to H	RL = 110 Ohms				30	nS	9
						40	nS	10, 11
tPLZ	Output Disable Time to L	RL = 110 Ohms				30	nS	9
						40	nS	10, 11
Tskew	Differentail Output Skew Time					6	nS	9
						12	nS	10, 11

Electrical Characteristics

AC PARAMETERS: ELECTRICAL CHARACTERISTICS OF RECEIVER

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V, PRR = 1MHz, Tr ≤ Tf ≤ 6nS, 50% duty cycle, AMP = 3V, VLo = 0V, Zout = 50 Ohms

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPLH	Propagation Delay Time Low to High	Cl = 15pF			10	27	nS	9
					10	38	nS	10, 11
tPHL	Propagation Delay Time High to Low	Cl = 15pF			10	27	nS	9
					10	38	nS	10, 11
tPZH	Output Enable Time to H	Cl = 15pF				20	nS	9
						30	nS	10, 11
tPZL	Output Enable Time to L	Cl = 15pF				20	nS	9
						30	nS	10, 11
|tPLH - tPHL|	Output to Output Delay Time					8	nS	9
						16	nS	10, 11
tPHZ	Output Disable Time From H	Cl = 20pF	4			30	nS	9
			4			40	nS	10, 11
		Cl = 5pF	4			20	nS	9
			4			30	nS	10, 11
tPLZ	Output Disable Time From L	Cl = 5pF				20	nS	9
						30	nS	10, 11

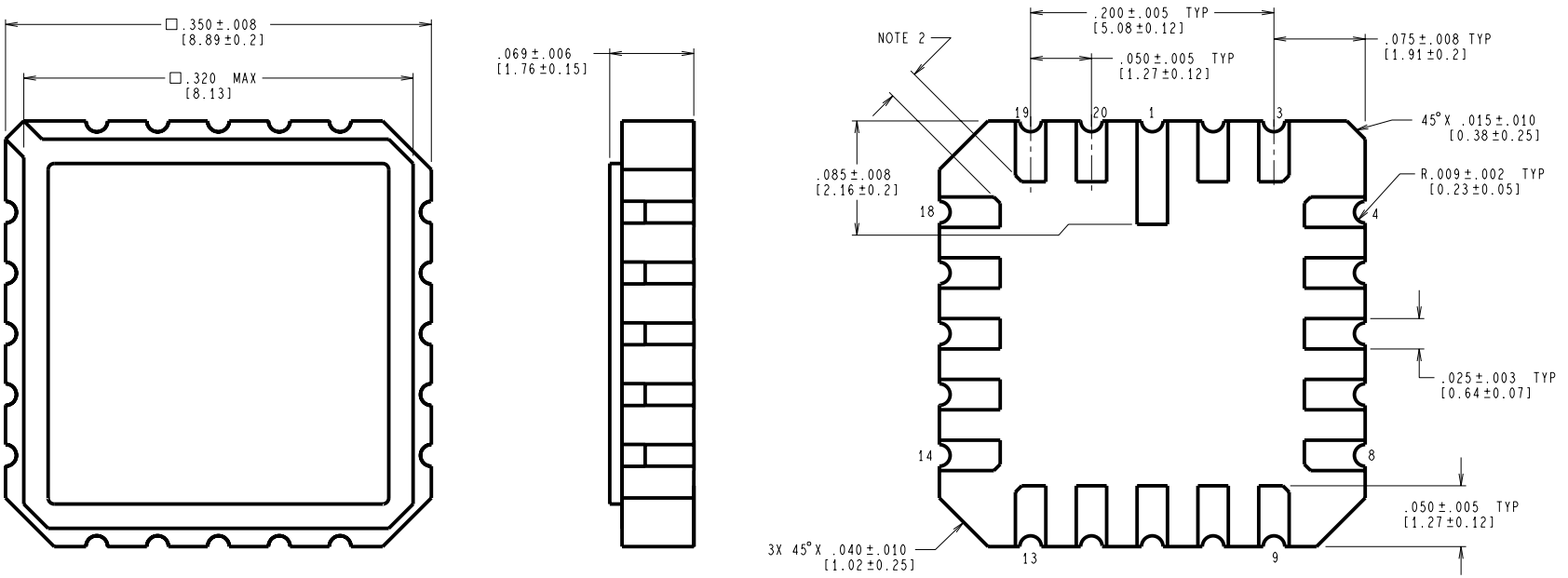
Note 1: Delta Vod and Delta Voc are the changes in magnitude of Vod and Voc.
Note 2: Negative sign of the limits indicates the direction of the current flow only.
Note 3: Rin is guaranteed by testing "Line Input Current" (II).
Note 4: Testing at 20pF assures conformance to spec at 5pF.
Note 5: tTD = Non-inverting output rise time + inverting output fall time / 2, Non-inverting output fall time + inverting output rise time / 2.
Note 6: Rise time 20% to 80%, Fall time 80% to 20%

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
E20ARE	LDLESS CHIP CARRIER, TYPE C 20 TERMINAL(P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
W10ARG	CERPAC (W), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION
INCH [MM]

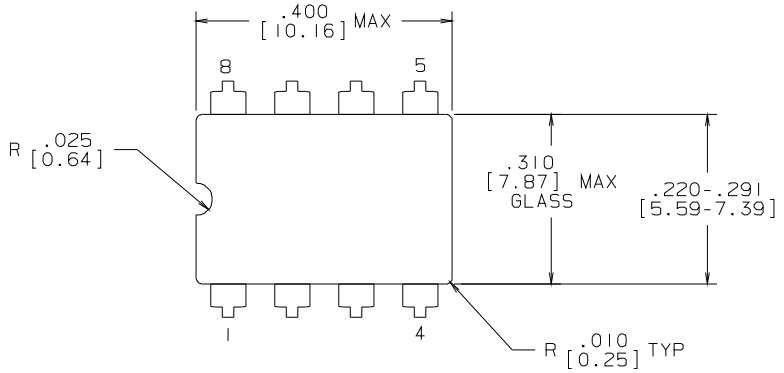
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

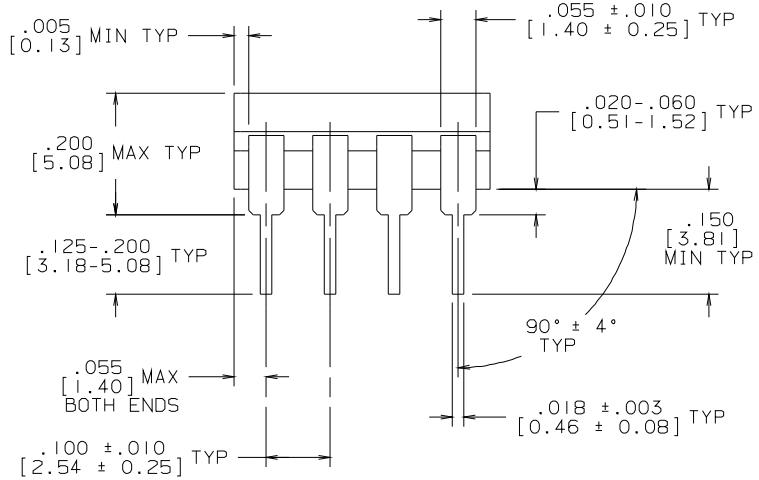
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

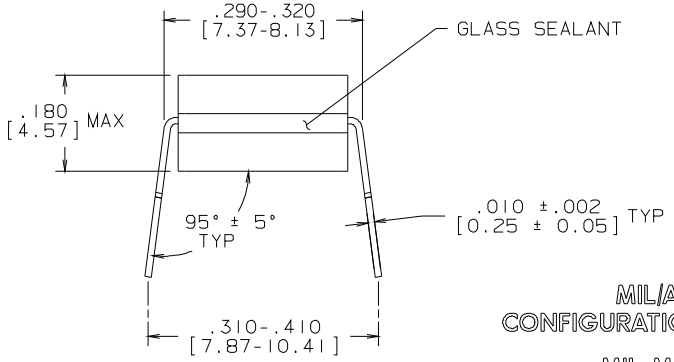
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

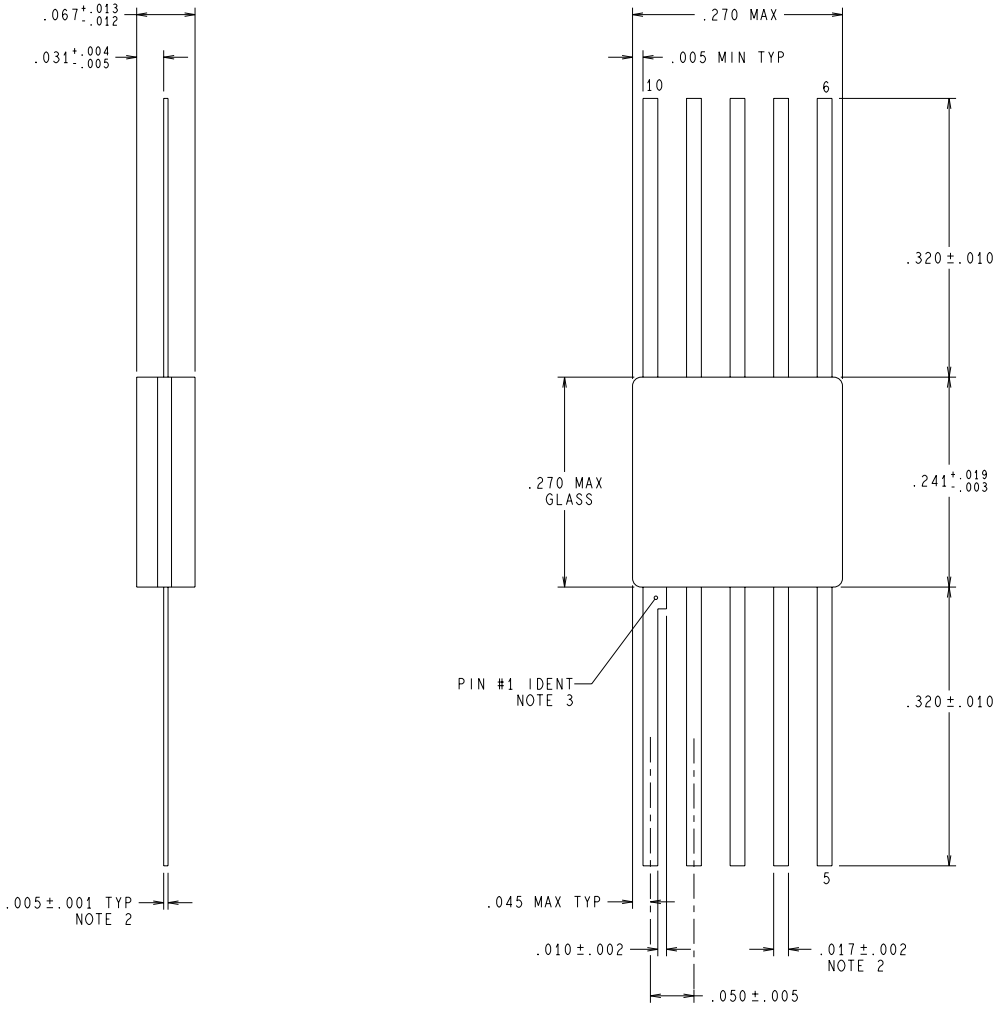
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE AND REDRAW PER NEW STANDARD.	10510	07/28/94	DEG/AEP
G	.017±.002 WAS .017±.020.	10654	10/21/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION MO-003, VARIATION AG, DATED 06/01/76.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: D.E.Grady	07/28/94
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 10 LEAD

PROJECTION — INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W10A	G

DO NOT SCALE DRAWING — SHEET 1 of 1