National Semiconductor

MILITARY DATA SHEET

MNDAC1054CM-X REV 0B0

Original Creation Date: 08/24/95
Last Update Date: 09/29/95
Last Major Revision Date: 08/24/95

QUAD 10-BIT VOLTAGE-OUTPUT SERIAL D/A CONVERTER WITH READBACK

General Description

The DAC1054 is a complete quad 10-bit voltage-output digital-to-analog converter that can operate on a single 5V supply. It includes on-chip output amplifiers, internal voltage reference, and serial microprocessor interface. By combining in one package the reference, amplifiers, and conversion circuitry for four D/A converters, the DAC1054 minimizes wiring and parts count and is hence ideally suited for applications where cost and board space are of prime concern.

The DAC1054 also has a data readback function, which can be used by the microprocessor to verify that the desired input word has been properly latched into the DAC1054's data registers. The data readback function simplifies the design and reduces the cost of systems which need to verify data integrity.

The logic comprises a MICROWIRE(TM)-compatible serial interface and control circuitry. The interface allows the user to write to any one of the input registers or to all four at once. The latching registers are double-buffered, consisting of 4 separate input registers and 4 DAC registers. Each DAC register may be written to individually. Double buffering allows all 4 DAC outputs to be updated simultaneously or individually.

The four reference inputs allow the user to configure the system to have a separate output voltage range for each DAC. The output voltage of each DAC can range between 0.3V and 2.8V and is a function of Vbias, Vref, and the input word.

Industry Part Number

DAC1054CMJ

NS Part Numbers

DAC1054CMJ-QML

Prime Die

DAC1054A

Controlling Document

5962-9466201QJA

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Single +5V supply operation
- MICROWIRE serial interface allows easy interface to many popular microcontrollers including the COPS(TM) and HPC(TM) families of microcontrollers
- Data readback capability
- Output data can be formatted to read back MSB or LSB first
- Versatile logic allows selective or global update of the DACs
- Power fail flag
- Output amplifiers can drive 2K Ohm load
- Synchronous/asynchronous update of the DAC outputs

Applications

- Automatic test equipment
- Industrial process controls
- Automotive controls and diagnostics
- Instrumentation

(Absolute Maximum Ratings)

(Note 1, 2)

Supply Voltage (AVcc, DVcc)	7V
Supply Voltage Difference (AVcc-DVcc)	±5.5V
Voltage at Any Pin (Note 3)	Gnd -0.3V to AVcc/DVcc +0.3V
Input Current at Any Pin (Note 3)	5mA
Package Input Current (Note 4)	30mA
Power Dissipation (Note 5)	950mW
ESD Susceptibility (Note 6)	
Human Body Model	2000V
Soldering Information (10 Sec.)	300 C
Storage Temperature	-65 C to +150 C
Maximum Junction Temperature	150 C
Thermal Resistance	
ThetaJA	
(Still Air)	41 C/W
(500LF/Min Air flow)	22 C/W
ThetaJC	3.0 C/W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Converter Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to ground, unless otherwise specified.

Note 3: When the input voltage (Vin) at any pin exceeds the power supply rails (Vin<Gnd or Vin>V+) the absolute value of current at that pin should be limited to 5mA or less.

Note 4: The sum of the currents at all pins that are driven beyond the power supply voltages should not exceed 30mA.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax-TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 6: Human body model, 100pF discharged through a 1.5K Ohm resistor.

Recommended Operating Conditions

(Note 1, 2)

Supply Voltage	4.5V to 5.5V
Supply Voltage Difference (AVcc-DVcc)	±1V
Temperature Range	Tmin <TA< Tmax -55 C <TA< +125 C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Converter Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to ground, unless otherwise specified.

Electrical Characteristics

DC PARAMETERS: STATIC CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vref = 2.65V, AVcc = DVcc = 5V, VBias = 1.4V, Rl = 2K Ohms, fCLK = 10MHz, Rl = The load resistors on the analog output pins Vout1, Vout2, Vout3, Vout4.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
n	Resolution					10	bits	1, 2, 3
	Monotonicity		1			10	bits	1, 2, 3
	Integral Linearity Error		2		-1.0	1.0	LSB	1, 2, 3
	Differential Linearity Error				-1.0	1.0	LSB	1, 2, 3
	Fullscale Error		3		-30	30	mV	1, 2, 3
	Zero Error		4		-25	25	mV	1, 2, 3
	Power Supply Sensitivity		5			-34	dB	1, 2, 3

DC PARAMETERS: DIGITAL CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vref = 2.65V, AVcc = DVcc = 5V, VBias = 1.4V, Rl = 2K Ohms, fCLK = 10MHz, Rl = The load resistors on the analog output pins Vout1, Vout2, Vout3, Vout4.

Vin(1)	Logical "1" Input Voltage	AVcc = DVcc = 5.5V			2.0		V	1, 2, 3
Vin(0)	Logical "0" Input Voltage	AVcc = DVcc = 4.5V				.8	V	1, 2, 3
Iil	Digital Input Leakage Current					5.0	uA	1, 2, 3
Vout(1)	Logical "1" Output Voltage	Isource = 0.8mA			2.4		V	1, 2, 3
Vout(0)	Logical "0" Output Voltage	Isink = 3.2mA				.4	V	1, 2, 3
Vint	Interrupt Pin Output Voltage	10K Ohms Pullup				.4	V	1, 2, 3
Is	Supply Current	Outputs Unloaded				20.0	mA	1, 2, 3

DC PARAMETERS: REFERENCE INPUT CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vref = 2.65V, AVcc = DVcc = 5V, VBias = 1.4V, Rl = 2K Ohms, fCLK = 10MHz, Rl = The load resistors on the analog output pins Vout1, Vout2, Vout3, Vout4.

Rref	Input Resistance				4	10	KOhms	1, 2, 3

Electrical Characteristics

DC PARAMETERS: BANDGAP REFERENCE CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vref = 2.65V, AVcc = DVcc = 5V, VBias = 1.4V, Rl = 2K Ohms, fCLK = 10MHz, Cl = 220uF, Rl = The load resistors on the analog output pins Vout1, Vout2, Vout3, Vout4.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
VrefOUT	Output Voltage		6		2.597	2.703	V	1, 2, 3
	Line Regulation	4.5V < Vcc < 5.5V, Il = 4mA				5	mV	1, 2, 3
Delta Vref/ Delta Il	Load Regulation	0 < IL < 4mA				10	mV	1, 2, 3

DC PARAMETERS: DYNAMIC CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vref = 2.65V, AVcc = DVcc = 5V, VBias = 1.4V, Rl = 2K Ohms, fCLK = 10MHz, Rl = The load resistors on the analog output pins Vout1, Vout2, Vout3, Vout4.

tS+	Positive Voltage Output Settling Time	Cl = 200pF	7			3.2	uS	4, 5, 6
tS-	Negative Voltage Output Settling Time	Cl = 200pF	7			3.7	uS	4, 5, 6

Electrical Characteristics

AC PARAMETERS: AC ELECTRICAL CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: AVcc = DVcc = 5V, Vref = 2.65V, VBias = 1.4V, Rl = 2K Ohms, fCLK = 10MHz, Rl = The load resistors on the analog output pins Vout1, Vout2, Vout3, Vout4.

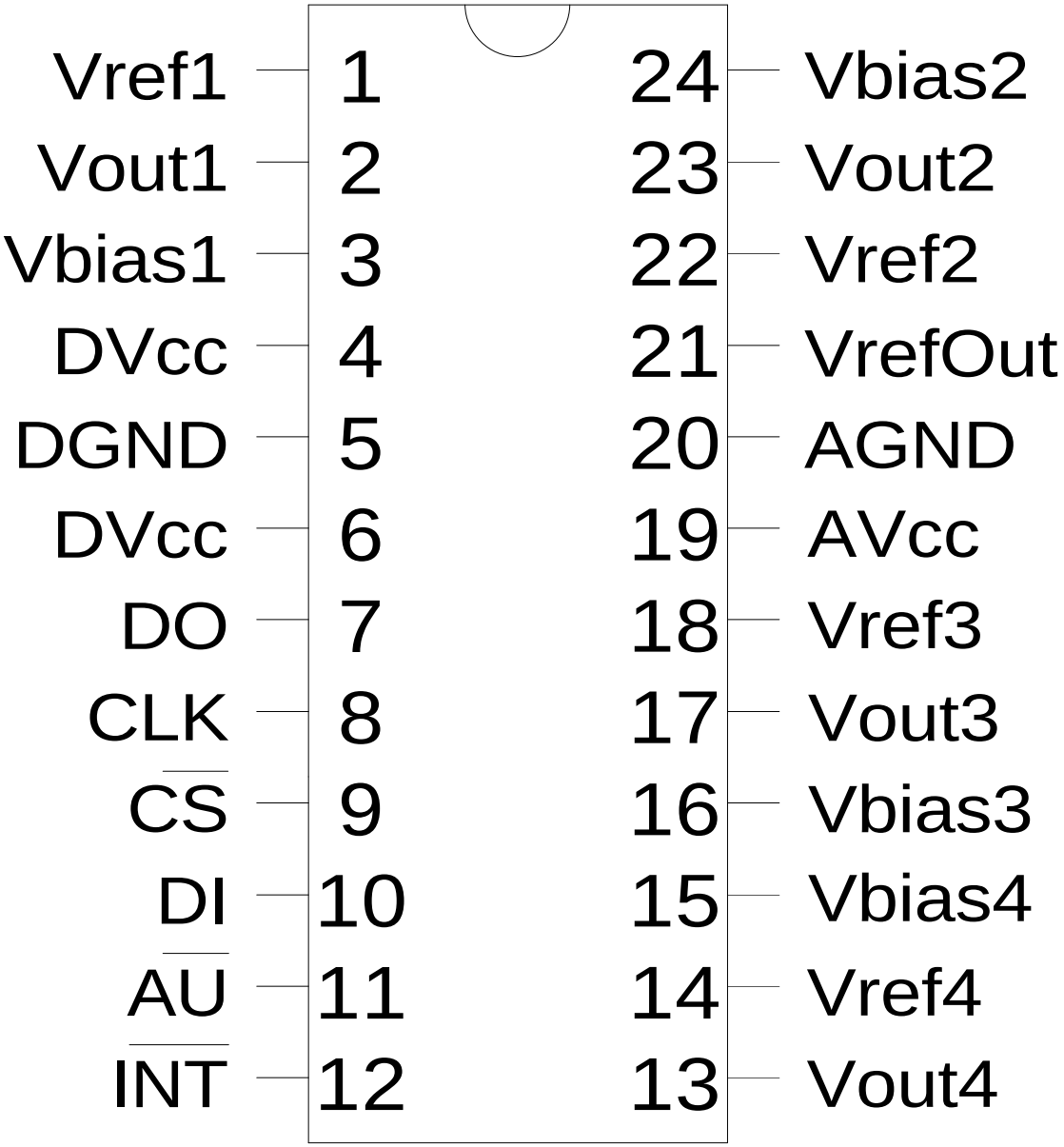
SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tDS	Data SETUP Time				15		nS	9, 10, 11
tDH	Data HOLD Time				0		nS	9, 10, 11
tCS	Control SETUP Time				15		nS	9, 10, 11
tCH	Control HOLD Time				0		nS	9, 10, 11
fWMAX	Clock Frequency Write					10	MHz	9, 10, 11
fRMAX	Clock Frequency Readback					5	MHz	9, 10, 11
tH	Minimum Clock High Time				20		nS	9, 10, 11
tL	Minimum Clock Low Time				20		nS	9, 10, 11
tCZ1	Output Hi-Z to Valid 1	fCLK = 5MHz				70	nS	9, 10, 11
tCZ0	Output Hi-Z to Valid 0	fCLK = 5MHz				70	nS	9, 10, 11
t1H	$\overline{CS}$ to Output Hi-Z	10K Ohms with 60pF, fCLK = 5MHz				150	nS	9, 10, 11
t0H	$\overline{CS}$ to Output Hi-Z	10K Ohms with 60pF, fCLK = 5MHz				130	nS	9, 10, 11

Note 1: A monotonicity of 10 bits for the DAC1054 means that the output voltage changes in the same direction (or remains constant) for each increase in the input code.
Note 2: Integral linearity error is the maximum deviation of the output from the line drawn between zero and full-scale (excluding the effects of zero error and full-scale error).
Note 3: Full-scale error is measured as the deviation from the ideal 2.800V full-scale output when Vref=2.650V and Vbias=1.400V.
Note 4: Zero error is measured as the deviation from the ideal 0.302V output when Vref=2.650V, Vbias=1.400V, and the digital input word is all zeros.
Note 5: Power Supply Sensitivity is the maximum change in the offset error or the full-scale error when the power supply differs from its optimum 5V by up to 0.50V (10%), load resistor Rl = 2K Ohms.
Note 6: Limit = $\pm$2%
Note 7: Positive or negative settling time is defined as the time taken for the output of the DAC to settle to its final full-scale or zero output to within $\pm$0.5LSB. This time shall be referenced to the 50% point of the positive edge of $\overline{CS}$, which initiates the update of the analog outputs.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
6304HRA1	24 LEAD CERDIP (J) (B/I CKT)
J24ARH	(blank)
P000003A	24 LEAD CERDIP (J) (PIN OUT)

See attached graphics following this page.



DAC1054CMJ/883
CONNECTION DIAGRAM
24 - LEAD DIP
(TOP VIEW)
P000003A