2 Channel DDX Controller

FEATURES

- DIGITAL VOLUME CONTROL
- ANTI-CLIPPING
- AUTOMATIC MUTE
- TWO CHANNEL DDX OUTPUTS
- ALL DIGITAL - NEEDS NO DAC

APPLICATIONS

- DIGITAL POWERED SPEAKERS
- PC SOUND CARDS
- CAR AUDIO
- SURROUND SOUND SYSTEMS
- DIGITAL AUDIO COMPONENTS

GENERAL DESCRIPTION

The DDX-2000 Controller includes two channels of DDX processing, digital volume control, mute and special processing to reduce distortion associated with signal clipping. A system formed by adding the DDX-2060 can provide up to 35 Watts per channel of audio power at very low distortion and very high efficiency. The controller accepts standard PCM serial formats and operates from an external 256*Fs clock or from a crystal.

The benefits of the DDX-2000/2060 audio amplifier system include an all-digital design that eliminates the need for a digital to analog converter (DAC) and the high efficiency, low distortion operation derived from the use of Apogee's patented damped ternary pulse width modulation (PWM). This approach provides an efficiency advantage over conventional Class-D designs and up to three times the efficiency of typical Class A/B amplifiers with music input signals.

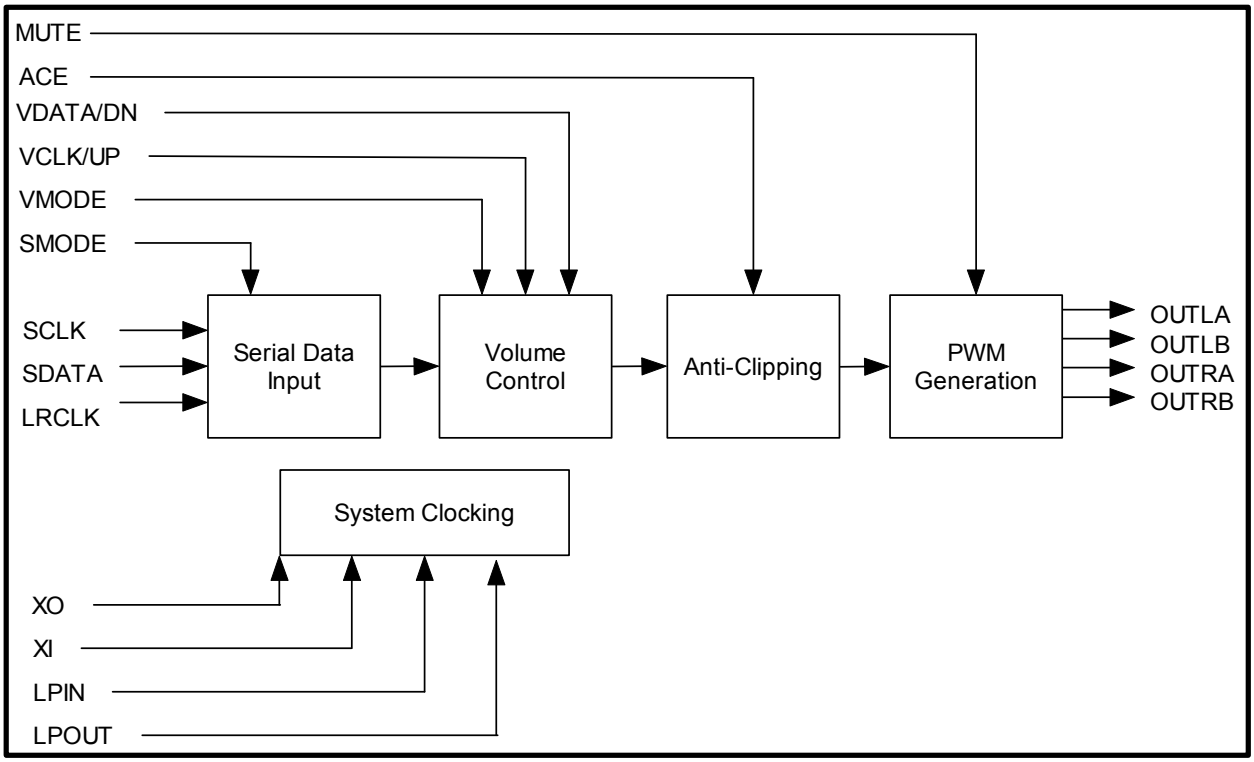


Figure 1. DDX-2000 Block Diagram

Absolute Maximum Ratings [Note 1]

SYMBOL	PARAMETER	VALUE	UNIT
VL	Power supply voltage	-0.3V to +4.6V	V
Note [Note 2]	Logic Inputs	-0.3V to +6.0V	V
Tstg	Storage temperature range	-40 to +150	°C

Recommended Operating Conditions [Note 3]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VL	Power supply voltage	3.0	3.3	3.6	V
VIH [Note 2]	Logic inputs, High	2.0		5.5	V
VIL	Logic inputs, Low	0		0.8	V
Fs	PCM Input Sample Rate	32		48	kHz
T_A	Ambient Temperature	0		70	°C

Thermal Data

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
θ_{JA}	Thermal resistance junction-ambient			110	°C/W

Electrical Characteristics

Refer to circuit Fig. 5 Ta=25C

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_L	VL supply current for DDX-2000	VL= +3.3V		90	100	mA

Volume Pins: Setup and Hold Times

Refer to circuit Fig. 4 Ta=25C

SIGNAL	SETUP TO:	CONDITION	MIN	TYP	MAX	UNIT
VDATA	VCLK	VL= +3.3V	50			ns
VDATA	VMODE		75			ns
	HOLD FROM:					
VDATA	VCLK		25			ns
VDATA	VMODE		75			ns
VCLK	VMODE		75			ns

External Clock

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
	Master Clock (XI) Jitter				400	ps_{pp}
	Sample Frequency Mismatch				0.2	%

Note 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: SCLK, SDATA, LRCLK, VMODE, VCLK/UP, VDATA/DN, SMODE, nRST, ACE and MUTE are 5V input tolerant.

Note 3: Performance not guaranteed beyond recommended operating conditions.

DDX-2000 Pin Function Description

Audio Serial Interface (I^2S)

Pin Name	Pin No.	Description
SCLK [Note 4]	1	Input serial clock
SDATA [Note 4]	2	Input serial data
LRCLK [Note 4,Note 5]	3	Input Left/Right
SMODE [Note 4, Note 5]	20	Serial Mode Select (0=Left Justified, 1= I^2S. See Figure 8)

Gain/Volume Interface

Pin Name	Pin No.	Description
VMODE [Note 4, Note 5]	39	Volume Mode Select (0 = serial, 1= toggle)
VCLK/UP [Note 4, Note 5]	40	Volume Data Clock or Increment Up
VDATA/DN[Note 4, Note 5]	41	Volume Serial Data In or Increment Down
ACE [Note 4, Note 5]	5	Anti-Clipping Enable, Active Hi

System Clocking

Pin Name	Pin No.	Description
XI	11	256*fs Oscillator/External 256*fs clock input
XO	10	256*fs Oscillator
INLP	16	PLL Filter
OUTLP	17	PLL Filter

DDX Output Signals/Control

Pin Name	Pin No.	Description
MUTE [Note 4, Note 6]	38	Active Hi, sets outputs to damped state
OUTLA	33	Left channel output A
OUTLB	32	Left channel output B
OUTRA	26	Right channel output A
OUTRB	25	Right channel output B

Power Supplies/Miscellaneous

Pin Name	Pin No.	Description
VL	4, 13, 15, 27, 29, 44	Power
GND	9, 12, 14, 18, 19, 28, 34, 35, 37, 42, 43	Ground
nRST [Note 4, Note 5, Note 7]	6, 7	System Reset, active low. Both pins must be connected for proper operation.
NC	8, 21, 22, 23, 24, 30, 31, 36	No Connect. Must be left open.

Note 4: Denotes 5V input tolerance.
Note 5: Denotes 50k internal pullup.
Note 6: Denotes 50k internal pulldown.
Note 7: Denotes TTL Schmitt Input Buffer. Vt+ = 2.0V max. Vt- = 0.7V min. Typical hysteresis is 0.5V.

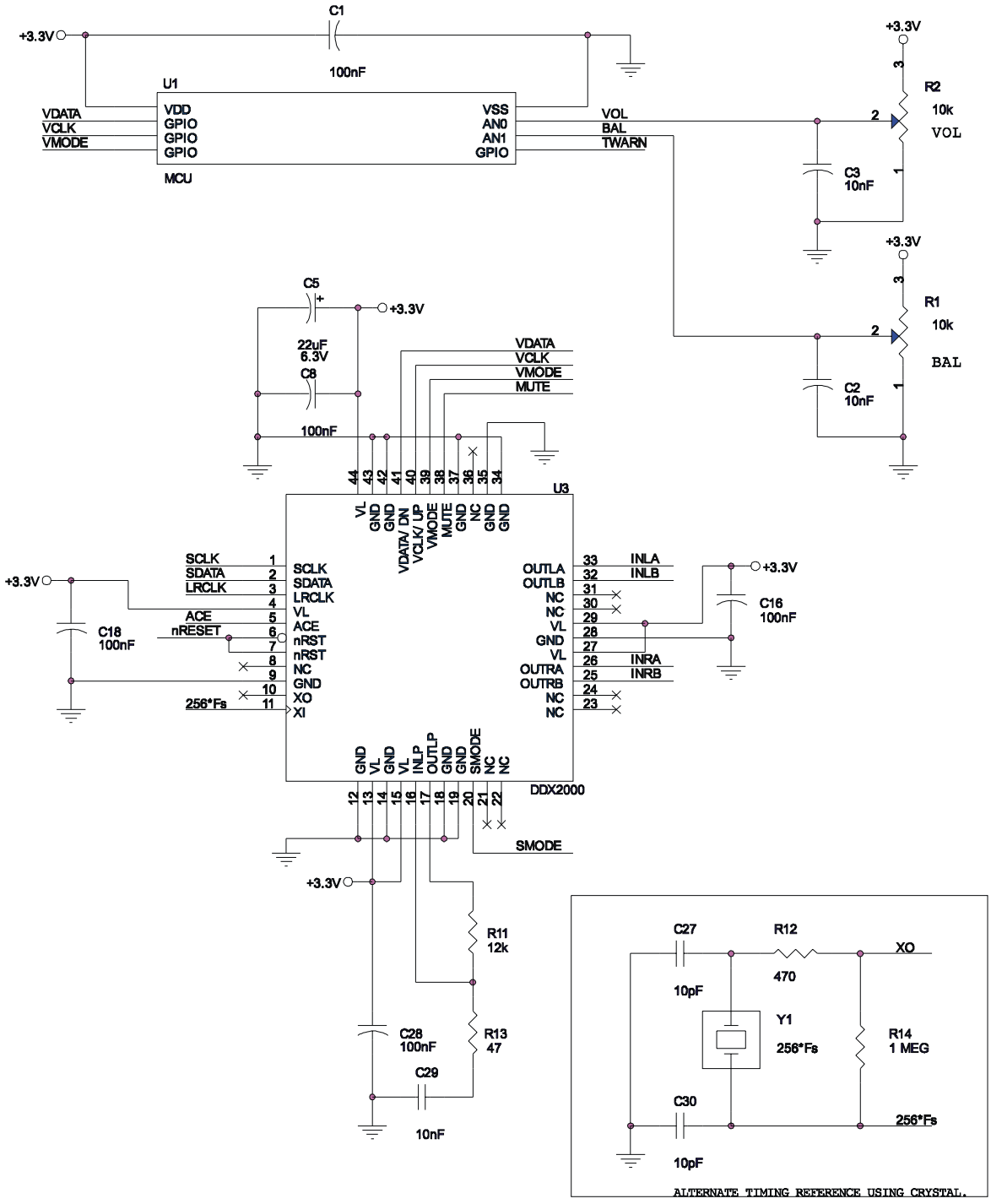


Figure 2. Typical Application Circuit (Signal Processing section)

Typical Performance Characteristics using
DDX-2060 Power Device at Vcc = 28V, 8 Ohm load.

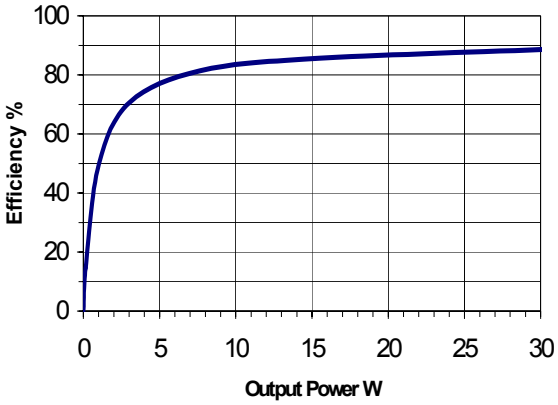


Figure 3. Efficiency vs. Output Power

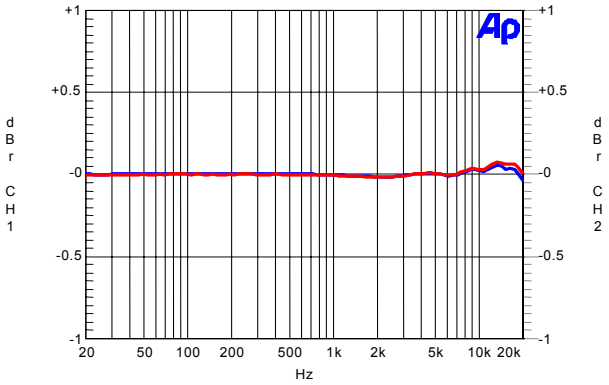


Figure 4. Frequency response

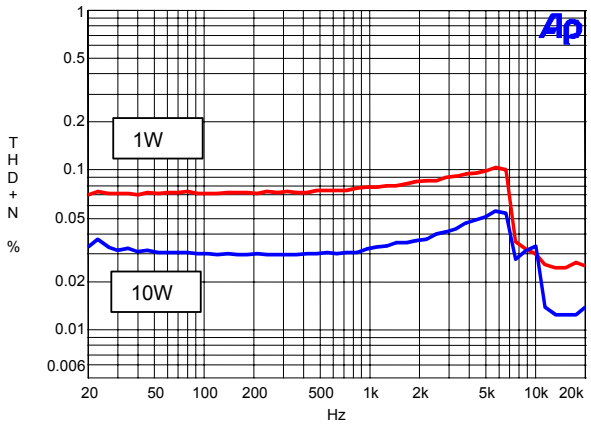


Figure 5. THD+N vs. Frequency

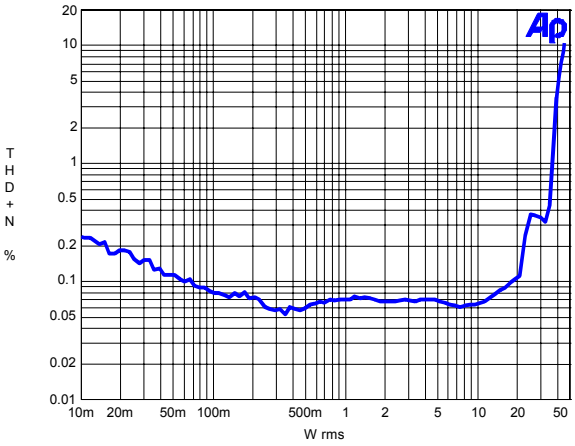


Figure 6. THD+N vs. output power at 1 KHz (w/ ANTICLIPPING DISABLED)

DDX-2000 CONTROLLER

The DDX-2000 Controller is a 3.3V digital integrated circuit that converts serial PCM digital audio signals into Apogee's patented damped ternary outputs. The device supports two modes of digital volume control, mute and anti-clipping functions. A block diagram of the device is shown in .

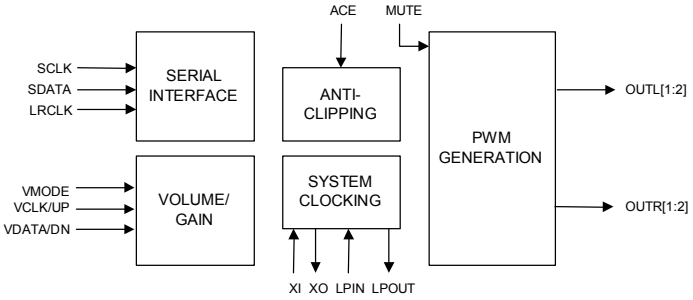


Figure 7. DDX-2000 Functional Diagram

Serial Interface

The DDX-2000 serial audio data input was designed to interface with standard digital audio components such as S/PDIF receivers, surround sound decoders and digital signal processors. Serial data input is controlled by three input pins: serial clock (SCLK), serial data (SDATA), and left/right clock (LRCLK) in either I^2S or left justified formats as controlled by the serial mode pin (SMODE). The serial data formats and timing diagram are shown in Figure 8. The DDX-2000 utilizes serial data words of 16 bits and accepts data words up to 24 bits.

Volume Interface

The volume level of the DDX2000 PWM outputs can be adjusted by setting the left and right volume registers (VOLL and VOLR). These registers are seven bits with a step size of approximately -0.75dB providing an adjustment range of –82.5dB to +12.0dB. Table 1 shows the volume level as a function of the register values. Following power-on-reset both volume registers are set to 0x26 or -15.75dB.

The volume registers, VOLL and VOLR, can be set with a serial data load using a micro-controller or similar device (serial mode) or by incrementing the volume register using control pins (toggle mode). This functionality is controlled using the volume mode select pin (VMODE) and two multifunction pins; volume clock/volume up (VCLK/UP) and the volume data/volume down (VDATA/DN).

Volume Register (VOLL, VOLR) hexadecimal	Volume (dB)
0x00, 0x80	+12.0
0x01, 0x81	+11.25
0x02, 0x82	+10.5
. . .	. . .
0x10, 0x90	0.0
0x11, 0x91	-0.75
0x12, 0x92	-1.5
. . .	. . .
0x7e, 0xfe	-82.5
0x7f, 0xff	Mute

Table 1. Volume Control

When the VMODE is logic-high (internally pulled-up) the device operates in toggle mode. The volume registers (both VOLL and VOLR) can be incremented either up or down by bringing the inputs VCLK/UP or VDATA/DN low. The volume register will increment at approximately 5 steps per second, for the first 1.4 seconds and then increase to approximately 10 steps per second until the upper or lower volume limits are reached or the input is released.

A serial mode volume change is initiated by bringing VMODE pin low. Serial data is input on VDATA/DN and is latched on the rising edge of the VCLK/UP input as shown in Figure 8. After all eight bits are received VMODE must be brought high to latch the volume register. Note, each channel volume register must be written independently (see Table 1).

For applications that provide digital volume control prior to the DDX-2000, the attenuation register can be set to 0dB by pulling both the VCLK/UP and VDATA/DN to ground, leaving VMODE high.

The DDX-2000 includes an anti-clipping function to improve audio quality when using the internal volume control set greater than 0dB. This function dynamically adjusts the volume level to significantly reduce distortion associated with signal clipping. This function is enabled by setting the anti-clipping enable (ACE) pin high. When enabled, the maximum distortion will be limited regardless of the volume. For applications where maximum power is desired, the ACE may be disabled and the output power and distortion will increase for volume settings which exceed 0dB.

System Clocking

The DDX-2000 operates from a master clock source whose frequency is 256 times the input LRCLK sample rate (256*fs). The device can accommodate sample rates from below 32 kHz to above 48 kHz. Either external clock sources or the built in oscillator may be used.

In designs that recover the clock (e.g., S/PDIF), the 256*fs output can be utilized for the master system clock to provide synchronous operation. For systems that operate asynchronously, i.e., the crystal clock is not exactly matched to the incoming serial data stream, the DDX-2000 will automatically accommodate sample frequency mismatch up to 0.2 %.

The accuracy of the master input clock will determine amplifier system performance. To meet the specified performance, random clock jitter must be less than 400pS p-p.

DDX Output Control

Asserting the MUTE input (logic-high), the DDX-2000 will command the zero state (load damping), which short-circuits the load to ground. The device also includes an automatic mute function which is activated upon receipt of 2048 consecutive zero data words on both the left and right serial inputs. Automatic transition from mute will occur on the first non-zero input word.

Performance Measurements

Class D amplifiers produce measurable switching noise outside the audio bandwidth. Apogee's DDX amplifier uses patented PWM modulation that significantly reduces the size of these products compared to typical Class D designs. However, in order to obtain accurate performance measurements in the audio bandwidth (i.e., 20Hz to 20kHz) additional filtering is required. The Typical Performance data was taken using a brick wall filter with a break frequency of 20kHz. This type of filter is often provided with audio measurement systems.

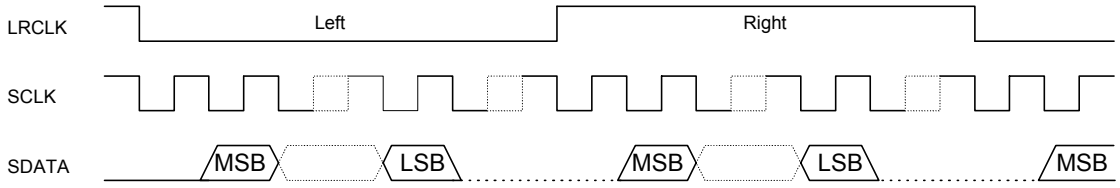
For More Information

More information is available at the DDX website (www.apogeeddx.com) such as:

- DDX Technology White Paper
- Testing DDX Amplifiers
- Thermal Design
- Power Supply Considerations
- EMI Considerations
- Reference Designs

INTERFACE TIMING

SMODE=1 I²S



SMODE=0 Left Justified

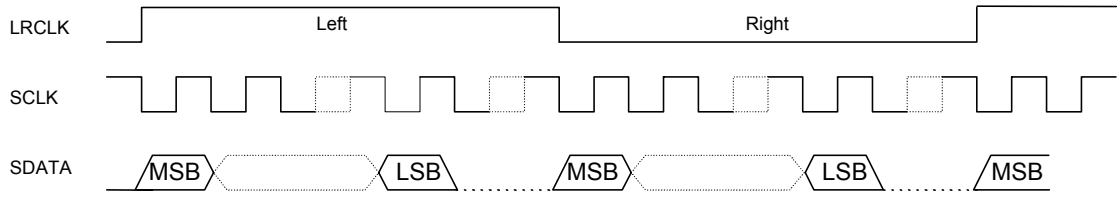
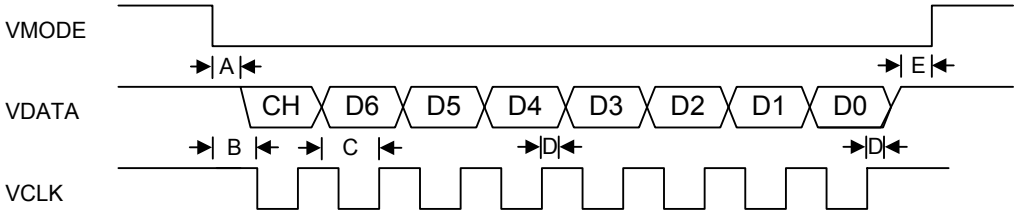


Figure 8. Audio Serial Interface

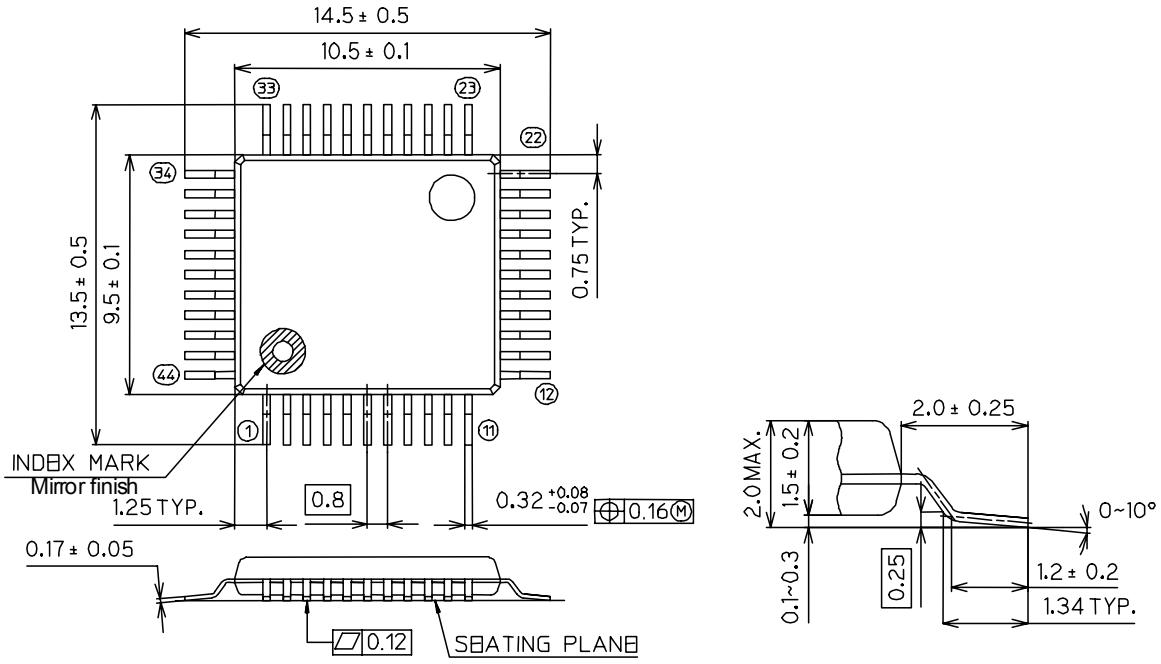


Notes:
- A) VDATA hold time from VMODE > 75 ns
- B) VCLK hold time from VMODE > 75 ns
- C) VDATA setup to VCLK > 50 ns
- D) VDATA hold from VCLK > 25 ns
- E) VDATA setup to VMODE > 75 ns
- F) VCLK HIGH TIME, CLK LOWTIME > 100 ns
- G) CH = Channel select. Left=0, Right=1.
- H) Volume register (MSB=D6, LSB=D0).

Figure 9. Serial Volume Load Timing

PHYSICAL DIMENSIONS

Dimensions shown in mm



DDX-2000 - 44 Pin Quad Plastic Flat Package