APOGEE TECHNOLOGY, INC.

DDX-8001

DDX® Multi-channel Digital Audio Processor

FEATURES

- 8 Channels of 24-Bit DDX®
- 100dB SNR and Dynamic Range
- 32kHz to 192kHz Input Sample Rates
- SACD/DSD Input (6 Channel)
- 24-bit to 36-bit Internal Processing
- Digital Gain/Attenuation +58dB to –100dB in 0.5dB steps
- Up to 10 Independent 32-bit User Programmable Biquads (EQ) per Channel
- I²C Control
- 8 Channel I²S Inputs and Outputs
- 3.3V Single Supply Operation
- Individual Channel, Master, and Channel Trim Gain/Attenuation
- Bass/Treble Tone Control
- Dual 8-Input Mix, Pre and Post EQ, per channel
- Dual Independent Programmable Limiters/Compressors
- Automodes™
  - * 5-Band Graphic EQ
  - * 32 Preset EQ Curves
  - * All 5.1 Bass Management Configs
  - * 8 Preset Crossover Filters
  - * Auto Volume Controlled Loudness
  - * 5.1 to 2 Channel Downmix
  - * 3 Preset Volume Curves
  - * 2 Preset Anti-Clipping Modes
  - * Preset Nighttime Listening Mode
  - * Preset TV AGC
- Input and I²S Output Channel Mapping
- AM Noise Reduction and PWM Frequency Shifting Modes
- Soft Volume and Muting
- Auto Zero Detect and Invalid Input Detect Muting
- Selectable DDX® Ternary or Binary PWM output + Variable PWM Speeds
- Internal Processing Loop-Through For Up To 40 Biquads / 2-Channels
- QSurround5.1*

* Provided only under License of QSound Labs, Inc.

1.0 GENERAL DESCRIPTION

The DDX-8001 is a single chip solution for digital audio processing and digital amplifier control, featuring output capabilities for DDX® (Direct Digital Amplification). In conjunction with a DDX® power device, it provides high-quality, high-efficiency, all digital amplification. The device is extremely versatile allowing for input of nearly all digital formats including 6.1/7.1 channel, 192kHz/24-bit DVD-Audio, and SACD. In 5.1 applications the additional two channels can be used for line-out or headphone drive.

Also provided in the DDX-8001 are a full assortment of digital processing features. This includes up to 10 programmable 32-bit biquads (EQ) per channel, bass/treble tone control, and dual 8-input mixing blocks per channel. Automodes™ enable a time-to-market advantage by substantially reducing the amount of software development needed for certain functions. This includes all possible 5.1 bass management configurations with simple large/small/off control settings. New advanced AM radio mode solves one of the most common concerns using switching power amplifiers.

The serial audio data input and output interfaces accept all possible formats, including the popular I²S format. Eight channels of DDX® processing are provided with capabilities of controlling the output switching frequency or modulation. This high quality conversion from PCM audio to DDX's patented tri-state PWM switching waveform provides over 100dB SNR and dynamic range.

The DDX-8001 is a 4th generation DDX® controller and is uniquely suited for the most demanding applications, providing an audiophile experience without parallel.

129 Morgan Drive, Norwood, MA 02062 voice: (781) 551-9450 fax: (781) 440-9528 email: apogee@apogeeddx.com

Table of Contents

Table of Figures

129 Morgan Drive, Norwood, MA 02062 voice: (781) 551-9450 fax: (781) 440-9528 email: apogee@apogeeddx.com

List of Tables

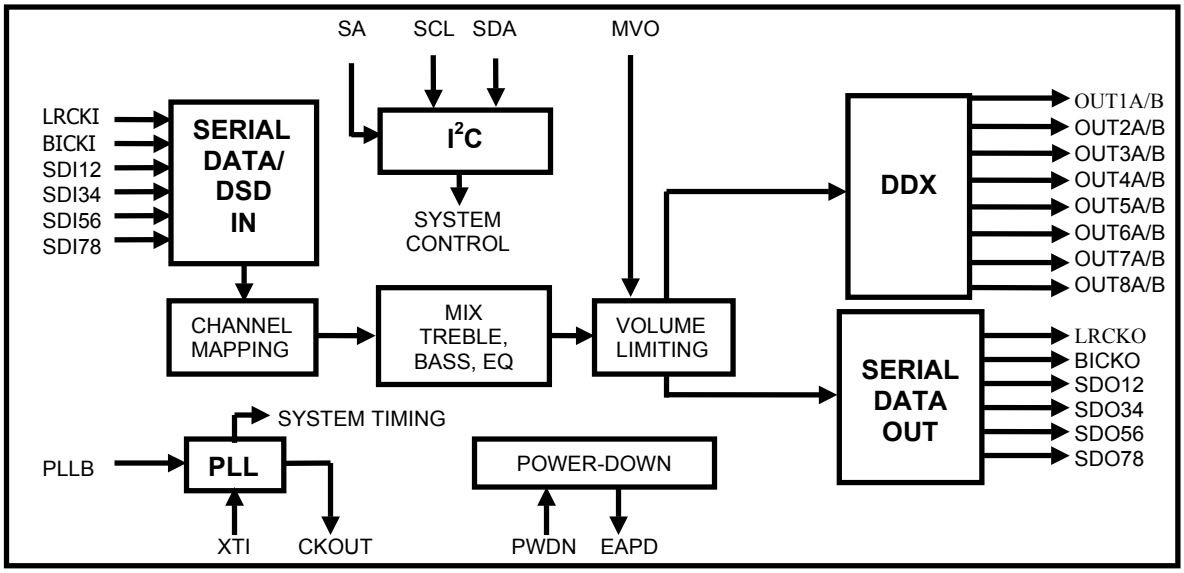


Figure 1 - IC-Level Block Diagram

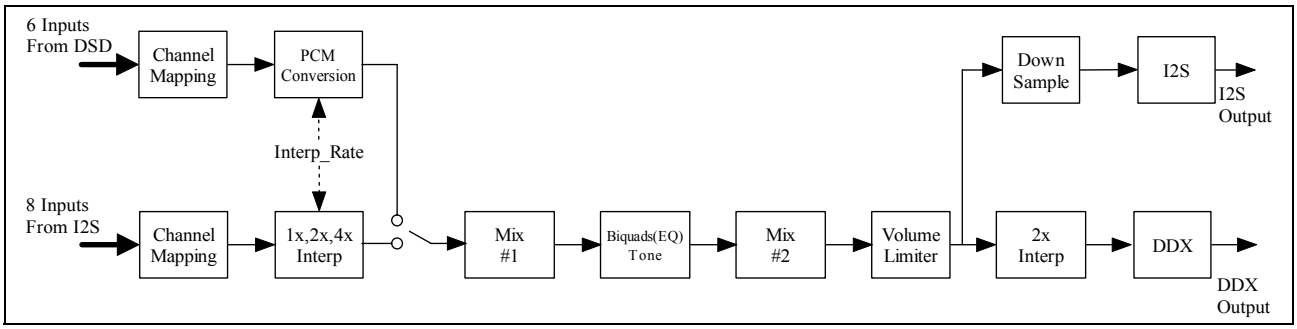


Figure 2 - Channel Signal Flow Diagram

1.1 Pin Function

Table 1 - Pin Description and Numbering

Pin	I/O	Pin Name	Description	Pad Type
1	I	MVO/DSD_CLK	Master Volume Override/ DSD Input Clock	5V Tolerant TTL Input Buffer
3, 12, 28, 35, 44, 52, 59	I	VDD3	3.3V Supply	3.3V Digital Power Supply Voltage
2, 4, 13, 27, 36, 45, 53, 60		GND	Ground	Digital Ground
5,14, 22, 26, 37, 46, 54, 61		NC	No Connect	
6	I	SDI_78/DSD_6	Input Serial Data Channels 7 & 8/ DSD Input Channel 6	5V Tolerant TTL Input Buffer

Table 1 - Pin Description and Numbering				
Pin	**I/O**	**Pin Name**	**Description**	**Pad Type**
7	I	SDI_56/DSD_5	Input Serial Data Channels 5 & 6/ DSD Input Channel 5	5V Tolerant TTL Input Buffer
8	I	SDI_34/DSD_4	Input Serial Data Channels 3 & 4/ DSD Input Channel 4	5V Tolerant TTL Input Buffer
9	I	SDI_12/DSD_3	Input Serial Data Channels 1 & 2/ DSD Input Channel 3	5V Tolerant TTL Input Buffer
10	I	LRCKI/DSD_2	Input Left/Right Clock/ DSD Input Channel 2	5V Tolerant TTL Input Buffer
11	I	BICKI/DSD_1	Input Serial Clock/ DSD Input Channel 1	5V Tolerant TTL Input Buffer
15	I	RESET	Global Reset	5V Tolerant TTL Schmitt Trigger Input Buffer
16	I	PLL_BYPASS	Bypass Phase Locked Loop	5V Tolerant TTL Input with Pull-Down
17	I	SA	Select Address (I2C)	5V Tolerant TTL Input with Pull-Down
18	I/O	SDA	I2C Serial Data	Bidirectional Buffer: 5 V Tolerant TTL Schmitt Trigger Input; 3.3V Capable 2 mA Slew-rate control Output;
19	I	SCL	I2C Serial Clock	5V Tolerant TTL Schmitt Trigger Input Buffer
20	I	XTI	Clock Input	5V Tolerant TTL Schmitt Trigger Input Buffer
21	I	FILTER_PLL	PLL Filter	Analog Pad
23		GNDA	PLL Ground	Analog Ground
24	I	VDDA	PLL Supply	3.3V Analog Power Supply Voltage
25	O	CKOUT	Clock Output	3.3 V Capable TTL Tristate 4 mA Output Buffer
29	O	OUT8B	PWM Channel 8 Output B	3.3V Capable TTL 2mA Output Buffer
30	O	OUT8A	PWM Channel 8 Output A	3.3V Capable TTL 2mA Output Buffer
31	O	OUT7B	PWM Channel 7 Output B	3.3V Capable TTL 2mA Output Buffer
32	O	OUT7A	PWM Channel 7 Output A	3.3V Capable TTL 2mA Output Buffer
33	O	OUT6B	PWM Channel 6 Output B	3.3V Capable TTL 2mA Output Buffer
34	O	OUT6A	PWM Channel 6 Output A	3.3V Capable TTL 2mA Output Buffer
38	O	OUT5B	PWM Channel 5 Output B	3.3V Capable TTL 2mA Output Buffer
39	O	OUT5A	PWM Channel 5 Output A	3.3V Capable TTL 2mA Output Buffer
40	O	OUT4B	PWM Channel 4 Output B	3.3V Capable TTL 2mA Output Buffer
41	O	OUT4A	PWM Channel 4 Output A	3.3V Capable TTL 2mA Output Buffer
42	O	OUT3B	PWM Channel 3 Output B	3.3V Capable TTL 2mA Output Buffer
43	O	OUT3A	PWM Channel 3 Output A	3.3V Capable TTL 2mA Output Buffer
47	O	OUT2B	PWM Channel 2 Output B	3.3V Capable TTL 2mA Output Buffer
48	O	OUT2A	PWM Channel 2 Output A	3.3V Capable TTL 2mA Output Buffer
49	O	OUT1B	PWM Channel 1 Output B	3.3V Capable TTL 2mA Output Buffer
50	O	OUT1A	PWM Channel 1 Output A	3.3V Capable TTL 2mA Output Buffer
51	O	EAPD	Ext. Amp Power Down	3.3V Capable TTL 2mA Output Buffer
55	O	BICKO	Output Serial Clock	3.3V Capable TTL 2mA Output Buffer
56	O	LRCKO	Output Left/Right Clock	3.3V Capable TTL 2mA Output Buffer
57	O	SDO_12	Output Serial Data Channels 1&2	3.3V Capable TTL 2mA Output Buffer
58	O	SDO_34	Output Serial Data Channels 3&4	3.3V Capable TTL 2mA Output Buffer
62	O	SDO_56	Output Serial Data Channels 5&6	3.3V Capable TTL 2mA Output Buffer
63	O	SDO_78	Output Serial Data Channels 7&8	3.3V Capable TTL 2mA Output Buffer
64	I	PWDN	Device Powerdown	5V Tolerant TTL Schmitt Trigger Input Buffer

1.2 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{DD\ 3.3}$	3.3V Digital Power Supply	-0.5 to 4	V
V_{DDA}	3.3V Analog Power Supply	-0.5 to 4	V
V_i	Voltage on input pins	-0.5 to (Vdd + 0.5)	V
V_o	Voltage on output pins	-0.5 to (Vdd + 0.5)	V
V_b	Voltage on 5V tolerant inputs and bi-directional pins (Note 1)	-0.5 to 5.5	V
T_{stg}	Storage Temperature	-40 to +150	°C
T_A	Ambient operating temperature	-20 to +85	°C

Note 1 –Withstands -0.8V undershoot and 6.3V overshoots for 4ns max.

1.3 THERMAL DATA

Symbol	Parameter	Value	Unit
$R\theta_{j-a}$	Thermal resistance Junction to Ambient	85	°C/W

1.4 RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}_3.3	3.3V Digital Power Supply Voltage	3.0 to 3.6	V
V_{DDA}	3.3V Analog Power Supply	3.0 to 3.6	V
T_A	Operating Ambient Temperature	0 to 70	°C

1.4.1 DC ELECTRICAL CHARACTERISTICS: 3.3V CAPABLE OUTPUT BUFFERS (Note 2) (pins 18,25,29-34,38-43,47-51,55-58,62,63)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{OL2}	Low Level 2mA Output	Iol = 2mA			0.15	V
V_{OH2}	High Level 2mA Output	Ioh = -2mA	V_{DD}-0.15			V
V_{OL4}	Low Level 4mA Output	Iol = 4 mA			0.15	V
V_{OH4}	High Level 4mA Output	Ioh = -4 mA	V_{DD}-0.15			V

Note 2 - The min and max values comply to the JEDEC standard, which is 0.4V max for Vol and 2.4 for Voh.

1.4.2 DC ELECTRICAL CHARACTERISTICS: 5V TOLERANT INPUT BUFFERS (pins 1,6-11,15,18,19,20,64)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{hyst}	Schmitt Trigger Hysteresis		0.4			V
I_{IL}	Low Level Input Current	Vi = 0V (Note 3)	40	60	110	uA
I_{IH}	High Level Input Current	Vi = VDD_3.3 (Note 3)	25	60	110	uA

Note 3 - Min condition: vdd=3V, 125C, min process; Max condition: vdd=3.6V, -40C, fast process.

1.4.3 OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$I_{VDD\ 3.3}$	Operating Current 3.3V	All 8-channels operating		73		mA
$I_{VDD\_3.3}$	PowerDown Current 3.3V	PowerDown Asserted		7		mA

1.4.4 ELECTRICAL CHARACTERISTICS (VDD= 3.3±0.3V, T_A=0 to 70°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{ESD}	Electrostatic Protection	Leakage <1uA (Note 4)	2000			V

Note 4 - Human Body Model.

1.4.5 TIMING CHARACTERISTICS

(VDD= 3.3±0.3V, T_A=0 to 70°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{reset}	Reset hold time	Active Low Reset (pin 15)	100			nSec
CKO_{48k}	Clock Out Frequency w/ 48k/96k/192k Fs	COS1..0 = '10'		12.288		MHz
$CKO_{44.1k}$	Clock Out Frequency w/ 44.1k/88.2k/176.4k Fs	COS1..0 = '10'		11.2896		MHz
$CKO_{Free\text{-}run}$	Clock Out Free-run Frequency	No clock applied at XTI (Note 5)	2.3	3.5		MHz
CKO_{Jitter}	Short-term Jitter	Rising →Rising Edge		300		pSec pk-pk

Note 5 - The DDX-8001 is designed to operate at a minimum free-run frequency when there is no clock applied at XTI. This assures proper I2C communication without a valid master clock. The device is not designed to process audio data without a valid clock applied at XTI.

1.5 PIN DESCRIPTION

1.5.1 MVO/DSD_CLK: Master Volume Override and DSD Input Clock (pin 1)

The Master Volume Override enables the user to bypass the Volume Control on all channels. When MVO is pulled High, the Master Volume Register is set to 00h, which corresponds to its Full Scale setting. The Master Volume Register Setting offsets the individual Channel Volume Settings, which default to 0dB. Also, with MVO pulled high the EAPD output will enable the power device. This mode is intended for testing purposes and applications where I^2C is not available.

When in DSD Mode (IR=11), this input is used for the DSD input clock, which should be typically 2.8224MHz. When operating the device in DSD Mode, this pin must be held low until the DSD input mode is selected via MCS and IR bits in Configuration Register A.

1.5.2 SDI_12 through 78/DSD Data Inputs: Serial Data In (pins 6-9)

PCM audio information enters the device here. Six format choices are available including I^2S, left- or right-justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits.

When in DSD Mode, these pins serve as the data inputs for channels 3 thru 6.

1.5.3 LRCKI: Left/Right Clock In/ DSD Data Input (pin 10)

The Left/Right clock input is for the purpose of data word framing. The clock frequency will be at the input sample rate Fs.

When in DSD Mode, this pin serves as the data input for channel 2.

1.5.4 BICKI: Bit Clock In/ DSD Data Input (pin 11)

The serial or bit clock input is for the purpose of framing each data bit. The bit clock frequency is typically 64*Fs, for example using I^2S serial format.

When in DSD Mode, this pin serves as the data input for channel 1.

1.5.5 RESET (pin 15)

Driving RESET low sets all outputs low and returns all register settings to their defaults. The reset is asynchronous to the internal clock.

1.5.6 PLL Bypass (pin 16)

PLL Bypass is used to steer the XTI input bypassing the internal PLL circuit. This pin will bypass the internal PLL and the XTI clock input will directly drive the internal device clock. This is intended for testing purposes only.

129 Morgan Drive, Norwood, MA 02062 voice: (781) 551-9450 fax: (781) 440-9528 email: apogee@apogeeddx.com

1.5.7 I²C (pins 17-19)

The SA (Select Address), SDA (I²C Data) and SCL (I²C Clock) pins operate per the I²C specification. See Section 2.0. Fast-mode (400kB/sec) I2C communication is supported.

1.5.8 PLL: Phase Locked Loop

The phase locked loop section provides the System Timing Signals and CKOUT.

1.5.8.1 XTI: Master clock In (pin 20)

This is the master clock input. The master clock must be an integer multiple of the LR clock frequency. Typically, the master clock frequency is 12.288 MHz (256*Fs) for a 48kHz sample rate, which is the default at power-up. Care must be taken not to exceed an internal clock frequency of 98.304MHz; otherwise the device may not properly operate or be able to communicate.

1.5.8.2 PLLF: PLL Filter (pin 21)

PLL Filter connects to external filter components for PLL loop compensation. Refer to the schematic diagram, Figure 23, for the recommended circuit.

1.5.8.3 VDDA and GNDA: Phase Locked Loop Power (pins 24, 23)

The phase locked loop power is applied here. This +3.3V supply must be well bypassed and filtered for noise immunity. The audio performance of the device is critically dependent upon the PLL circuit.

1.5.8.4 CKOUT: Clock Out (pin 25)

System synchronization and master clocks are provided by the CKOUT. This output may be used as a clock source for other devices in the system.

1.5.9 OUT1 through OUT8: PWM Outputs (pins 29-34, 38-43, 47-50)

The PWM outputs provide the input signal for the power devices. Both patented DDX® and binary PWM modes are supported.

1.5.10 EAPD: External Amplifier Power-Down (pin 51)

EAPD (output) is used to control the operation of DDX® Power Devices and for Power-on and Power-off sequencing.

1.5.11 BICKO and LRCKO: Bit Clock Out and LR Clock Out (pins 55, 56)

These clock signals are used to frame the I²S output audio data.

When in DSD mode, these pins output at 176.4kHz sample rate.

1.5.12 SDO_12 through 78: Serial Data Out (pins 57, 58, 62, 63)

PCM audio information exits the device here. Six different format choices are available including I²S, left- or right-justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits.

1.5.13 PWDN: Device Power-Down (pin 64)

PWDN puts the DDX-8001 into a low-power state via appropriate power-down sequence. Pulling PWDN low begins power-down sequence, a soft-mute is performed on all outputs, and EAPD goes low ~30ms later.

1.6 AUDIO PERFORMANCE

Parameter	From DDX-2160 Output	From I2S Output	From Analog Line Ouput
SNR AW(Typical)	-100dB	-137dB	-99dB
Dynamic Range AW(Typical)	-100dB	-137dB	-99dB
THD (Typical)	0.035% (1W, 1kHz)	0.00002% (-10dBFS)	0.015% (1 VRMS, 1kHz)

The EB-8001 test platform was used to produce the measurements shown in the following sections. This platform was designed with the interest of testing and demonstrating the DDX-8001 device in concert with the DDX-2160 power device(s). See the corresponding application note for more detailed information including schematics concerning this evaluation board.

1.6.1 Performance measured with DDX-2160 Power Device at Vcc=34V, 8 Ohm load.

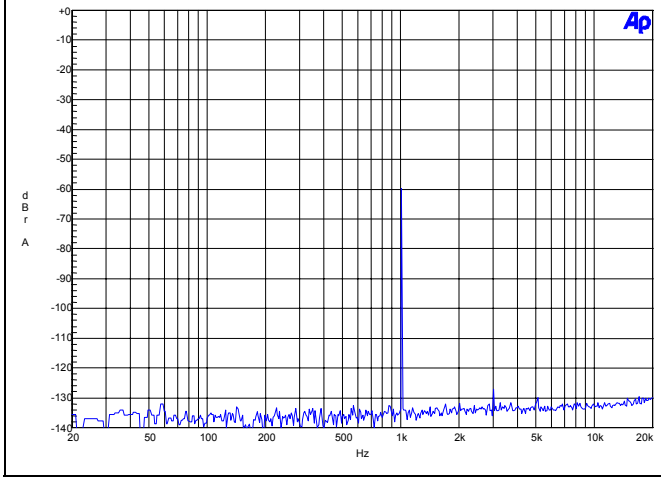


Figure 3 - FFT –60dB, 1kHz Output

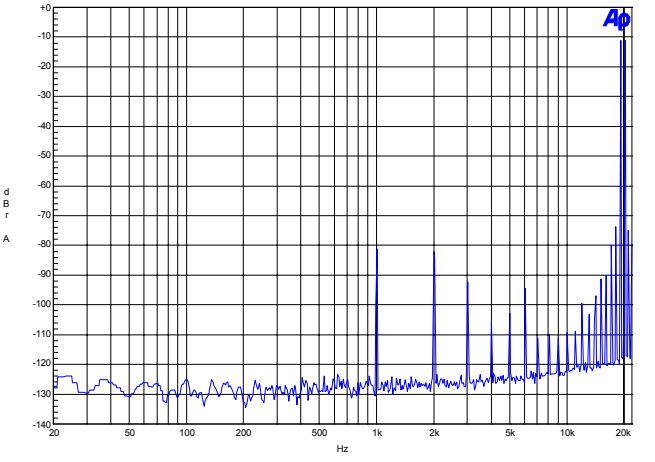


Figure 4 - FFT Inter-Modulation Distortion 19kHz and 20kHz

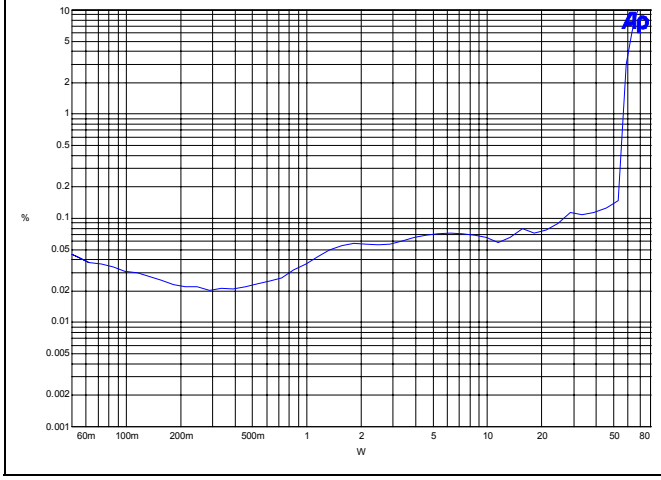


Figure 5 - THD vs. Power, 1kHz

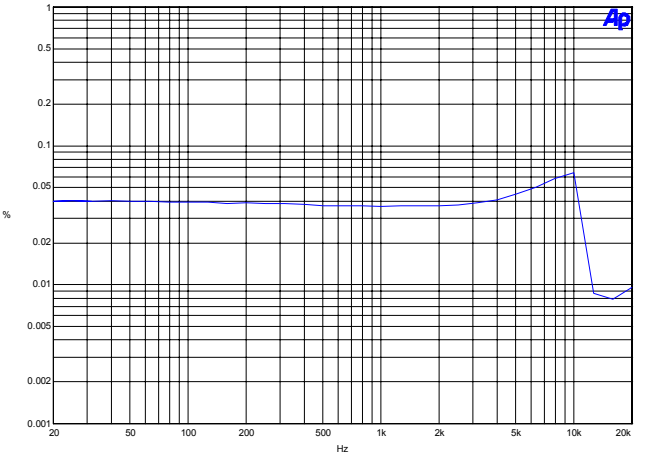


Figure 6 - THD vs. Frequency, 1W

1.6.2 Performance of I2S Output :

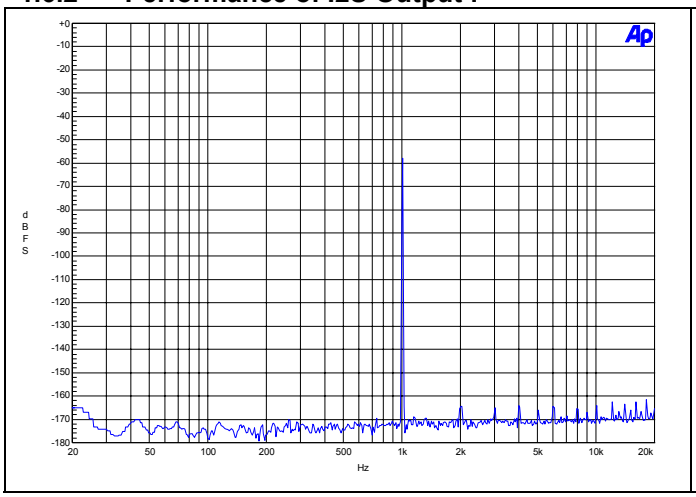


Figure 7 - FFT –60dB, 1kHz Output

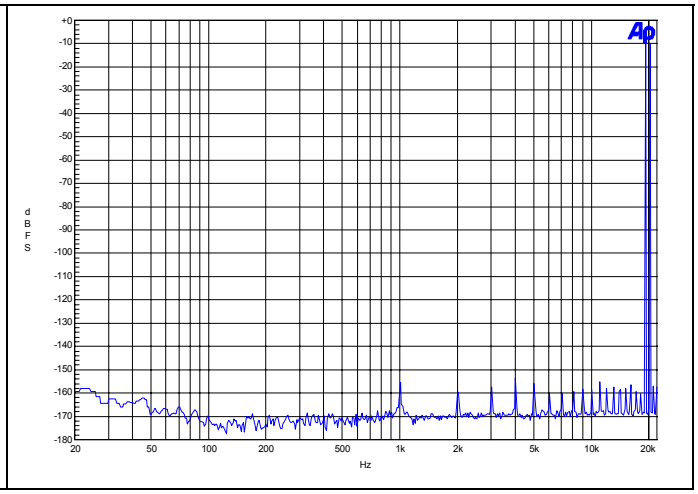


Figure 8 - FFT Inter-Modulation Distortion

1.6.3 Performance of Analog Line Output

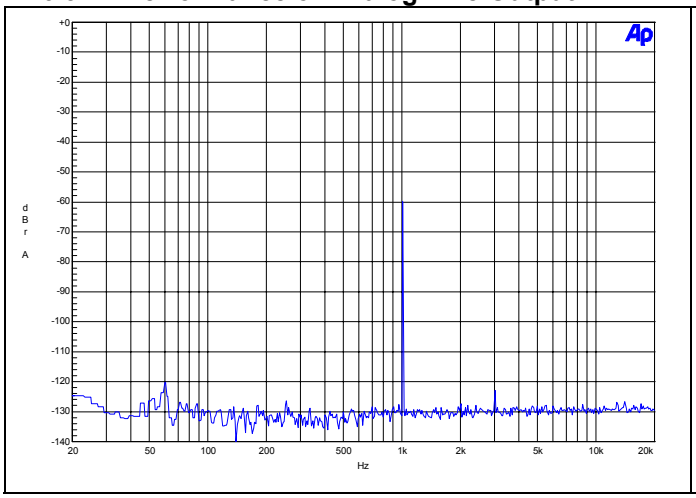


Figure 9 - FFT –60dB, 1kHz Output

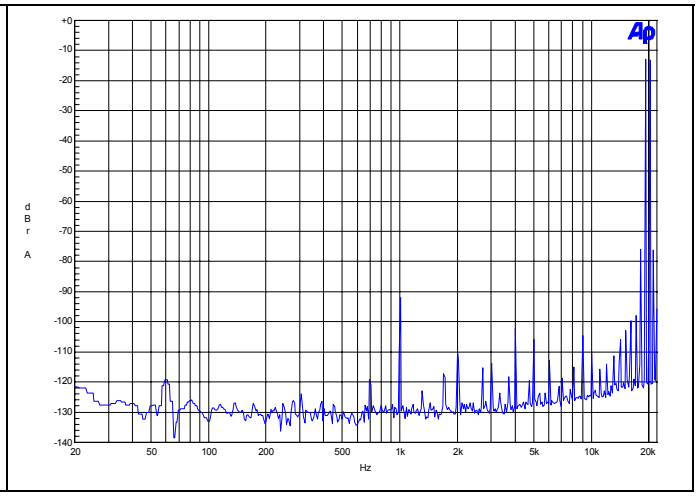


Figure 10 - FFT Inter-Modulation Distortion 19kHz and 20kHz

1.6.3 Performance of Analog Line Output (continued)

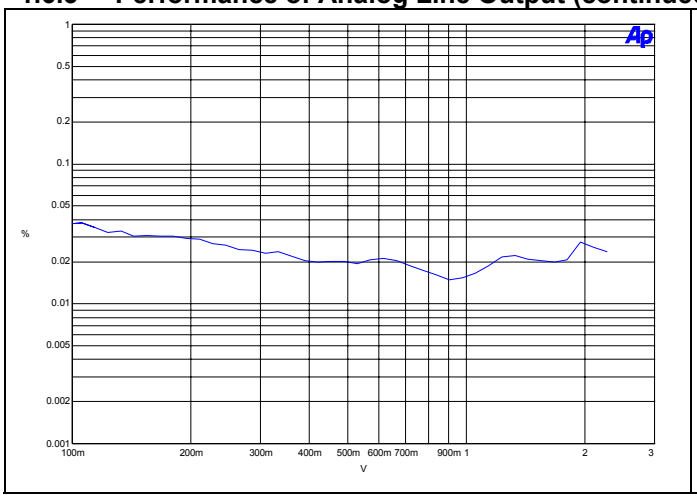


Figure 11 - THD vs. Voltage RMS , 1kHz

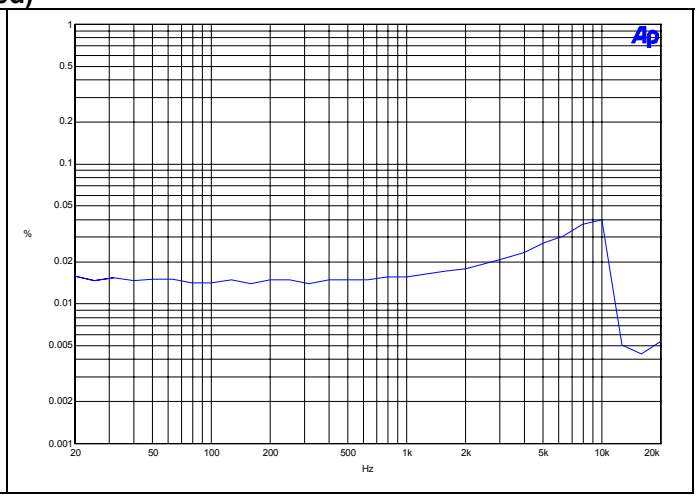


Figure 12 - THD vs. Frequency, 1Vrms

1.7 PIN CONNECTION (Top View)

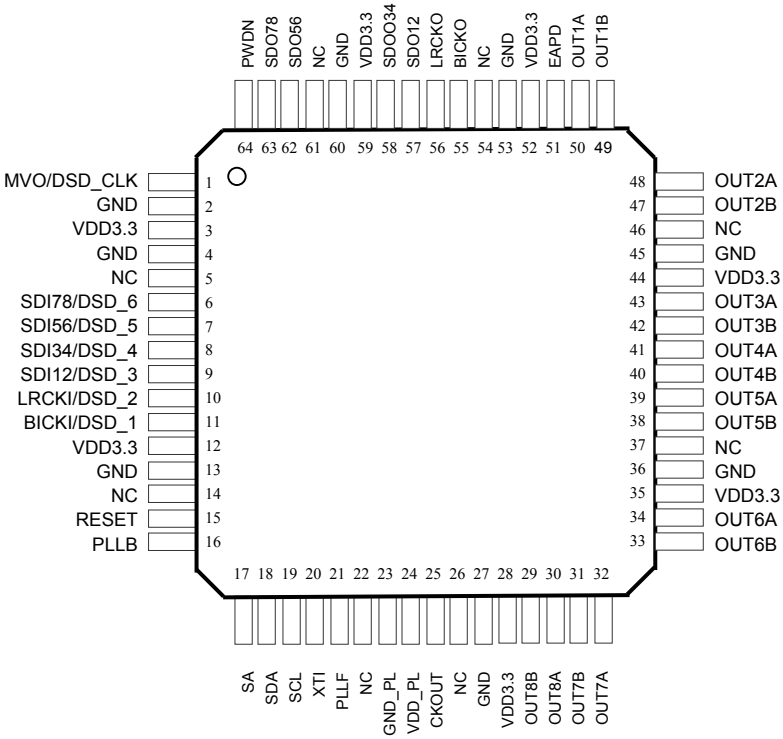


Figure 13 – Pin Connection Diagram.

2.0 DDX-8001 I²C BUS SPECIFICATION

The DDX-8001 supports the I²C protocol. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The DDX-8001 is always a slave device in all of its communications.

2.1 COMMUNICATION PROTOCOL

2.1.1 Data Transition or change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition.

2.1.2 Start Condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

2.1.3 Stop Condition

STOP is identified by a low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between DDX-8001 and the bus master.

2.1.4 Data Input

During the data input the DDX-8001 samples the SDA signal on the rising edge of clock SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

2.2 DEVICE ADDRESSING

To start communication between the master and the DDX-8001, the master must initiate with a start condition. Following this, the master sends 8-bits (MSB first) onto the SDA line corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I²C bus definition. In the DDX-8001 the I²C interface has two device addresses depending on the SA pin configuration, 0x40 or 0100000x when SA = 0, and 0x42 or 0100001x when SA = 1.

The 8th bit (LSB) identifies read or write operation, RW. This bit is set to 1 in read mode and 0 for write mode. After a START condition the DDX-8001 identifies the device address on the bus. If a match is found, it acknowledges the identification on the SDA bus during the 9th bit time. The byte following the device identification byte is the internal space address.

2.3 WRITE OPERATION

Following the START condition the master sends a device select code with the RW bit set to 0. The DDX-8001 acknowledges this and then the master writes the internal address byte. After receiving the internal byte address the DDX-8001 again responds with an acknowledgement.

2.3.1 Byte Write

In the byte write mode the master sends one data byte. This is acknowledged by the DDX-8001. The master then terminates the transfer by generating a STOP condition.

2.3.2 Multi-byte Write

The multi-byte write modes can start from any internal address. Sequential data byte writes will be written to sequential addresses within the DDX-8001. The master generating a STOP condition terminates the transfer.

2.4 READ OPERATION

2.4.1 Current Address Byte Read

Following the START condition the master sends a device select code with the RW bit set to 1. The DDX-8001 acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

2.4.1.1 Current Address Multi-byte Read

The multi-byte read modes can start from any internal address. Sequential data bytes will be read from sequential addresses within the DDX-8001. The master acknowleges each data byte read and then generates a STOP condition terminating the transfer.

2.4.2 Random Address Byte Read

Following the START condition the master sends a device select code with the RW bit set to 0. The DDX-8001 acknowledges this and then the master writes the internal address byte. After receiving the internal byte address the DDX-8001 again responds with an acknowledgement. The master then initiates another START condition and sends the device select code with the RW bit set to 1. The DDX-8001 acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

2.4.2.1 Random Address Multi-byte Read

The multi-byte read modes can start from any internal address. Sequential data bytes will be read from sequential addresses within the DDX-8001. The master acknowleges each data byte read and then generates a STOP condition terminating the transfer.

Write Mode Sequence

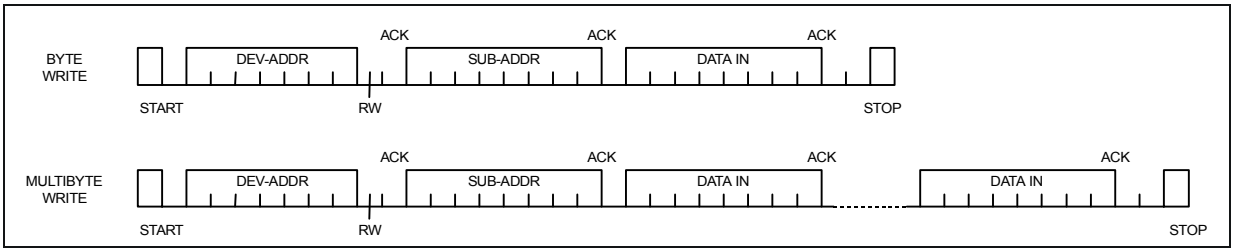


Figure 14 - I²C Write Procedure

Read Mode Sequence

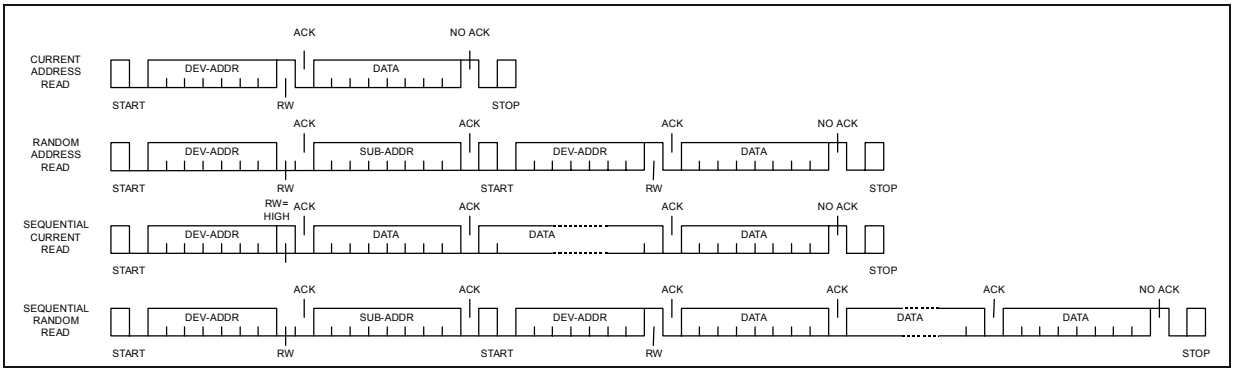


Figure 15 - I²C Read Procedure

3.0 Register Description

Table 2 - Register Summary

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x00	ConfA	COS1	COS0	DSPB	IR1	IR0	MCS2	MCS1	MCS0
0x01	ConfB				SAIFB	SAI3	SAI2	SAI1	SAI0
0x02	ConfC				SAOFB	SAO3	SAO2	SAO1	SAO0
0x03	*ConfD*	MPC	CSZ4	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
0x04	ConfE	C8BO	C7BO	C6BO	C5BO	C4BO	C3BO	C2BO	C1BO
0x05	ConfF	PWMS2	PWMS1	PWMS0	BQL	PSL	DEMP	DRC	HPB
0x06	ConfG	MPCV	RES	HPE	RES	AME	COD	SID	PWMD
0x07	ConfH	ECLE	RES	BCLE	IDE	ZDE	SVE	ZCE	NSBW
0x08	ConfI	EAPD							PSCE
0x09	Mmute								MMute
0x0A	Mvol	MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
0x0B	C1Vol	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0x0C	C2Vol	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0x0D	C3Vol	C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0x0E	C4Vol	C4V7	C4V6	C4V5	C4V4	C4V3	C4V2	C4V1	C4V0
0x0F	C5Vol	C5V7	C5V6	C5V5	C5V4	C5V3	C5V2	C5V1	C5V0
0x10	C6Vol	C6V7	C6V6	C6V5	C6V4	C6V3	C6V2	C6V1	C6V0
0x11	C7Vol	C7V7	C7V6	C7V5	C7V4	C7V3	C7V2	C7V1	C7V0
0x12	C8Vol	C8V7	C8V6	C8V5	C8V4	C8V3	C8V2	C8V1	C8V0
0x13	C1VTMB	C1M	C1VBP		C1VT4	C1VT3	C1VT2	C1VT1	C1VT0
0x14	C2VTMB	C2M	C2VBP		C2VT4	C2VT3	C2VT2	C2VT1	C2VT0
0x15	C3VTMB	C3M	C3VBP		C3VT4	C3VT3	C3VT2	C3VT1	C3VT0
0x16	C4VTMB	C4M	C4VBP		C4VT4	C4VT3	C4VT2	C4VT1	C4VT0
0x17	C5VTMB	C5M	C5VBP		C5VT4	C5VT3	C5VT2	C5VT1	C5VT0
0x18	C6VTMB	C6M	C6VBP		C6VT4	C6VT3	C6VT2	C6VT1	C6VT0
0x19	C7VTMB	C7M	C7VBP		C7VT4	C7VT3	C7VT2	C7VT1	C7VT0
0x1A	C8VTMB	C8M	C8VBP		C8VT4	C8VT3	C8VT2	C8VT1	C8VT0
0x1B	C12im		C2IM2	C2IM1	C2IM0		C1IM2	C1IM1	C1IM0
0x1C	C34im		C4IM2	C4IM1	C4IM0		C3IM2	C3IM1	C3IM0
0x1D	C56im		C6IM2	C6IM1	C6IM0		C5IM2	C5IM1	C5IM0
0x1E	C78im		C8IM2	C8IM1	C8IM0		C7IM2	C7IM1	C7IM0
0x1F	Auto1	AMDM	AMGC2	AMGC1	AMGC0	AMV1	AMV0	AMEQ1	AMEQ0
0x20	Auto2	SUB	RSS1	RSS0	CSS1	CSS0	FSS	AMBMXE	AMBMME
0x21	Auto3	AMAM2	AMAM1	AMAM0	AMAME			MSA	AMPS
0x22	PreEQ	XO2	XO1	XO0	PEQ4	PEQ3	PEQ2	PEQ1	PEQ0
0x23	Ageq				AGEQ4	AGEQ3	AGEQ2	AGEQ1	AGEQ0
0x24	Bgeq				BGEQ4	BGEQ3	BGEQ2	BGEQ1	BGEQ0
0x25	Cgeq				CGEQ4	CGEQ3	CGEQ2	CGEQ1	CGEQ0
0x26	Dgeq				DGEQ4	DGEQ3	DGEQ2	DGEQ1	DGEQ0
0x27	Fgeq				EGEQ4	EGEQ3	EGEQ2	EGEQ1	EGEQ0
0x28	BQlp	C8BLP	C7BLP	C6BLP	C5BLP	C4BLP	C3BLP	C2BLP	C1BLP
0x29	MXlp	C8MXLP	C7MXLP	C6MXLP	C5MXLP	C4MXLP	C3MXLP	C2MXLP	C1MXLP
0x2A	EQbp	C8EQBP	C7EQBP	C6EQBP	C5EQBP	C4EQBP	C3EQBP	C2EQBP	C1EQBP
0x2B	ToneBP	C8TCB	C7TCB	C6TCB	C5TCB	C4TCB	C3TCB	C2TCB	C1TCB
0x2C	Tone	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0x2D	C1234ls	C4LS1	C4LS0	C3LS1	C3LS0	C2LS1	C2LS0	C1LS1	C1LS0
0x2E	C5678ls	C8LS1	C8LS0	C7LS1	C7LS0	C6LS1	C6LS0	C5LS1	C5LS0
0x2F	L1ar	L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0x30	L1atrt	L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0x31	L2ar	L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0x32	L2atrt	L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0

Table 2 - Register Summary

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x33	C12ot		C2OT2	C2OT1	C2OT0		C1OT2	C1OT1	C1OT0
0x34	C34ot		C4OT2	C4OT1	C4OT0		C3OT2	C3OT1	C3OT0
0x35	C56ot		C6OT2	C6OT1	C6OT0		C5OT2	C5OT1	C5OT0
0x36	C78ot		C8OT2	C8OT1	C8OT0		C7OT2	C7OT1	C7OT0
0x37	C12om		C2OM2	C2OM1	C2OM0		C1OM2	C1OM1	C1OM0
0x38	C34om		C4OM2	C4OM1	C4OM0		C3OM2	C3OM1	C3OM0
0x39	C56om		C6OM2	C6OM1	C6OM0		C5OM2	C5OM1	C5OM0
0x3A	C78om		C8OM2	C8OM1	C8OM0		C7OM2	C7OM1	C7OM0
0x3B	Cfaddr1							CFA9	CFA8
0x3C	Cfaddr2	CFA7	CFA6	CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0x3D	B1cf1	C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0x3E	B1cf2	C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0x3F	B1cf3	C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0x40	B2cf1	C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0x41	B2cf2	C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0x42	B2cf3	C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0x43	A1cf1	C3B23	C3B22	C3B21	C3B20	C3B19	C3B18	C3B17	C3B16
0x44	A1cf2	C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0x45	A1cf3	C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0x46	A2cf1	C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0x47	A2cf2	C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0x48	A2cf3	C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0x49	B0cf1	C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0x4A	B0cf2	C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0x4B	B0cf3	C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0x4C	Cfud							WA	W1
0x4D	MPCC1	MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0x4E	MPCC2	MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
0x4F	*RES*	*RES*	*RES*	*RES*	*RES*	*RES*	*RES*	*RES*	*RES*
0x50	*RES*	*RES*	*RES*	*RES*	*RES*	*RES*	*RES*	*RES*	*RES*
0x51	PSC1	RCV11	RCV10	RCV9	RCV8	RCV7	RCV6	RCV5	RCV4
0x52	PSC2	RCV3	RCV2	RCV1	RCV0	CNV11	CNV10	CNV9	CNV8
0x53	PSC3	CNV7	CNV6	CNV5	CNV4	CNV3	CNV2	CNV1	CNV0

3.1 Configuration Register A (address 00h)

D7	D6	D5	D4	D3	D2	D1	D0
COS1	COS0	DSPB	IR1	IR0	MCS2	MCS1	MCS0
1	0	0	0	0	0	1	1

3.1.1 Master Clock Select

BIT	R/W	RST	NAME	DESCRIPTION
2..0	R/W	011	MCS (2..0)	Master Clock Select : Selects the ratio between the input I^2S sample frequency and the input clock.

The DDX-8001 will support sample rates of 32kHz, 44.1kHz, 48khz, 88.2kHz, 96kHz, 176.4kHz, 192kHz, and 2.8224MHz DSD. Therefore the internal clock will be:

- 65.536MHz for 32kHz
- 90.3168MHz for 44.1kHz, 88.2kHz, 176.4kHz, and DSD
- 98.304MHz for 48kHz, 96kHz, and 192kHz

The external clock frequency provided to the XTI pin must be an exact multiple of the input sample frequency (fs). The relationship between the input clock and the input sample rate is determined by both the MCSx and the IRx (Input Rate) register bits. The MCSx bits determine the PLL factor generating the internal clock and the IRx bits

determine the oversampling ratio used internally. Care must be taken to not exceed an internal clock frequency of 98.304 MHz when changing MCS bits.

Table 3 - IR and MCS Settings for Input Sample Rate and Clock Rate

Input Sample Rate fs (kHz)	IR	MCS (2..0)				
		1xx	011	010	001	000
32, 44.1, 48	00	128fs	256fs	384fs	512fs	768fs
88.2, 96	01	64fs	128fs	192fs	256fs	384fs
176.4, 192	10	64fs	128fs	192fs	256fs	384fs
DSD	11	2fs	4fs	6fs	8fs	12fs

3.1.2 Interpolation Ratio Select

BIT	R/W	RST	NAME	DESCRIPTION
4..3	R/W	00	IR (1..0)	Interpolation Ratio Select: Selects internal interpolation ratio based on input I^2S sample frequency

The DDX-8001 has variable interpolation (oversampling) settings such that internal processing and DDX® output rates remain consistent. The first processing block interpolates by either 4 times, 2 times, or 1 time (pass-through). The oversampling ratio of this interpolation is determined by the IR bits.

Table 4 - IR bit settings as a function of Input Sample Rate

Input Sample RateFs (kHz)	IR (1,0)	1st Stage Interpolation Ratio
32	00	4 times oversampling
44.1	00	4 times oversampling
48	00	4 times oversampling
88.2	01	2 times oversampling
96	01	2 times oversampling
176.4	10	Pass-Through
192	10	Pass-Through
DSD	11	DSD -> 176.4kHz Conversion

3.1.3 DSP Bypass

BIT	R/W	RST	NAME	DESCRIPTION
5	R/W	0	DSPB	DSP Bypass Bit: 0 – Normal Operation 1 – Bypass of EQ and Mixing Functionality

Setting the DSPB bit bypasses all the EQ and Mixing functionality of the DDX-8001 Core.

3.1.4 Clock Output Select

BIT	R/W	RST	NAME	DESCRIPTION
7..6	R/W	10	COS (1..0)	Clock Output Select: Selects the frequency of the Clock Output, CKOUT pin

Table 5 - Clock Output Rate as a Function of COS and Sample Rate

COS (1,0)	Input Sample Rate (kHz)		
	32, 44.1, 48	88.2, 96	176.4, 192
00	2048*fs	1024*fs	512*fs
01	512*fs	256*fs	128*fs
10	256*fs	128*fs	64*fs
11	128*fs	64*fs	32*fs

3.2 Configuration Register B : Serial Input Formats (Address 01h)

D7	D6	D5	D4	D3	D2	D1	D0
			SAIFB	SAI3	SAI2	SAI1	SAI0
			0	0	0	0	0

3.2.1 Serial Audio Input Interface Format

BIT	R/W	RST	NAME	DESCRIPTION
3..0	R/W	0000	SAI (3..0)	Serial Audio Input Interface Format: Determines the interface format of the input serial digital audio interface.

Serial Data Interface

The DDX-8001 serial audio input was designed to interface with standard digital audio components and to accept a number of serial data formats. The DDX-8001 always acts as a slave when receiving audio input from standard digital audio components. Serial data for eight channels is provided using 6 input pins: left/right clock LRCKI (pin 10), serial clock BICKI (pin 11), serial data 1 & 2 SDI12 (pin 9), serial data 3 & 4 SDI34 (pin 8), serial data 5 & 6 SDI56 (pin 7), and serial data 7 & 8 SDI78 (pin 6).

The SAI register (Configuration Register B – 01h, Bits D3-D0) and the SAIFB register (Configuration Register B – 01h, Bit D4) are used to specify the serial data format. The default serial data format is I^2S, MSB-First. Available formats are shown in Figure 16 and the tables that follow.

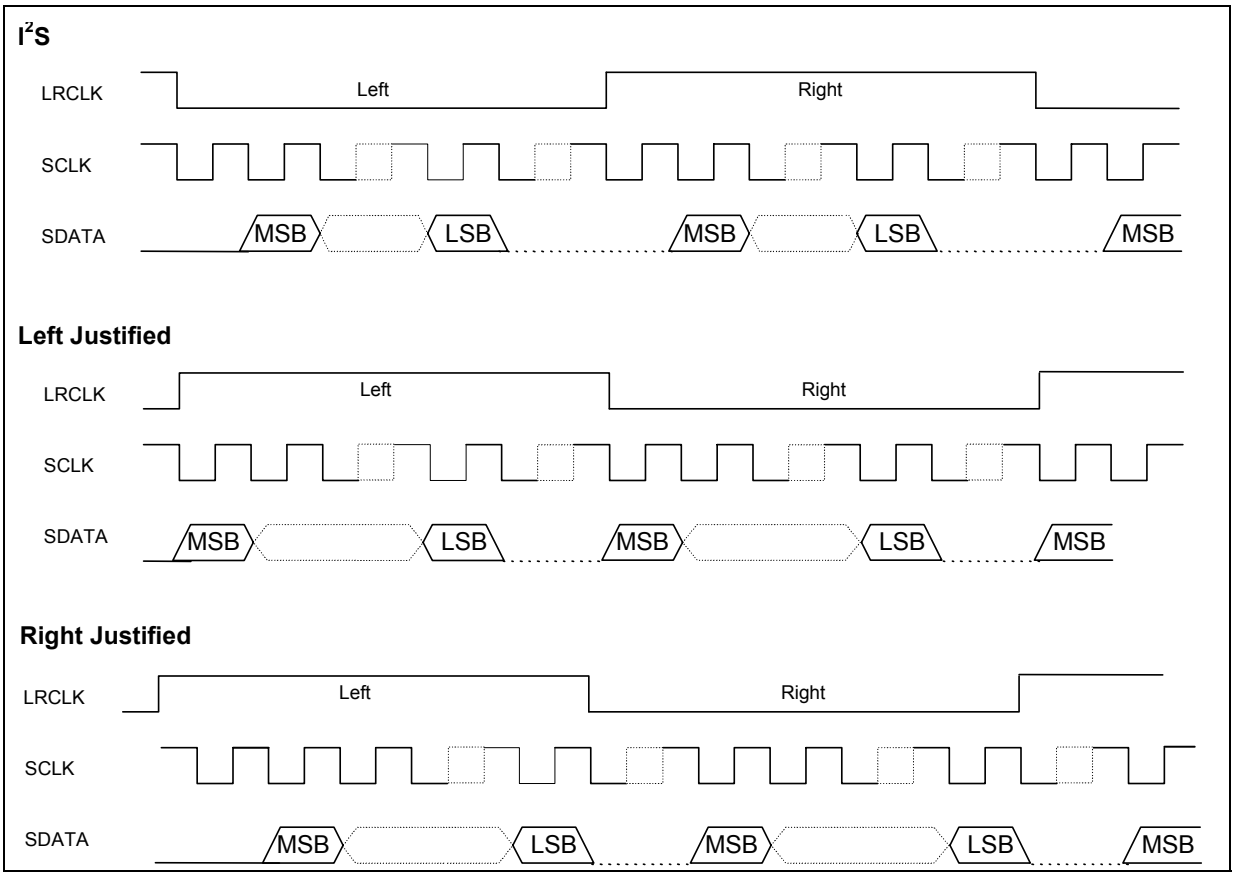


Figure 16 - General Serial Input and Output Formats

For example, SAI=1110 and SAIFB=1 would specify Right-Justified 16-bit data, LSB-First.

Table 7 below lists the serial audio input formats supported by DDX-8001 as related to BICKI = 32/48/64fs, where the sampling rate fs = 32/44.1/48/88.2/96/176.4/192 kHz.

Table 6 – First Bit Selection Table

SAIFB	Format
0	MSB-First
1	LSB-First

Note: Serial input and output formats are specified distinctly.

Table 7 - Supported Serial Audio Input Formats

BICKI	SAI (3...0)	SAIFB	Interface Format
32fs	1100	X	I^2S 15bit Data
	1110	X	Left/Right-Justified 16bit Data
48fs	0100	X	I^2S 23bit Data
	0100	X	I^2S 20bit Data
	1000	X	I^2S 18bit Data
	0100	0	MSB First I^2S 16bit Data
	1100	1	LSB First I^2S 16bit Data
	0001	X	Left-Justified 24bit Data
	0101	X	Left-Justified 20bit Data
	1001	X	Left-Justified 18bit Data
	1101	X	Left-Justified 16bit Data
	0010	X	Right-Justified 24bit Data
	0110	X	Right-Justified 20bit Data
	1010	X	Right-Justified 18bit Data
	1110	X	Right-Justified 16bit Data
64fs	0000	X	I^2S 24bit Data
	0100	X	I^2S 20bit Data
	1000	X	I^2S 18bit Data
	0000	0	MSB First I^2S 16bit Data
	1100	1	LSB First I^2S 16bit Data
	0001	X	Left-Justified 24bit Data
	0101	X	Left-Justified 20bit Data
	1001	X	Left-Justified 18bit Data
	1101	X	Left-Justified 16bit Data
	0010	X	Right-Justified 24bit Data
	0110	X	Right-Justified 20bit Data
	1010	X	Right-Justified 18bit Data
	1110	X	Right-Justified 16bit Data

Table 8 - Serial Input Data Timing characteristics (Fs = 32 to 192kHz)

BICKI FREQUENCY (slave mode)	12.5MHz max.
BICKI pulse width low (T0) (slave mode)	40 ns min.
BICKI pulse width high (T1) (slave mode)	40 ns min.
BICKI active to LRCKI edge delay (T2)	20 ns min.
BICKI active to LRCKI edge delay (T3)	20 ns min.
SDI valid to BICKI active setup (T4)	20 ns min.
BICKI active to SDI hold time (T5)	20 ns min.

129 Morgan Drive, Norwood, MA 02062 voice: (781) 551-9450 fax: (781) 440-9528 email: apogee@apogeeddx.com

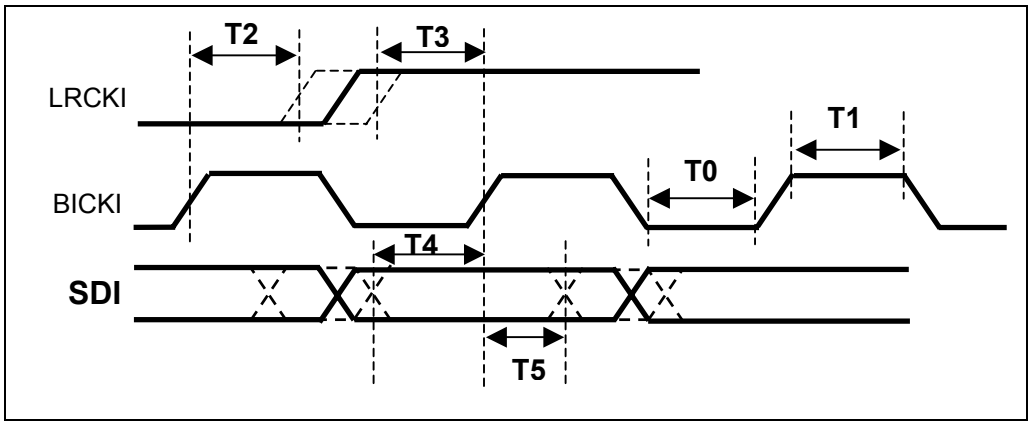


Figure 17 – Serial Input Data Timing Characteristics

3.3 Configuration Register C : Serial Output Formats (Address 02h)

D7	D6	D5	D4	D3	D2	D1	D0
			SAOFB	SAO3	SAO2	SAO1	SAO0
			0	0	0	0	0

3.3.1 Serial Audio Output Interface Format

BIT	R/W	RST	NAME	DESCRIPTION
3..0	R/W	0000	SAO (3..0)	Serial Audio Output Interface Format: Determines the interface format of the output serial digital audio interface.

The DDX-8001 Features a Serial Audio Output Interface that consists of 8 Channels. The Serial Audio Output always acts as a slave to the serial audio input interface and therefore all output clocks are synchronous with the input clocks. The output sample frequency (fs) is also equivalent to the input sample frequency. In the case of SACD/DSD input, the serial audio output will act as a master with an output fs of 176.4kHz. The output serial format can be selected independently from the input format and is done via the SAO and SAOFB bits found in configuration register C (02h).

3.3.2 Serial Audio Output Interface First Bit

BIT	R/W	RST	NAME	DESCRIPTION
4	R/W	0	SAOFB	Determines MSB or LSB first for all SAO formats 0 – MSB First 1 – LSB First

Table 9 - Serial Audio Output Data Formats

BICKI= BICKO	SAO (3...0)	Interface Format
32fs	0111	I^2S Data
	1111	Left/Right-Justified 16bit Data
48fs	1110	I^2S Data
	0001	Left-Justified Data
	1010	Right-Justified 24bit Data
	1011	Right-Justified 20bit Data
	1100	Right-Justified 18bit Data
	1101	Right-Justified 16bit Data
64fs	0000	I^2S Data
	0001	Left-Justified Data
	0010	Right-Justified 24bit Data
	0011	Right-Justified 20bit Data
	0100	Right-Justified 18bit Data
	0101	Right-Justified 16bit Data

3.4 Configuration Register D : PWM Output Formatting (Address 03h)

D7	D6	D5	D4	D3	D2	D1	D0
MPC	CSZ4	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
1	1	0	0	0	0	1	0

3.4.1 DDX® Power Output Mode

BIT	R/W	RST	NAME	DESCRIPTION
1..0	R/W	10	OM (1..0)	DDX Power Output Mode: Selects configuration of DDX® output.

The DDX® Power Output Mode selects how the DDX® output timing is configured. Different power devices can use different output modes. The DDX-2060/2100/2160 recommended use is OM = 10. When OM=11 the CSZ bits determine the size of the DDX® compensating pulse.

Table 10 - DDX® Output Modes

OM (1,0)	Output Stage – Mode
00	Not Used
01	Not Used
10	DDX-2060/2100/2160
11	Variable Compensation

3.4.2 DDX® Variable Compensating Pulse Size

CSZ(4..0)	Compensating Pulse Size
00000	0 Clock period Compensating Pulse Size
00001	1 Clock period Compensating Pulse Size
…	…
11111	31 Clock period Compensating Pulse Size

The DDX® variable compensating pulse size is intended to adapt to different power stage ICs. Contact Apogee applications for support when deciding this function.

3.4.3 Max Power Correction

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	1	MPC	Max Power Correction: 0 – MPC Disabled 1 – MPC Enabled

Setting the MPC bit corrects the DDX-2060/2100/2160 power device at high power. This mode will lower the THD+N of a full DDX-2060 DDX® system at maximum power output and slightly below.

3.5 Configuration Register E : Binary Output Selection (Address 04h)

D7	D6	D5	D4	D3	D2	D1	D0
C8BO	C7BO	C6BO	C5BO	C4BO	C3BO	C2BO	C1BO
0	0	0	0	0	0	0	0

3.5.1 Binary Output Enable Registers

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	C1BO	Channels 1, 2, 3, 4, 5, 6, 7, & 8 Binary Output Mode Enable Bits. 0 – DDX® Ternary Output Modulation 1 – Binary Output Modulation
1	R/W	0	C2BO	
2	R/W	0	C3BO	
3	R/W	0	C4BO	
4	R/W	0	C5BO	
5	R/W	0	C6BO	
6	R/W	0	C7BO	
7	R/W	0	C8BO	

Each individual channel output can be set to output a binary PWM stream. In this mode output A of a channel will be considered the positive output and output B is the negative inverse.

3.6 Configuration Register F (Address 05h)

D7	D6	D5	D4	D3	D2	D1	D0
PWMS2	PWMS1	PWMS0	BQL	PSL	DEMP	DRC	HPB
0	0	0	0	0	0	0	0

3.6.1 High-Pass Filter Bypass

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	HPB	High-Pass Filter Bypass Bit. 0 – AC Coupling High Pass Filter Enabled 1 – AC Coupling High Pass Filter Disabled

The DDX-8001 features an internal digital high-pass filter for the purpose of DC Blocking. The purpose of this filter is to prevent DC signals from passing through a DDX® amplifier. DC signals can cause speaker damage.

If HPB = 1, then this filter is made available as user-programmable biquad#1.

3.6.2 Dynamic Range Compression/Anti-Clipping Bit

BIT	R/W	RST	NAME	DESCRIPTION
1	R/W	0	DRC	Dynamic Range Compression/Anti-Clipping 0 – Limiters act in Anti-Clipping Mode 1 – Limiters act in Dynamic Range Compression Mode

Both limiters can be used in one of two ways, anti-clipping or dynamic range compression. When used in anti-clipping mode the limiter threshold values are constant and dependent on the limiter settings. In dynamic range compression mode the limiter threshold values vary with the volume settings allowing a nighttime listening mode that provides a reduction in the dynamic range regardless of the volume level.

3.6.3 De-Emphasis

BIT	R/W	RST	NAME	DESCRIPTION
2	R/W	0	DEMP	De-emphasis: 0 – No De-emphasis 1 – De-emphasis

By setting this bit to HIGH, or one (1), de-emphasis will implemented on all channels. When this feature is used it takes the place of biquad #7 in each channel and any coefficients using biquad #1 will be ignored. DSPB (DSP Bypass, Bit D5, CFA) bit must be set to 0 for De-emphasis to function.

3.6.4 Post-Scale Link

BIT	R/W	RST	NAME	DESCRIPTION
3	R/W	0	PSL	Post-Scale Link: 0 – Each Channel uses individual Post-Scale value 1 – Each Channel uses Channel 1 Post-Scale value

Post-Scale functionality is an attenuation placed after the volume control and directly before the conversion to PWM. Post-Scale is used by the PSCorrect™ feature and can also be used to limit the maximum modulation index and therefore the peak current. A setting of 1 in the PSL register will result in the use of the value stored in Channel 1 post-scale for all eight internal channels.

3.6.5 Biquad Coefficient Link

BIT	R/W	RST	NAME	DESCRIPTION
4	R/W	0	BQL	Biquad Link: 0 – Each Channel uses coefficient values 1 – Each Channel uses Channel 1 coefficient values

For ease of use, all channels can use the biquad coefficients loaded into the Channel 1 Coefficient RAM space by setting the BQL bit to 1. Therefore, any EQ updates only have to be performed once.

3.6.6 PWM Speed Mode

BIT	R/W	RST	NAME	DESCRIPTION
7..5	R/W	000	PWMS (2..0)	PWM Speed Selection:

Table 12 - PWM Output Speed Selections

PWMS (1..0)	PWM Output Speed
000	Normal Speed (384kHz) All Channels
001	Half Speed (192kHz) All Channels
010	Double Speed (768kHz) All Channels
011	Normal Speed Channels 1-6, Double Speed Channels 7-8
100	Odd Speed (341.3kHz) All Channels

3.7 Configuration Register G (Address 06h)

D7	D6	D5	D4	D3	D2	D1	D0
MPCV	*RES*	HPE	*RES*	AME	COD	SID	PWMD
0	0	0	0	0	0	0	0

3.7.1 Output Signal Disables

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	PWMD	PWM Output Disable: 0 – PWM Output Normal 1 - No PWM Output
1	R/W	0	SID	Serial Interface (I^2S Out) Disable: 0 – I^2S Output Normal 1- No I^2S Output
2	R/W	0	COD	Clock Output Disable: 0 – Clock Output Normal 1- No Clock Output

The Output Signal Disable bits will turn off, driving low, the corresponding outputs at the pin.

3.7.2 AM Mode Enable

BIT	R/W	RST	NAME	DESCRIPTION
3	R/W	0	AME	AM Mode Enable: 0 – Normal DDX® operation. 1 – AM reduction mode DDX® operation.

The DDX-8001 features a DDX® processing mode that minimizes the amount of noise generated in the frequency range of AM radio. This mode is intended for use when DDX® is operating in a device with an active AM tuner. The SNR of the DDX® processing is reduced to ~83dB in this mode, which is still greater than the SNR of AM radio.

3.7.3 Headphone Enable

BIT	R/W	RST	NAME	DESCRIPTION
5	R/W	0	HPE	DDX® Headphone Enable: 0 – Channels 7 & 8 normal DDX® operation 1 – Channels 7 & 8 headphone operation

Channels 7 and 8 can be configured to be processed and output in such a manner that headphones can be driven using an appropriate output device. This signal is a fully differential 3-wire drive called DDX® Headphone.

3.7.4 Max Power Correction Variable

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	MPCV	Max Power Correction Variable: 0 – Use Standard MPC Coefficient 1 – Use MPCC bits for MPC Coefficient

By enabling MPC and setting MPCV = 1, the max power correction becomes variable. By adjusting the MPCC registers (address 0x4D-0x4E) it becomes possible to adjust the THD at maximum unclipped power to a lower value for a particular application.

3.8 Configuration Register H (Address 07h)

D7	D6	D5	D4	D3	D2	D1	D0
ECLE	*RES*	BCLE	IDE	ZDE	SVE	ZCE	*RES*
0	1	1	1	1	1	1	0

3.8.1 Zero-Crossing Volume Enable

BIT	R/W	RST	NAME	DESCRIPTION
1	R/W	1	ZCE	Zero-Crossing Volume Enable: 1 – Volume adjustments will only occur at digital zero-crossings 0 – Volume adjustments will occur immediately

The ZCE bit enables zero-crossing volume adjustments. When volume is adjusted on digital zero-crossings no clicks will be audible.

3.8.2 Soft Volume Update Enable

BIT	R/W	RST	NAME	DESCRIPTION
2	R/W	1	SVE	Soft Volume Enable: 1 – Volume adjustments will use soft volume 0 – Volume adjustments will occur immediately

The DDX-8001 includes a soft volume algorithm that will step through the intermediate volume values at a predetermined rate when a volume change occurs. By setting SVE=0 this can be bypassed and volume changes will jump from old to new value directly.

3.8.3 Zero-Detect Mute Enable

BIT	R/W	RST	NAME	DESCRIPTION
3	R/W	1	ZDE	Zero-Detect Mute Enable: Setting of 1 enables the automatic zero-detect mute

Setting the ZDE bit enables the zero-detect automatic mute. When ZDE=1, the zero-detect circuit looks at the input data to each processing channel after the channel-mapping block. If any channel receives 2048 consecutive zero value samples (regardless of fs) then that individual channel is muted.

3.8.4 Invalid Input Detect Mute Enable

BIT	R/W	RST	NAME	DESCRIPTION
4	R/W	1	IDE	Invalid Input Detect Auto-Mute Enable: 0 – Disabled 1 – Enabled

Setting the IDE bit enables this function, which looks at the input I^2S data and clocking and will automatically mute all outputs if the signals are perceived as invalid.

3.8.5 Binary Clock Loss Detection Enable

BIT	R/W	RST	NAME	DESCRIPTION
5	R/W	1	BCLE	Binary Output Mode Clock Loss Detection Enable 0 – Disabled 1 – Enabled

Detects loss of input MCLK in binary mode and will output 50% duty cycle to prevent audible artifacts when input clocking is lost.

3.8.6 Auto-EAPD on Clock Loss Enable

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	ECLE	Auto EAPD on Clock Loss 0 – Disabled 1 – Enabled

When ECLE is active, it issues a power device power down signal (EAPD) on clock loss detection.

3.9 Configuration Register I (Address 08h)

D7	D6	D5	D4	D3	D2	D1	D0
EAPD							PSCE
0							0

3.9.1 PSCorrect™ Enable

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	PSCE	Power Supply Ripple Correction Enable: 0 – Normal Operation 1 – PSCorrect™ Operation

This feature utilizes an ADC on SDI78 that provides power supply ripple information for correction. Registers PSC1, PSC2, PSC3 are utilized in this mode. Please refer to PSCorrect™ Application Note for further details.

3.9.2 External Amplifier Power Down

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	EAPD	External Amplifier Power Down: 0 – External Power Stage Power Down Active 1 – Normal Operation

EAPD is used to actively power down a connected DDX® Power device. This register has to be written to 1 at start-up to enable the DDX® power device for normal operation.

3.10 Volume Control

3.10.1 Master Controls

3.10.1.1 Master Mute Register (Address 09h)

D7	D6	D5	D4	D3	D2	D1	D0
							MMUTE
							0

3.10.1.2 Master Volume Register (Address 0Ah)

D7	D6	D5	D4	D3	D2	D1	D0
MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
1	1	1	1	1	1	1	1

Note : Value of volume derived from MVOL is dependent on AMV AutoMode Volume settings.

3.10.2 Channel Controls

3.10.2.1 Channel 1 Volume (Address 0Bh)

D7	D6	D5	D4	D3	D2	D1	D0
C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0	1	1	0	0	0	0	0

3.10.2.2 Channel 2 Volume (Address 0Ch)

D7	D6	D5	D4	D3	D2	D1	D0
C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0	1	1	0	0	0	0	0

3.10.2.3 Channel 3 Volume (Address 0Dh)

D7	D6	D5	D4	D3	D2	D1	D0
C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0	1	1	0	0	0	0	0

3.10.2.4 Channel 4 Volume (Address 0Eh)

D7	D6	D5	D4	D3	D2	D1	D0
C4V7	C4V6	C4V5	C4V4	C4V3	C4V2	C4V1	C4V0
0	1	1	0	0	0	0	0

3.10.2.5 Channel 5 Volume (Address 0Fh)

D7	D6	D5	D4	D3	D2	D1	D0
C5V7	C5V6	C5V5	C5V4	C5V3	C5V2	C5V1	C5V0
0	1	1	0	0	0	0	0

3.10.2.6 Channel 6 Volume (Address 10h)

D7	D6	D5	D4	D3	D2	D1	D0
C6V7	C6V6	C6V5	C6V4	C6V3	C6V2	C6V1	C6V0
0	1	1	0	0	0	0	0

3.10.2.7 Channel 7 Volume (Address 11h)

D7	D6	D5	D4	D3	D2	D1	D0
C7V7	C7V6	C7V5	C7V4	C7V3	C7V2	C7V1	C7V0
0	1	1	0	0	0	0	0

3.10.2.8 Channel 8 Volume (Address 12h)

D7	D6	D5	D4	D3	D2	D1	D0
C8V7	C8V6	C8V5	C8V4	C8V3	C8V2	C8V1	C8V0
0	1	1	0	0	0	0	0

3.10.2.9 Channel 1 Volume Trim, Mute, Bypass (Address 13h)

D7	D6	D5	D4	D3	D2	D1	D0
C1M	C1VBP		C1VT4	C1VT3	C1VT2	C1VT1	C1VT0
0	0	0	1	0	0	0	0

3.10.2.10 Channel 2 Volume Trim, Mute, Bypass (Address 14h)

D7	D6	D5	D4	D3	D2	D1	D0
C2M	C2VBP		C2VT4	C2VT3	C2VT2	C2VT1	C2VT0
0	0	0	1	0	0	0	0

3.10.2.11 Channel 3 Volume Trim, Mute, Bypass (Address 15h)

D7	D6	D5	D4	D3	D2	D1	D0
C3M	C3VBP		C3VT4	C3VT3	C3VT2	C3VT1	C3VT0
0	0	0	1	0	0	0	0

3.10.2.12 Channel 4 Volume Trim, Mute, Bypass (Address 16h)

D7	D6	D5	D4	D3	D2	D1	D0
C4M	C4VBP		C4VT4	C4VT3	C4VT2	C4VT1	C4VT0
0	0	0	1	0	0	0	0

3.10.2.13 Channel 5 Volume Trim, Mute, Bypass (Address 17h)

D7	D6	D5	D4	D3	D2	D1	D0
C5M	C5VBP		C5VT4	C5VT3	C5VT2	C5VT1	C5VT0
0	0	0	1	0	0	0	0

3.10.2.14 Channel 6 Volume Trim, Mute, Bypass (Address 18h)

D7	D6	D5	D4	D3	D2	D1	D0
C6M	C6VBP		C6VT4	C6VT3	C6VT2	C6VT1	C6VT0
0	0	0	1	0	0	0	0

3.10.2.15 Channel 7 Volume Trim, Mute, Bypass (Address 19h)

D7	D6	D5	D4	D3	D2	D1	D0
C7M	C7VBP		C7VT4	C7VT3	C7VT2	C7VT1	C7VT0
0	0	0	1	0	0	0	0

3.10.2.16 Channel 8 Volume Trim, Mute, Bypass (Address 1Ah)

D7	D6	D5	D4	D3	D2	D1	D0
C8M	C8VBP		C8VT4	C8VT3	C8VT2	C8VT1	C8VT0
0	0	0	1	0	0	0	0

3.10.3 Volume Description

The Volume structure of the DDX-8001 consists of individual volume registers for each channel, a master volume register, and individual channel volume trim registers. The channel volume settings are normally used to set the maximum allowable digital gain and to hard-set gain differences between certain channels. These values are normally set at the initialization of the IC and not changed. The individual channel volumes are adjustable in 0.5dB steps from +48dB to -78 dB. There is also an additional offset for each channel called the channel volume trim. The Channel trim is normally controlled via the consumer for balancing the output of the channels in surround sound settings. The Channel Volume Trim is adjustable independently on each channel from –10dB to +10dB in 1 dB steps. The master volume control is normally mapped to the master volume of the system.

The values of these three settings are summed to find the actual gain/volume value for any given channel. As an example if C5V = 1Eh or +33dB, C5VT = 12h or –2dB, and MV = 2Ah or –21dB, then the total gain for channel 5 = +10dB.

When set to 1, the Master Mute will mute all channels, whereas the individual channel mutes (CxM) will mute only that channel. Both the Master Mute and the Channel Mutes provide a “soft mute” with the volume ramping down to mute in 8192 samples from the maximum volume setting at the internal processing rate (~192kHz). A “hard mute” can be obtained by commanding a value of all 1’s (FFh) to any channel volume register or the master volume register. When volume offsets are provided via the master volume register any channel whose total volume is less than –100dB will be muted.

All changes in volume take place at zero-crossings when ZCE = 1 (configuration register H) on a per channel basis as this creates the smoothest possible volume transitions. When ZCE=0, volume updates will occur immediately.

The DDX-8001 also features a soft-volume update function that will ramp the volume between intermediate values when the value is updated, when SVE = 1 (configuration register H). This feature can be disabled by setting SVE = 0.

Each channel also contains an individual channel volume bypass. If a particular channel has volume bypassed via the CxVBP = 1 register then only the channel volume setting for that particular channel affects the volume setting, the master volume setting will not affect that channel.

Each channel also contains a channel mute. If CxM = 1 a soft mute is performed on that channel.

Table 13 - Master Volume Offset as a function of MV (7..0)

MV (7..0)	Volume Offset from Channel Value
00000000 (00h)	0dB
00000001 (01h)	-0.5dB
00000010 (02h)	-1dB
…	…
01001100 (4Ch)	-38dB
…	…
11111110 (FEh)	-127dB
11111111 (FFh)	Hard Master Mute

Table 14 - Channel Volume as a function of CxV (7..0)

CxV (7..0)	Volume
00000000 (00h)	+48dB
00000001 (01h)	+47.5dB
00000010 (02h)	+47dB
…	…
01100001 (5Fh)	+0.5dB
01100000 (60h)	0dB
01011111 (61h)	-0.5dB
…	…
11111110 (FEh)	-79.5 dB
11111111 (FFh)	Hard Channel Mute

129 Morgan Drive, Norwood, MA 02062 voice: (781) 551-9450 fax: (781) 440-9528 email: apogee@apogeeddx.com

Table 15 - Channel Volume Trim as a Function of CxVT (4..0)

CxVT (4..0)	Volume
00000 (00h)	+10dB
…	…
00110 (06h)	+10dB
00111 (07h)	+9dB
…	…
01111 (0Fh)	+1dB
10000 (10h)	0dB
10001 (11h)	-1dB
…	…
11001 (19h)	-9dB
11010 (1Ah)	-10dB
…	…
11111 (1Fh)	-10dB

3.11 Input Mapping

3.11.1 Channel Input Mapping Channels 1 & 2 (Address 1Bh)

D7	D6	D5	D4	D3	D2	D1	D0
	C2IM2	C2IM1	C2IM0		C1IM2	C1IM1	C1IM0
	0	0	1		0	0	0

3.11.2 Channel Input Mapping Channels 3 & 4 (Address 1Ch)

D7	D6	D5	D4	D3	D2	D1	D0
	C4IM2	C4IM1	C4IM0		C3IM2	C3IM1	C3IM0
	0	1	1		0	1	0

3.11.3 Channel Input Mapping Channels 5 & 6 (Address 1Dh)

D7	D6	D5	D4	D3	D2	D1	D0
	C6IM2	C6IM1	C6IM0		C5IM2	C5IM1	C5IM0
	1	0	1		1	0	0

3.11.4 Channel Input Mapping Channels 7 & 8 (Address 1Eh)

D7	D6	D5	D4	D3	D2	D1	D0
	C8IM2	C8M1	C8IM0		C7IM2	C7IM1	C7IM0
	1	1	1		1	1	0

Each channel received via I^2S can be mapped to any internal processing channel via the Channel Input Mapping registers. This allows for flexibility in processing, simplifies output stage designs, and enables crossovers to be performed. The default settings of these registers map each I^2S input channel to its corresponding processing channel.

Table 16 - Channel mapping as a function of CxIM bits.

CxIM (2..0)	Serial Input From
000	Channel 1
001	Channel 2
010	Channel 3
011	Channel 4
100	Channel 5
101	Channel 6
110	Channel 7
111	Channel 8

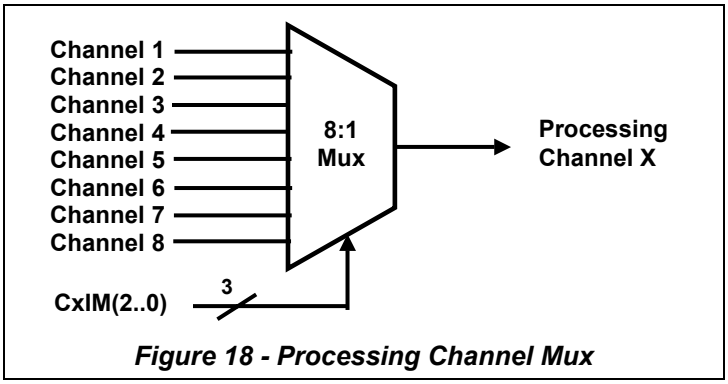


Figure 18 - Processing Channel Mux

3.12 AutoMode™ Registers

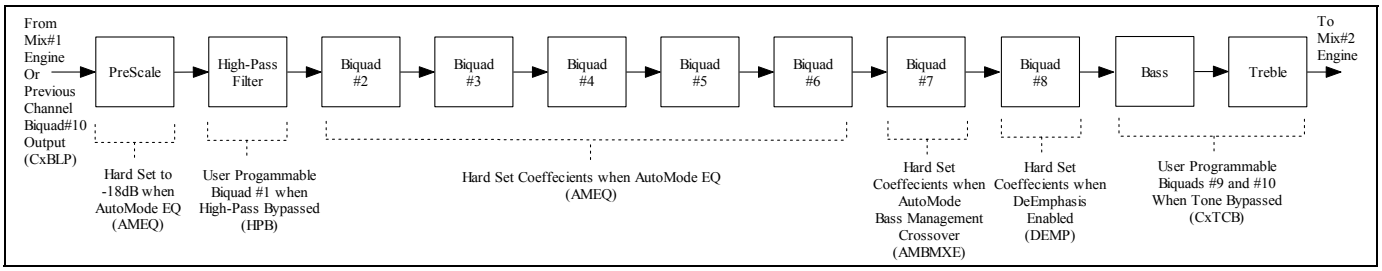


Figure 19 - EQ Processing Data Path and AutoMode Usage

3.12.1 Register – AutoModes EQ, Volume, GC (Address 1Fh)

D7	D6	D5	D4	D3	D2	D1	D0
AMDM	AMGC2	AMGC1	AMGC0	AMV1	AMV0	AMEQ1	AMEQ0
0	0	0	0	0	0	0	0

Table 17 - AutoMode EQ

AMEQ (1,0)	Mode (Biquad 2-6)
00	User Programmable
01	Preset EQ – PEQ bits
10	Graphic EQ – xGEQ bits
11	Auto Volume Controlled Loudness Curve

By setting AMEQ to any setting other than 00 enables AutoMode EQ. When set, biquads 1-5 are not user programmable. Any coefficient settings for these biquads will be ignored. Also when AutoMode EQ is used the pre-scale value for channels 1-6 becomes hard-set to –18dB.

Table 18 - AutoMode Volume

AMV (1,0)	Mode (MVOL)
00	MVOL 0.5dB 256 Steps (Standard)
01	MVOL Auto Curve 30 Steps
10	MVOL Auto Curve 40 Steps
11	MVOL Auto Curve 50 Steps

Table 19 - AutoMode Gain Compression/Limiters

AMGC (2..0)	Mode
000	User Programmable GC
001	AC No Clipping
010	AC Limited Clipping (10%)
011	DRC Nighttime Listening Mode
100	DRC TV Commercial/Channel AGC
101	AC 5.1 No Clipping
110	AC 5.1 Limited Clipping (10%)

AMDM – Automode 5.1 Downmix

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	AMDM	0 – Normal Operation 1 – Channels 7-8 are 2 channel downmix of channels 1-6

The Automode downmix setting uses channels 7-8 of Mix#1 engine and therefore these channels are hard-set and not allowed to be user set when in this mode.

Channels 1-6 must be arranged via Channel Mapping (CxIM) if necessary in the following manner for this operation:

Channel 1 – Left
Channel 2 – Right
Channel 3 – Left Surround
Channel 4 – Right Surround
Channel 5 – Center
Channel 6 – LFE

3.12.2 Register – AutoModes Bass Management (Address 20h)

D7	D6	D5	D4	D3	D2	D1	D0
SUB	RSS1	RSS0	CSS1	CSS0	FSS	AMBMXE	AMBMME
1	0	0	0	0	0	0	0

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	AMBMME	0 – Automode Bass Management Mix Disabled 1 – Automode Bass Management Mix Enabled

BIT	R/W	RST	NAME	DESCRIPTION
1	R/W	0	AMBMXE	0 – Automode Bass Management Crossover Disabled 1 – Automode Bass Management Crossover Enabled

Setting the AMBMME bit enables the proper mixing to take place for various preset bass management configurations. Setting the AMBMXE bit enables the proper crossover filtering in biquad #7 to take place. The crossover for bass management is always 2nd order (12 dB/octave) for the low-pass filter and 1st order (6 dB/octave) for the high-pass filter. The frequency of crossover is determined by the XOx bits in the Preset EQ register.

All configurations of Dolby Bass-Management can be performed in the IC. These different configurations are selected as they would be by the end-user on the basis of speaker size and/or on and off.

The AutoMode Bass Management Settings utilize Channels 1-6 on the Mix #1 engine, Channels 1-6 biquad #6, and Channels 1-2 on the Mix#2 engine in configuration #2. These functions cannot be user programmed while the bass management automode is active.

Not all settings are valid as some configurations are unlikely and do not have to be supported by Dolby Specification.

Automatic crossover settings are provided or custom crossovers can be implemented using the programmable biquads available.

Input Channels must be mapped using the channel-mapping feature in the following manner for Bass Management to be performed properly.

1 – Left front
2 – Right front
3 – Left Rear
4 – Right Rear
5 – Center
6 – LFE

Table 20 - Center and Rear Speaker Size Selection

Register/Setting	10	01	00
CSS – Center Speaker Size	Off	Large	Small
RSS – Rear Speaker Size	Off	Large	Small

Table 21 - Front and Sub Speaker Selection

Register/Setting	1	0
FSS – Front Speaker Size	Large	Small
SUB – Subwoofer	On	Off

When AMBMXE = 1, biquad #7 on channels 1-6 are utilized for bass-management crossover filter. This biquad is not user programmable in this mode. The XO settings determine the crossover frequency used. The crossover is 2nd order for both high-pass and low-pass with a –3dB cross point. Higher order filters can be obtained by programming coefficients in other biquads if desired.

It is recommended to use settings of 120-160Hz when using small, single driver satellite speakers, as the frequency response of these speakers is normally limited to this region.

3.12.3 Register – AutoMode AM/Pre-Scale/Bass Management Scale (Address 21h)

D7	D6	D5	D4	D3	D2	D1	D0
AMAM2	AMAM1	AMAM0	AMAME			MSA	AMPS
0	0	0	0			0	0

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	AMPS	AutoMode Pre-Scale 0 – -18dB used for Pre-scale when AMEQ /= 00 1 – User Defined Pre-scale when AMEQ /= 00

BIT	R/W	RST	NAME	DESCRIPTION
1	R/W	0	MSA	Bass Management Mix Scale Adjustment 0 – -12dB Scaling on satellite channels in Config #1 1 – No Scaling on satellite channels in Config #1

BIT	R/W	RST	NAME	DESCRIPTION
4	R/W	0	AMAME	AutoMode AM Enable 0 – Switching Frequency Determined by PWMS Settings 1 – Switching Frequency Determined by AMAM Settings

Table 22 - AutoMode AM Switching Frequency Selection

AMAM (2..0)	48kHz/96kHz Input Fs	44.1kHz/88.2kHz Input Fs
000	0.535MHz – 0.720MHz	0.535MHz – 0.670Mhz
001	0.721MHz – 0.900MHz	0.671MHz – 0.800MHz
010	0.901MHz – 1.100MHz	0.801MHz – 1.000MHz
011	1.101MHz – 1.300MHz	1.001MHz – 1.180MHz
100	1.301MHz – 1.480MHz	1.181MHz – 1.340Mhz
101	1.481MHz – 1.600MHz	1.341MHz – 1.500MHz
110	1.601MHz – 1.700MHz	1.501MHz – 1.700MHz

When DDX® is used concurrently with an AM radio tuner, it is advisable to use the AMAM bits to automatically adjust the output PWM switching rate dependent upon the specific radio frequency that the tuner is receiving. The values used in AMAM are also dependent upon the sample rate determined by the ADC used.

3.12.4 Register - Preset EQ Settings (Address 22h)

D7	D6	D5	D4	D3	D2	D1	D0
XO2	XO1	XO0	PEQ4	PEQ3	PEQ2	PEQ1	PEQ0
1	0	1	0	0	0	0	0

Table 23 - Crossover Frequency Selection

XO (2..0)	Bass Management Crossover Frequency
000	70 Hz
001	80 Hz
010	90 Hz
011	100 Hz
100	110 Hz
101	120 Hz
110	140 Hz
111	160 Hz

Table 24 - Preset EQ Selection

PEQ (3..0)	Setting
00000	Flat
00001	Rock
00010	Soft Rock
00011	Jazz
00100	Classical
00101	Dance
00110	Pop
00111	Soft
01000	Hard
01001	Party
01010	Vocal
01011	Hip-Hop
01100	Dialog
01101	Bass-Boost #1
01110	Bass-Boost #2
01111	Bass-Boost #3
10000	Loudness 1 (least boost)
10001	Loudness 2
10010	Loudness 3
10011	Loudness 4
10100	Loudness 5
10101	Loudness 6
10110	Loudness 7
10111	Loudness 8
11000	Loudness 9
11001	Loudness 10
11010	Loudness 11
11011	Loudness 12
11100	Loudness 13
11101	Loudness 14
11110	Loudness 15
11111	Loudness 16 (most boost)

3.12.5 Graphic EQ

3.12.5.1 Register – Graphic EQ 80Hz Band (Address 23h)

D7	D6	D5	D4	D3	D2	D1	D0
			AGEQ4	AGEQ3	AGEQ2	AGEQ1	AGEQ0
			0	1	1	1	1

3.12.5.2 Register – Graphic EQ 300Hz Band (Address 24h)

D7	D6	D5	D4	D3	D2	D1	D0
			BGEQ4	BGEQ3	BGEQ2	BGEQ1	BGEQ0
			0	1	1	1	1

3.12.5.3 Register – Graphic EQ 1kHz Band (Address 25h)

D7	D6	D5	D4	D3	D2	D1	D0
			CGEQ4	CGEQ3	CGEQ2	CGEQ1	CGEQ0
			0	1	1	1	1

3.12.5.4 Register – Graphic EQ 3kHz Band (Address 26h)

D7	D6	D5	D4	D3	D2	D1	D0
			DGEQ4	DGEQ3	DGEQ2	DGEQ1	DGEQ0
			0	1	1	1	1

3.12.5.5 Register – Graphic EQ 8kHz Band (Address 27h)

D7	D6	D5	D4	D3	D2	D1	D0
			EGEQ4	EGEQ3	EGEQ2	EGEQ1	EGEQ0
			0	1	1	1	1

Table 25 - Graphic EQ Boost/Cut Selection

XGEQ (4..0)	Boost/Cut
11111	+16
11110	+15
11101	+14
…	…
10000	+1
01111	0
01110	-1
…	…
00001	-14
00000	-15

3.13 Processing Loop Modes

3.13.1 Biquad Internal Channel Loop-Through (Address 28h)

D7	D6	D5	D4	D3	D2	D1	D0
C8BLP	C7BLP	C6BLP	C5BLP	C4BLP	C3BLP	C2BLP	C1BLP
0	0	0	0	0	0	0	0

Each internal processing channel can receive two possible inputs at the input to the biquad block. The input can be received either from the output of that channel's MIX#1 engine or from the output of bass/treble (Biquad#10) of the previous channel. In this scenario, channel 1 would receive channel 8. This enables the use of more than 10 biquads on any given channel at the loss of the number of separate internal processing channels.

CxBLP:
0 – Input from Channel X MIX#1 engine output – normal operation
1 – Input from Channel X-1 biquad #10 output – loop operation

3.13.2 Mix Internal Channel Loop-Through (Address 29h)

D7	D6	D5	D4	D3	D2	D1	D0
C8MXLP	C7MXLP	C6MXLP	C5MXLP	C4MXLP	C3MXLP	C2MXLP	C1MXLP
0	0	0	0	0	0	0	0

Each internal processing channel can receive two possible sets of inputs at the inputs to the Mix#1 block. The inputs can be received from the outputs of the interpolation block as normally occurs (CxMXLP = 0) or the inputs can be received from the outputs of the Mix#2 block. This enables the ability to perform additional filtering after the second mix block at the expense of losing this processing capability on the channel.

CxMXLP:
0 – Inputs to Channel X MIX#1 engine from interpolation outputs – Normal Operation
1 – Inputs from Channel X MIX#1 engine from MIX#2 engine outputs – loop operation

3.14 Processing Bypass Modes

3.14.1 EQ Bypass (Address 2Ah)

D7	D6	D5	D4	D3	D2	D1	D0
C8EQBP	C7EQBP	C6EQBP	C5EQBP	C4EQCBP	C3EQBP	C2EQBP	C1EQBP
0	0	0	0	0	0	0	0

EQ control can be bypassed on a per channel basis. If EQ control is bypassed on a given channel the prescale and all 10 filters (high-pass, biquads, de-emphasis, bass management cross-over, bass, treble in any combination) are bypassed for that channel.

CxEQBP:
0 – Perform EQ on Channel X – normal operation
1 – Bypass EQ on Channel X

3.14.2 Tone Control Bypass (Address 2Bh)

D7	D6	D5	D4	D3	D2	D1	D0
C8TCB	C7TCB	C6TCB	C5TCB	C4TCB	C3TCB	C2TCB	C1TCB
0	0	0	0	0	0	0	0

Tone control (bass/treble) can be bypassed on a per channel basis. If tone control is bypassed on a given channel the two filters that tone control utilizes are made available as user programmable biquads #9 and #10.

3.15 Tone Control (Address 2Ch)

D7	D6	D5	D4	D3	D2	D1	D0
TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0	1	1	1	0	1	1	1

Table 26 - Tone Control Boost/Cut Selection

BTC (3..0)/TTC (3..0)	Boost/Cut
0000	-12dB
0001	-12dB
…	…
0111	-4dB
0110	-2dB
0111	0dB
1000	+2dB
1001	+4dB
…	…
1101	+12dB
1110	+12dB
1111	+12dB

3.16 Dynamics Control

3.16.1 Channel Limiter Select Channels 1,2,3,4 (Address 2Dh)

D7	D6	D5	D4	D3	D2	D1	D0
C4LS1	C4LS0	C3LS1	C3LS0	C2LS1	C2LS0	C1LS1	C1LS0
0	0	0	0	0	0	0	0

3.16.2 Channel Limiter Select Channels 5,6,7,8 (Address 2Eh)

D7	D6	D5	D4	D3	D2	D1	D0
C8LS1	C8LS0	C7LS1	C7LS0	C6LS1	C6LS0	C5LS1	C5LS0
0	0	0	0	0	0	0	0

3.16.3 Limiter 1 Attack/Release Rate (Address 2Fh)

D7	D6	D5	D4	D3	D2	D1	D0
L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0	1	1	0	1	0	1	0

3.16.4 Limiter 1 Attack/Release Threshold (Address 30h)

D7	D6	D5	D4	D3	D2	D1	D0
L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0	1	1	0	1	0	0	1

3.16.5 Limiter 2 Attack/Release Rate (Address 31h)

D7	D6	D5	D4	D3	D2	D1	D0
L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0	1	1	0	1	0	1	0

3.16.6 Limiter 2 Attack/Release Threshold (Address 32h)

D7	D6	D5	D4	D3	D2	D1	D0
L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
0	1	1	0	1	0	0	1

3.16.7 Dynamics Control Description

The DDX-8001 includes 2 independent limiter blocks. The purpose of the limiters is to automatically reduce the dynamic range of a recording to prevent the outputs from clipping in anti-clipping mode, or to actively reduce the dynamic range for a better listening environment (such as a night-time listening mode, which is often needed for DVDs.) The two modes are selected via the DRC bit in Configuration Register F, bit 1 address 0x05. Each channel can be mapped to Limiter1, Limiter2, or not mapped. If a channel is not mapped, that channel will clip normally when 0 dB FS is exceeded. Each limiter will look at the present value of each channel that is mapped to it, select the maximum absolute value of all these channels, perform the limiting algorithm on that value, and then if needed adjust the gain of the mapped channels in unison.

The limiter attack thresholds are determined by the LxAT registers. When the Attack Thesehold has been exceeded, the limiter, when active, will automatically start reducing the gain. The rate at which the gain is reduced when the attack threshold is exceeded is dependent upon the attack rate register setting for that limiter. The gain reduction occurs on a peak-detect algorithm.

The release of limiter, when the gain is again increased, is dependent on a RMS-detect algorithm. The output of the volume/limiter block is passed through an RMS filter. The output of this filter is compared to the release threshold, determined by the Release Threshold register. When the RMS filter output falls below the release threshold, the gain is increased at a rate dependent upon the Release Rate register. The gain can never be increased past its set value and therefore the release will only occur if the limiter has already reduced the gain. The release threshold value can be used to set what is effectively a minimum dynamic range. This is helpful as over-limiting can reduce the dynamic range to virtually zero and cause program material to sound “lifeless”.

In AC mode the attack and release thresholds are set relative to full-scale. In DRC mode the attack threshold is set relative to the maximum volume setting of the channels mapped to that limiter and the release threshold is set relative to the maximum volume setting plus the attack threshold.

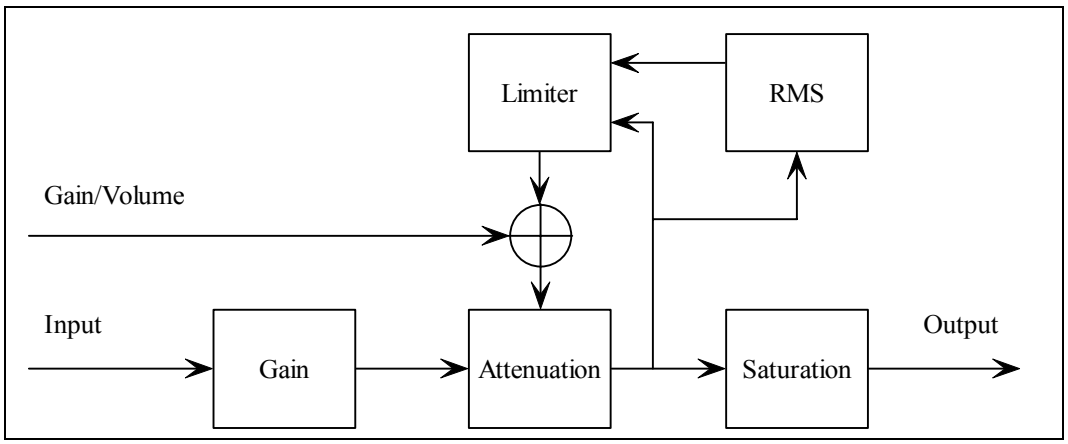


Figure 20 - Basic Limiter and Volume Flow Diagram.

Table 27 - Channel Limiter Mapping Selection

CxLS (1,0)	Channel Limiter Mapping
00	Channel has limiting disabled
01	Channel is mapped to limiter #1
10	Channel is mapped to limiter #2

Table 28 - Limiter Attack Rate Selection

LxA (3..0)	Attack Rate dB/ms	
0000	3.1584	Fast
0001	2.7072	
0010	2.2560	
0011	1.8048	
0100	1.3536	
0101	0.9024	
0110	0.4512	
0111	0.2256	
1000	0.1504	
1001	0.1123	
1010	0.0902	
1011	0.0752	
1100	0.0645	
1101	0.0564	
1110	0.0501	
1111	0.0451	Slow

Table 29 - Limiter Release Rate Selection

LxR (3..0)	Release Rate dB/ms	
0000	0.5116	Fast
0001	0.1370	
0010	0.0744	
0011	0.0499	
0100	0.0360	
0101	0.0299	
0110	0.0264	
0111	0.0208	
1000	0.0198	
1001	0.0172	
1010	0.0147	
1011	0.0137	
1100	0.0134	
1101	0.0117	
1110	0.0110	
1111	0.0104	Slow

Anti-Clipping Mode

Table 30 - Limiter Attack Threshold Selection (AC-Mode).

LxAT (3..0)	AC (dB relative to FS)
0000	-12
0001	-10
0010	-8
0011	-6
0100	-4
0101	-2
0110	0
0111	+2
1000	+3
1001	+4
1010	+5
1011	+6
1100	+7
1101	+8
1110	+9
1111	+10

Table 31 - Limiter Release Threshold Selection (AC-Mode).

LxRT (3..0)	AC (dB relative to FS)
0000	-∞
0001	-29dB
0010	-20dB
0011	-16dB
0100	-14dB
0101	-12dB
0110	-10dB
0111	-8dB
1000	-7dB
1001	-6dB
1010	-5dB
1011	-4dB
1100	-3dB
1101	-2dB
1110	-1dB
1111	-0dB

Dynamic Range Compression Mode

Table 32 - Limiter Attack Threshold Selection (DRC-Mode).

LxAT (3..0)	DRC (dB relative to Volume)
0000	-31
0001	-29
0010	-27
0011	-25
0100	-23
0101	-21
0110	-19
0111	-17
1000	-16
1001	-15
1010	-14
1011	-13
1100	-12
1101	-10
1110	-7
1111	-4

Table 33 - Limiter Release Threshold Selection (DRC-Mode).

LxRT (3..0)	DRC (db relative to Volume + LxAT)
0000	-∞
0001	-38dB
0010	-36dB
0011	-33dB
0100	-31dB
0101	-30dB
0110	-28dB
0111	-26dB
1000	-24dB
1001	-22dB
1010	-20dB
1011	-18dB
1100	-15dB
1101	-12dB
1110	-9dB
1111	-6dB

3.17 PWM Output Timing

3.17.1 Channel 1&2 Output Timing (Address 33h)

D7	D6	D5	D4	D3	D2	D1	D0
	C2OT2	C2OT1	C2OT0		C1OT2	C1OT1	C1OT0
	1	0	0		0	0	0

3.17.2 Channel 3&4 Output Timing (Address 34h)

D7	D6	D5	D4	D3	D2	D1	D0
	C4OT2	C4OT1	C4OT0		C3OT2	C3OT1	C3OT0
	1	1	0		0	1	0

3.17.3 Channel 5&6 Output Timing (Address 35h)

D7	D6	D5	D4	D3	D2	D1	D0
	C6OT2	C6OT1	C6OT0		C5OT2	C5OT1	C5OT0
	1	0	1		0	0	1

3.17.4 Channel 7&8 Output Timing (Address 36h)

D7	D6	D5	D4	D3	D2	D1	D0
	C8OT2	C8OT1	C8OT0		C7OT2	C7OT1	C7OT0
	1	1	1		0	1	1

The centering of the individual channel PWM output periods can be adjusted by the Output Timing registers. PWM slot settings can be chosen to insure that pulse transitions do not occur at the same time on different channels using the same power device. There are 8 possible settings, the appropriate setting varying based on the application and connections to the DDX® power devices.

Table 34 - Channel Output Timing Selection.

CxOT (2..0)	PWM Slot
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

3.18 I^2S Output Channel Mapping

3.18.1 Channel I^2S Output Mapping Channels 1 & 2 (Address 37h)

D7	D6	D5	D4	D3	D2	D1	D0
	C2OM2	C2OM1	C2OM0		C1OM2	C1OM1	C1OM0
	0	0	1		0	0	0

3.18.2 Channel I^2S Output Mapping Channels 3 & 4 (Address 38h)

D7	D6	D5	D4	D3	D2	D1	D0
	C4OM2	C4OM1	C4OM0		C3OM2	C3OM1	C3OM0
	0	1	1		0	1	0

3.18.3 Channel I^2S Output Mapping Channels 5 & 6 (Address 39h)

D7	D6	D5	D4	D3	D2	D1	D0
	C6OM2	C6OM1	C6OM0		C5OM2	C5OM1	C5OM0
	1	0	1		1	0	0

3.18.4 Channel I^2S Output Mapping Channels 7 & 8 (Address 3Ah)

D7	D6	D5	D4	D3	D2	D1	D0
	C8OM2	C8M1	C8OM0		C7OM2	C7OM1	C7OM0
	1	1	1		1	1	0

Each I^2S Output Channel can receive data from any channel output of the volume block. Which channel a particular I^2S output receives is dependent upon that channel's CxOM register bits.

Table 35 - Channel I²S Output Mapping

CxOM (2..0)	Serial Output From
000	Channel 1
001	Channel 2
010	Channel 3
011	Channel 4
100	Channel 5
101	Channel 6
110	Channel 7
111	Channel 8

4.0 User Programmable Processing

4.1 EQ – Biquad Equation

The biquads use the equation that follows. This is diagrammed in Figure 21 below.

$$Y[n] = 2(b_0/2)X[n] + 2(b_1/2)X[n-1] + b_2X[n-2] – 2(a_1/2)Y[n-1] – a_2Y[n-2]$$

$$= b_0X[n] + b_1X[n-1] + b_2X[n-2] – a_1Y[n-1] – a_2Y[n-2]$$

where Y[n] represents the output and X[n] represents the input. Multipliers are 28-bit signed fractional multipliers, with coefficient values in the range of 800000h (-1) to 7FFFFFh (0.9999998808).

Coefficients stored in the User Defined Coefficient RAM are referenced in the following manner:

CxHy0 = $b_1/2$

CxHy1 = b_2

CxHy2 = $-a_1/2$

CxHy3 = $-a_2$

CxHy4 = $b_0/2$

The x represents the channel and the y the biquad number. For example C3H41 is the $b_0/2$ coefficient in the fourth biquad for channel 3

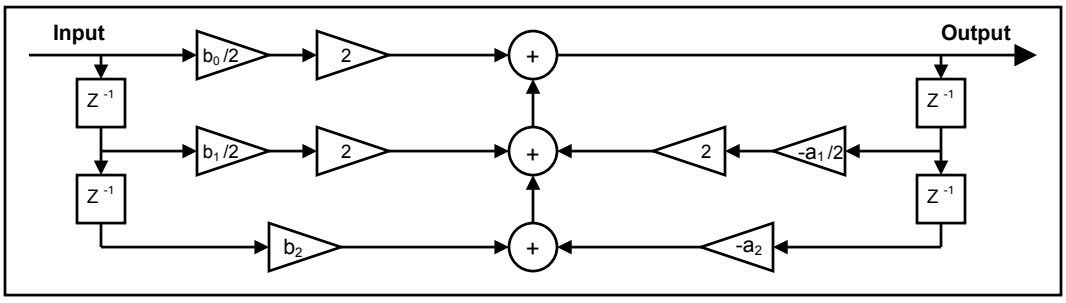


Figure 21 - Biquad Filter

4.2 Pre-Scale

The Pre-Scale block which precedes the first biquad is used for attenuation when filters are designed that boost frequencies above 0dBFS. This is a single 28-bit signed multiplier, with 800000h = -1 and 7FFFFFh = 0.9999998808. By default, all pre-scale factors are set to 800000h.

Note that the default pre-scale value inverts the signal phase. This should be understood when the output is taken from the I^2S output interface.

4.3 Post-Scale

The DDX-8001 provides one additional multiplication after the last interpolation stage and before the distortion compensation on each channel. This is a 24-bit signed fractional multiplier. The scale factor for this multiplier is loaded into RAM using the same I^2C registers as the biquad coefficients and the bass-management. All channels can use the same settings as channel 1 by setting the post-scale link bit.

4.4 Mixing

The DDX-8001 provides two mixing blocks per channel, one located before the EQ section and the other located after. Each mix block has 8 mixing coefficients, which are each 24-bit signed fractional multipliers, that correspond to the 8 channels of input to the mixing block. These coefficients are accessible via the User Controlled Coefficient RAM described below.

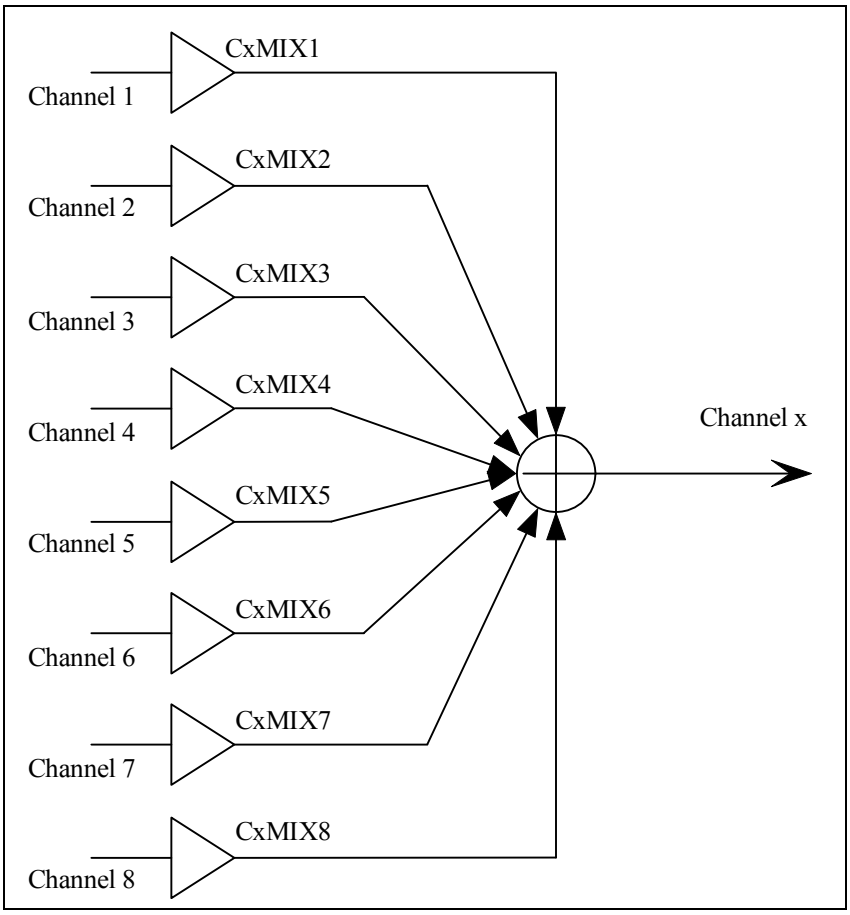


Figure 22 - Mix Block Diagram

4.5 Calculating 24-Bit Signed Fractional Numbers from a dB Value

The pre-scale, mixing, and post-scale functions of the DDX-8001 use 24-bit signed fractional multipliers to attenuate signals. These attenuations can also invert the phase and therefore range in value from –1 to +1. It is possible to calculate the coefficient to utilize for a given negative dB value (attenuation) via the equations below.

Non-Inverting Phase Numbers 0 to +1 :

Coefficient = Round(8388607 * 10^(dB/20))

Inverting Phase Numbers 0 to –1 :

Coefficient = 16777216 - Round(8388607 * 10^(dB/20))

As can be seen by the preceding equations, the value for positive phase 0dB is 0x7FFFFF and the value for negative phase 0dB is 0x800000.

4.6 User Defined Coefficient RAM

4.6.1 Coefficient Address Register 1 (Address 3Bh)

D7	D6	D5	D4	D3	D2	D1	D0
						CFA9	CFA8
						0	0

4.6.2 Coefficient Address Register 2 (Address 3Ch)

D7	D6	D5	D4	D3	D2	D1	D0
CFA7	CFA6	CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0	0	0	0	0	0	0	0

4.6.3 Coefficient b1Data Register Bits 23..16 (Address 3Dh)

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

4.6.4 Coefficient b1Data Register Bits 15..8 (Address 3Eh)

D7	D6	D5	D4	D3	D2	D1	D0
C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0	0	0	0	0	0	0	0

4.6.5 Coefficient b1Data Register Bits 7..0 (Address 3Fh)

D7	D6	D5	D4	D3	D2	D1	D0
C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0	0	0	0	0	0	0	0

4.6.6 Coefficient b2 Data Register Bits 23..16 (Address 40h)

D7	D6	D5	D4	D3	D2	D1	D0
C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0	0	0	0	0	0	0	0

4.6.7 Coefficient b2 Data Register Bits 15..8 (Address 41h)

D7	D6	D5	D4	D3	D2	D1	D0
C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0	0	0	0	0	0	0	0

4.6.8 Coefficient b2 Data Register Bits 7..0 (Address 42h)

D7	D6	D5	D4	D3	D2	D1	D0
C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0	0	0	0	0	0	0	0

4.6.9 Coefficient a1 Data Register Bits 23..16 (Address 43h)

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

4.6.10 Coefficient a1 Data Register Bits 15..8 (Address 44h)

D7	D6	D5	D4	D3	D2	D1	D0
C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0	0	0	0	0	0	0	0

4.6.11 Coefficient a1 Data Register Bits 7..0 (Address 45h)

D7	D6	D5	D4	D3	D2	D1	D0
C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0	0	0	0	0	0	0	0

4.6.12 Coefficient a2 Data Register Bits 23..16 (Address 46h)

D7	D6	D5	D4	D3	D2	D1	D0
C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0	0	0	0	0	0	0	0

4.6.13 Coefficient a2 Data Register Bits 15..8 (Address 47h)

D7	D6	D5	D4	D3	D2	D1	D0
C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0	0	0	0	0	0	0	0

4.6.14 Coefficient a2 Data Register Bits 7..0 (Address 48h)

D7	D6	D5	D4	D3	D2	D1	D0
C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0	0	0	0	0	0	0	0

4.6.15 Coefficient b0 Data Register Bits 23..16 (Address 49h)

D7	D6	D5	D4	D3	D2	D1	D0
C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0	0	0	0	0	0	0	0

4.6.16 Coefficient b0 Data Register Bits 15..8 (Address 4Ah)

D7	D6	D5	D4	D3	D2	D1	D0
C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0	0	0	0	0	0	0	0

4.6.17 Coefficient b0 Data Register Bits 7..0 (Address 4Bh)

D7	D6	D5	D4	D3	D2	D1	D0
C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0	0	0	0	0	0	0	0

4.6.18 Coefficient Write Control Register (Address 4Ch)

D7	D6	D5	D4	D3	D2	D1	D0
						WA	W1
						0	0

Coefficients for EQ and Bass Management are handled internally in the DDX-8001 via RAM. Access to this RAM is available to the user via an I^2C register interface. A collection of I^2C registers are dedicated to this function. Two registers contain a coefficient base address, five sets of three registers store the values of the 24-bit coefficients to be written or that were read, and one contains bits used to control the write of the coefficient (s) to RAM. The following are instructions for reading and writing coefficients.

Reading a coefficient from RAM

- write top 2-bits of address to I^2C register 3Bh
- write bottom 8-bits of address to I^2C register 3Ch
- read top 8-bits of coefficient in I^2C address 3Dh
- read middle 8-bits of coefficient in I^2C address 3Eh
- read bottom 8-bits of coefficient in I^2C address 3Fh

Reading a set of coefficients from RAM

- write top 2-bits of address to I^2C register 3Bh
- write bottom 8-bits of address to I^2C register 3Ch
- read top 8-bits of coefficient in I^2C address 3Dh
- read middle 8-bits of coefficient in I^2C address 3Eh
- read bottom 8-bits of coefficient in I^2C address 3Fh
- read top 8-bits of coefficient b2 in I^2C address 40h
- read middle 8-bits of coefficient b2 in I^2C address 41h

- read bottom 8-bits of coefficient b2 in I²C address 42h
- read top 8-bits of coefficient a1 in I²C address 43h
- read middle 8-bits of coefficient a1 in I²C address 44h
- read bottom 8-bits of coefficient a1 in I²C address 45h
- read top 8-bits of coefficient a2 in I²C address 46h
- read middle 8-bits of coefficient a2 in I²C address 47h
- read bottom 8-bits of coefficient a2 in I²C address 48h
- read top 8-bits of coefficient b0 in I²C address 49h
- read middle 8-bits of coefficient b0 in I²C address 4Ah
- read bottom 8-bits of coefficient b0 in I²C address 4Bh

Writing a single coefficient to RAM

- write top 2-bits of address to I²C register 3Bh
- write bottom 8-bits of address to I²C register 3Ch
- write top 8-bits of coefficient in I²C address 3Dh
- write middle 8-bits of coefficient in I²C address 3Eh
- write bottom 8-bits of coefficient in I²C address 3Fh
- write 1 to W1 bit in I²C address 4Ch

Writing a set of coefficients to RAM

- write top 2-bits of starting address to I²C register 3Bh
- write bottom 8-bits of starting address to I²C register 3Ch
- write top 8-bits of coefficient b1 in I²C address 3Dh
- write middle 8-bits of coefficient b1 in I²C address 3Eh
- write bottom 8-bits of coefficient b1 in I²C address 3Fh
- write top 8-bits of coefficient b2 in I²C address 40h
- write middle 8-bits of coefficient b2 in I²C address 41h
- write bottom 8-bits of coefficient b2 in I²C address 42h
- write top 8-bits of coefficient a1 in I²C address 43h
- write middle 8-bits of coefficient a1 in I²C address 44h
- write bottom 8-bits of coefficient a1 in I²C address 45h
- write top 8-bits of coefficient a2 in I²C address 46h
- write middle 8-bits of coefficient a2 in I²C address 47h
- write bottom 8-bits of coefficient a2 in I²C address 48h
- write top 8-bits of coefficient b0 in I²C address 49h
- write middle 8-bits of coefficient b0 in I²C address 4Ah
- write bottom 8-bits of coefficient b0 in I²C address 4Bh
- write 1 to WA bit in I²C address 4Ch

The mechanism for writing a set of coefficients to RAM provides a method of updating the five coefficients corresponding to a given biquad (filter) simultaneously to avoid possible unpleasant acoustic side-effects. When using this technique, the 10-bit address would specify the address of the biquad b1 coefficient (e.g. 0, 5, 10, 15, …, 100, … 395 decimal), and the DDX-8001 will generate the RAM addresses as offsets from this base value to write the complete set of coefficient data.

Table 36 - RAM Block for Biquads, Mixing, and Scaling

Index (Decimal)	Index (Hex)		Coefficient	Default
0	00h	Channel 1 – Biquad 1	C1H10 (b1/2)	000000h
1	01h		C1H11 (b2)	000000h
2	02h		C1H12 (a1/2)	000000h
3	03h		C1H13 (a2)	000000h
4	04h		C1H14 (b0/2)	400000h
5	05h	Channel 1 – Biquad 2	C1H20	000000h
…	…	…	…	…
49	31h	Channel 1 – Biquad 10	C1HA4	400000h
50	32h	Channel 2 – Biquad 1	C2H10	000000h
51	33h		C2H11	000000h
…	…	…	…	…
99	63h	Channel 2 – Biquad 10	C2HA4	400000h
100	64h	Channel 3 – Biquad 1	C3H10	000000h
…	…	…	…	…
399	18Fh	Channel 8 – Biquad 10	C8HA4	400000h
400	190h	Channel 1 – Pre-Scale	C1PreS	7FFFFFh
401	191h	Channel 2 – Pre-Scale	C2PreS	7FFFFFh
402	192h	Channel 3 – Pre-Scale	C3PreS	7FFFFFh
…	…	…	…	…
407	197h	Channel 8 – Pre-Scale	C8PreS	7FFFFFh
408	198h	Channel 1 – Post-Scale	C1PstS	7FFFFFh
409	199h	Channel 2 – Post-Scale	C2PstS	7FFFFFh
…	…	…	…	…
415	19Fh	Channel 8 – Post-Scale	C8PstS	7FFFFFh
416	1A0h	Channel 1 – Mix#1 1	C1MX11	7FFFFFh
417	1A1h	Channel 1 – Mix#1 2	C1MX12	000000h
…	…	…	…	…
423	1A7h	Channel 1 – Mix#1 8	C1MX18	000000h
424	1A8h	Channel 2 – Mix#1 1	C2MX11	000000h
425	1A9h	Channel 2 – Mix#1 2	C2MX12	7FFFFFh
…	…	…	…	…
479	1DFh	Channel 8 – Mix#1 8	C8MX18	7FFFFFh
480	1E0h	Channel 1 – Mix#2 1	C1MX21	7FFFFFh
481	1E1h	Channel 1 – Mix#2 2	C1MX22	000000h
…	…	…	…	…
487	1E7h	Channel 1 – Mix#2 8	C1MX28	000000h
488	1E8h	Channel 2 – Mix#2 1	C2MX21	000000h
489	1E9h	Channel 2 – Mix#2 2	C2MX22	7FFFFFh
…	…	…	…	…
543	21Fh	Channel 8 – Mix#2 8	C8MX28	7FFFFFh

Variable Max Power Correction (Address 4Dh-4Eh):

MPCC bits determine the 16 MSBs of the MPC compensation coefficient. This coefficient is used in place of the default coefficient when MPCV = 1.

D7	D6	D5	D4	D3	D2	D1	D0
MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0	0	1	0	1	1	0	1
MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
1	1	0	0	0	0	0	0

129 Morgan Drive, Norwood, MA 02062 voice: (781) 551-9450 fax: (781) 440-9528 email: apogee@apogeeddx.com

PSCorrect™ (Address 51h-53h):

An ADC is used to input ripple data to SDI78. The left channel (7) is used internally. No audio data can therefore be input on these channels (7 and 8). Though all channel mapping and mixing from other inputs to channels 7 and 8 internally are still valid.

Ripple Correction Value – RCV

Correction Normalization Value – CNV

D7	D6	D5	D4	D3	D2	D1	D0
RCV11	RCV10	RCV9	RCV8	RCV7	RCV6	RCV5	RCV4
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
RCV3	RCV2	RCV1	RCV0	CNV11	CNV10	CNV9	CNV8
0	0	0	0	1	1	1	1

D7	D6	D5	D4	D3	D2	D1	D0
CNV7	CNV6	CNV5	CNV4	CNV3	CNV2	CNV1	CNV0
1	1	1	1	1	1	1	1

129 Morgan Drive, Norwood, MA 02062 voice: (781) 551-9450 fax: (781) 440-9528 email: apogee@apogeeddx.com

5.0 Design Information

Schematic Diagram

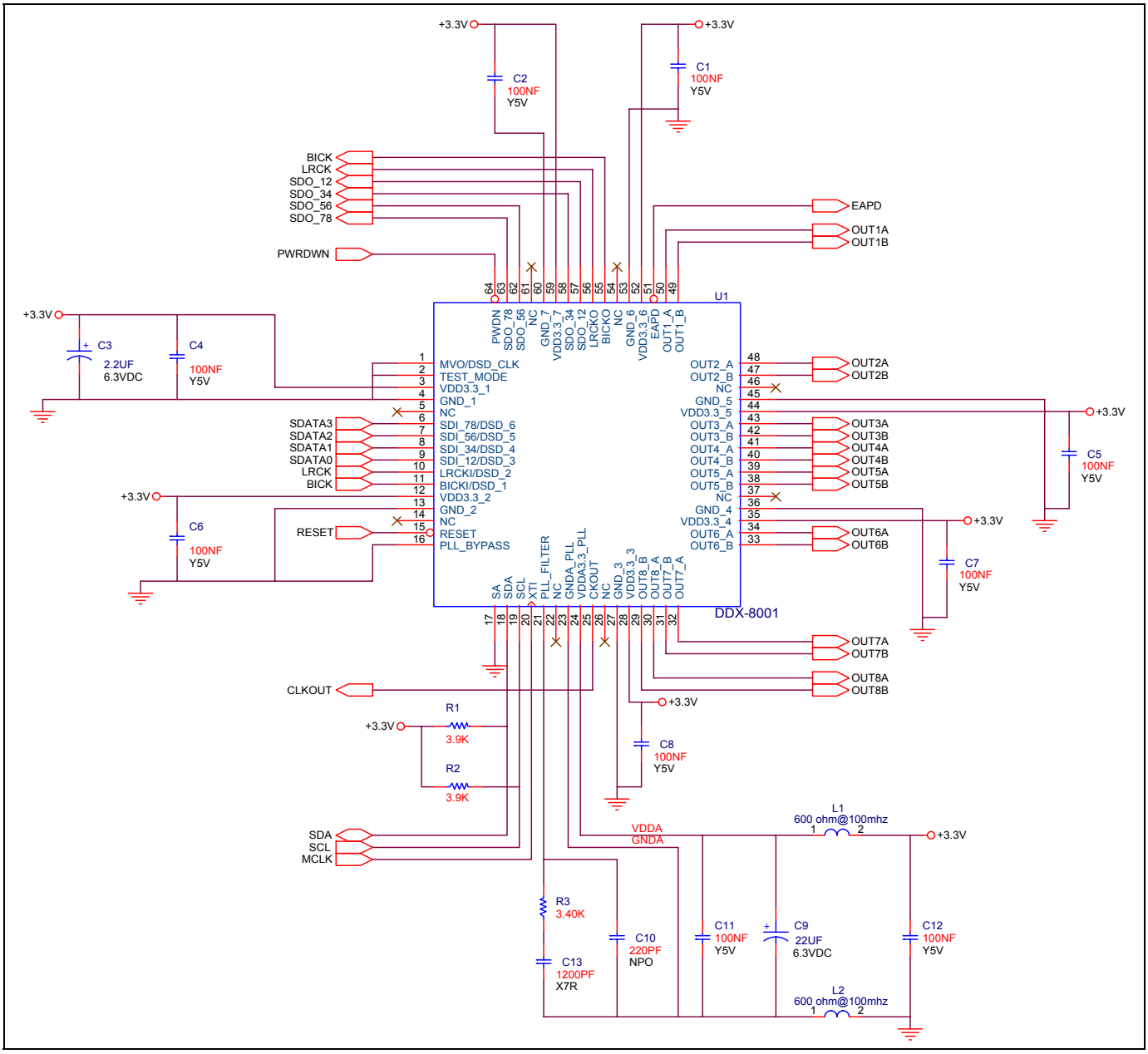
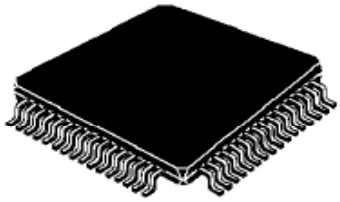


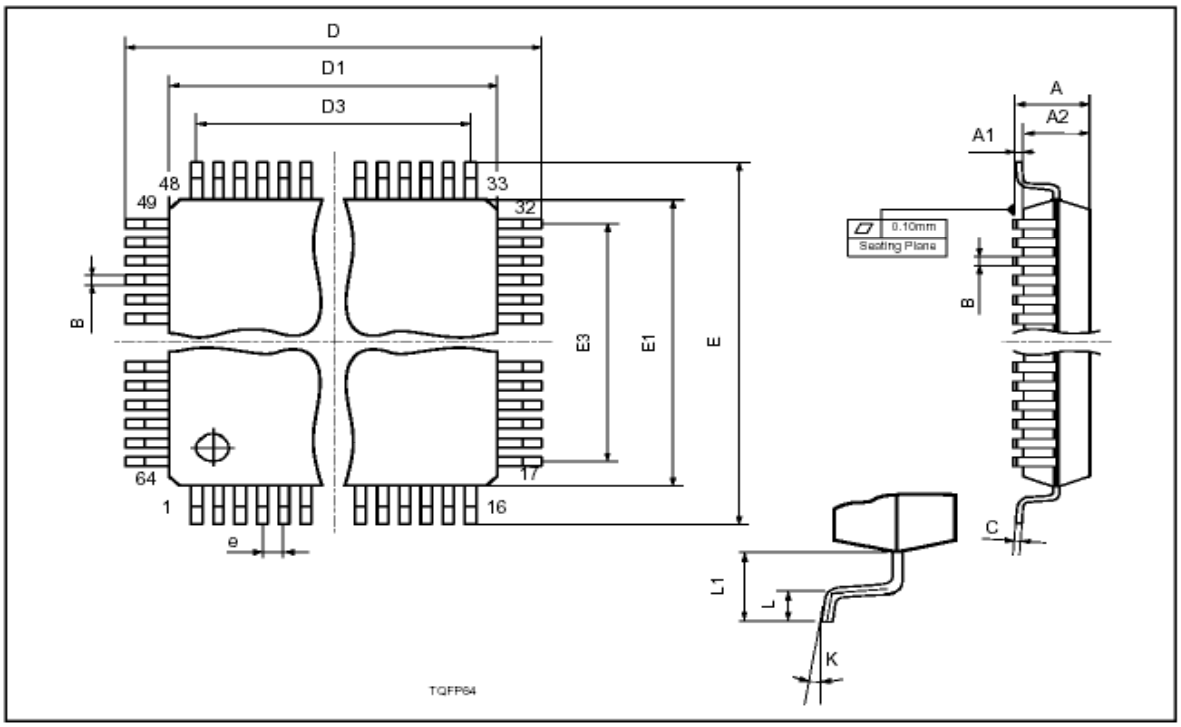
Figure 23 - Schematic Diagram.

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.18	0.23	0.28	.007	0.009	0.011
C	0.12	0.16	0.20	0.0047	0.0063	0.0079
D		12.0			0.472	
D1		10.0			0.394	
D3		7.50			0.295	
e		0.50			0.0197	
E		12.0			0.472	
E1		10.0			0.394	
E3		7.50			0.295	
L	0.40	0.60	0.75	0.0157	0.0236	0.0295
L1		1.00			0.0393	
K	0°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP64



This is preliminary information on a new product. Specifications are subject to change without notice.