DDTA (LO-R1) U

PNP PRE-BIASED 100 mA SOT-323 SURFACE MOUNT TRANSISTOR

SPICE MODELS: DDTA122LU DDTA142JU DDTA122TU DDTA142TU

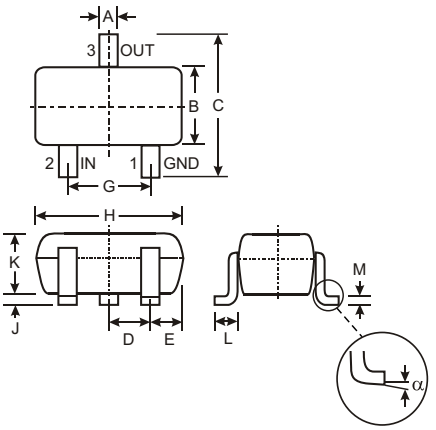
NEW PRODUCT

Features

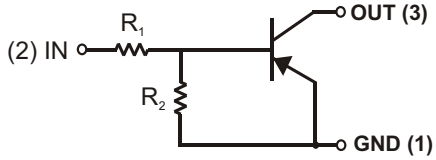
- Epitaxial Planar Die Construction
- Complementary NPN Types Available (DDTC)
- Built-In Biasing Resistors
- Lead Free Product

Mechanical Data

- Case: SOT-323, Molded Plastic
- Case material - UL Flammability Rating 94V-0
- Moisture sensitivity: Level 1 per J-STD-020A
- Terminals: Finish - Matte Tin (Note 1) Solderable per MIL-STD-202, Method 208
- Terminal Connections: See Diagram
- Marking: Date Code and Marking Code (See Diagrams & Page 2)
- Weight: 0.006 grams (approx.)
- Ordering Information (See Page 2)



SOT-323		
Dim	**Min**	**Max**
A	0.25	0.40
B	1.15	1.35
C	2.00	2.20
D	0.65 Nominal	
E	0.30	0.40
G	1.20	1.40
H	1.80	2.20
J	0.0	0.10
K	0.90	1.00
L	0.25	0.40
M	0.10	0.18
α	0°	8°
All Dimensions in mm		



P/N	R1 (NOM)	R2 (NOM)	MARKING
DDTA122LU	0.22KΩ	10KΩ	P81
DDTA142JU	0.47KΩ	10KΩ	P82
DDTA122TU	0.22KΩ	OPEN	P83
DDTA142TU	0.47KΩ	OPEN	P84

Maximum Ratings @ T_A = 25°C unless otherwise specified

Characteristic		Symbol	Value	Unit
Supply Voltage, (3) to (1)		V_{CC}	-50	V
Input Voltage, (2) to (1)	DDTA122LU DDTA142JU	V_{IN}	+5 to -6 +5 to -6	V
Input Voltage, (1) to (2)	DDTA122TU DDTA142TU	$V_{EBO\ (MAX)}$	-5	V
Output Current	All	I_C	-100	mA
Power Dissipation (Note 2)		P_d	200	mW
Thermal Resistance, Junction to Ambient Air (Note 2)		$R_{\theta JA}$	625	°C/W
Operating and Storage and Temperature Range		T_j, T_{STG}	-55 to +150	°C

Note: 1. If lead-bearing terminal plating is required, please contact your Diodes Inc. sales representative for availability and minimum order details.
2. Mounted on FR4 PC Board with recommended pad layout at http://www.diodes.com/datasheets/ap02001.pdf.

Electrical Characteristics @ T_A = 25°C unless otherwise specified — R1, R2 Types

Characteristic		Symbol	Min	Typ	Max	Unit	Test Condition
Input Voltage	DDTA122LU DDTA142JU	$V_{I(off)}$	-0.3 -0.3	—	—	V	V_{CC} = -5V, I_O = -100μA
	DDTA122LU DDTA142JU	$V_{I(on)}$	—	—	-2.0 -2.0	V	V_O = -0.3V, I_O = -20mA V_O = -0.3V, I_O = -20mA
Output Voltage		$V_{O(on)}$	—	—	-0.3V	V	I_O/I_I = -5mA/-0.25mA
Input Current	DDTA122LU DDTA142JU	I_I	—	—	-28 -13	mA	V_I = -5V
Output Current		$I_{O(off)}$	—	—	-0.5	μA	V_{CC} = -50V, V_I = 0V
DC Current Gain	DDTA122LU DDTA142JU	G_I	56 56	—	—	—	V_O = -5V, I_O = -10mA
Gain-Bandwidth Product*		f_T	—	200	—	MHz	V_{CE} = -10V, I_E = -5mA, f = 100MHz

* Transistor - For Reference Only

Electrical Characteristics @ T_A = 25°C unless otherwise specified — R1-Only Types

Characteristic		Symbol	Min	Typ	Max	Unit	Test Condition
Collector-Base Breakdown Voltage		BV_{CBO}	-50	—	—	V	I_C = -50μA
Collector-Emitter Breakdown Voltage		BV_{CEO}	-40	—	—	V	I_C = -1mA
Emitter-Base Breakdown Voltage	DDTA122TU DDTA142TU	BV_{EBO}	-5	—	—	V	I_E = -50μA I_E = -50μA
Collector Cutoff Current		I_{CBO}	—	—	-0.5	μA	V_{CB} = -50V
Emitter Cutoff Current	DDTA122TU DDTA142TU	I_{EBO}	— —	—	-0.5 -0.5	μA	V_{EB} = -4V
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	—	—	-0.3	V	I_C = -5mA, I_B = -0.25mA
DC Current Transfer Ratio	DDTA122TU DDTA142TU	h_{FE}	100 100	250 250	600 600	—	I_C = -1mA, V_{CE} = -5V
Gain-Bandwidth Product*		f_T	—	200	—	MHz	V_{CE} = -10V, I_E = 5mA, f = 100MHz

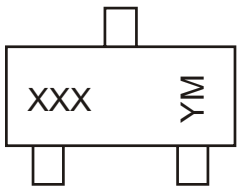
* Transistor - For Reference Only

Ordering Information (Note 3)

Device	Packaging	Shipping
DDTA122LU-7	SOT-323	3000/Tape & Reel
DDTA142JU-7	SOT-323	3000/Tape & Reel
DDTA122TU-7	SOT-323	3000/Tape & Reel
DDTA142TU-7	SOT-323	3000/Tape & Reel

Notes: 1. If lead-bearing terminal plating is required, please contact your Diodes Inc. sales representative for availability and minimum order details.
3. For Packaging Details, go to our website at http://www.diodes.com/datasheets/ap02007.pdf.
4. For Lead Free version (with Lead Free terminal finish) part number, please add "-F" suffix to part number above. Example: DDTA142TU-7-F.

Marking Information



XXX = Product Type Marking Code
See Sheet 1 Diagrams
YM = Date Code Marking
Y = Year ex: P = 2003
M = Month ex: 9 = September

Date Code Key

Year	2002	2003	2004	2005	2006	2007	2008	2009
Code	N	P	R	S	T	U	V	W

Month	Jan	Feb	March	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

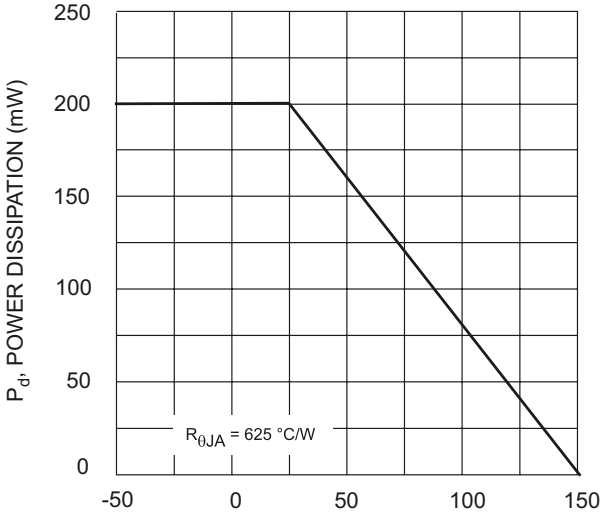


Fig. 1 Power Derating Curve