GENERAL DESCRIPTION

DAC1253X is a CMOS 12Bit D/A converter for general application. This digital to analog converter has a R-string structure. Its settling time is 500ns (Typical value).

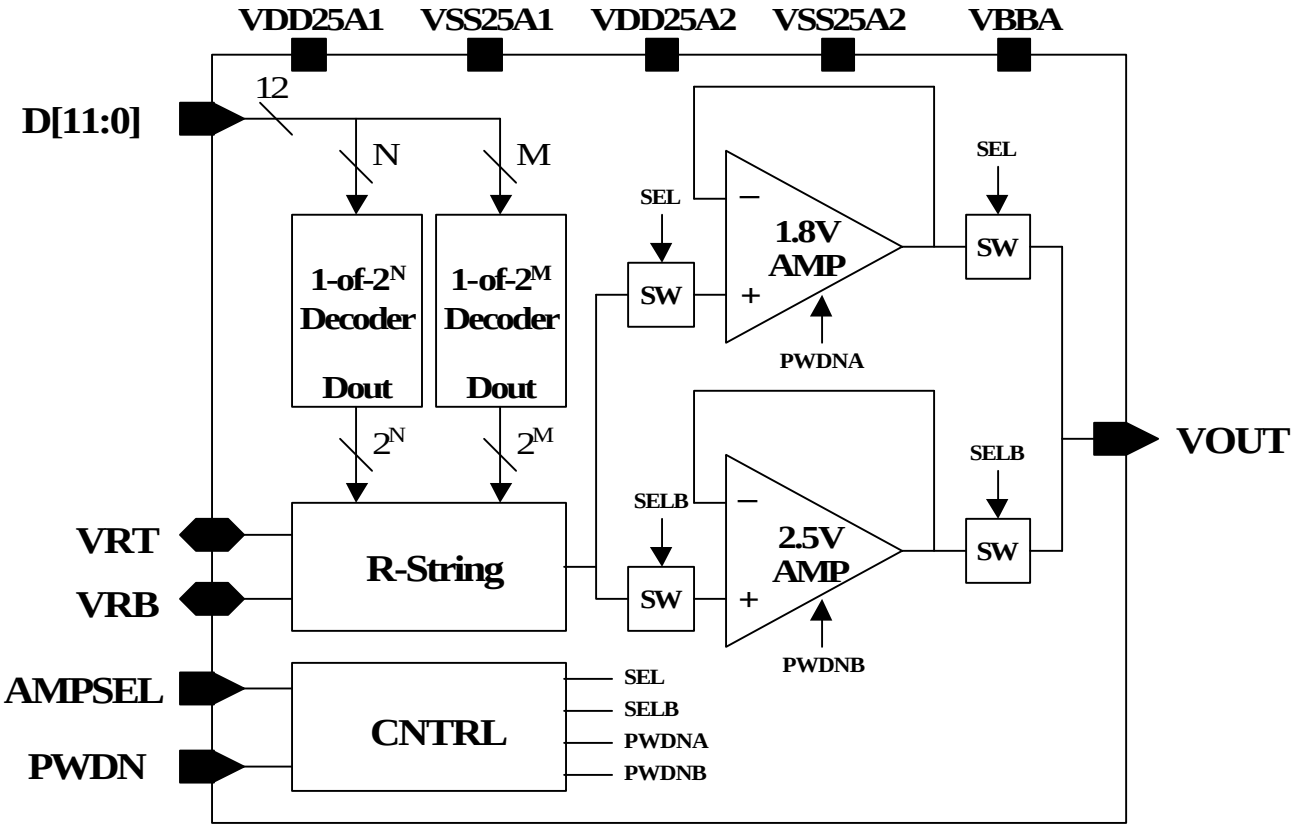
FEATURES

— Resolution: 12Bit
— Differential Linearity Error: ± 1.0 LSB
— Integral Linearity Error: ± 4.0 LSB
— Settling Time: 500ns
— Low Power Consumption: 890μA
— Power Down Mode
— Operation Temperature Range: 0°C ~ 70°C
— Power Supply: 2.5V Single

TYPICAL APPLICATIONS

— Hard Disk Driver (HDD)
— Battery Operated Instruments
— Motor Control Systems
— General Applications

FUNCTIONAL BLOCK DIAGRAM



Ver 1.8 (June 2003)

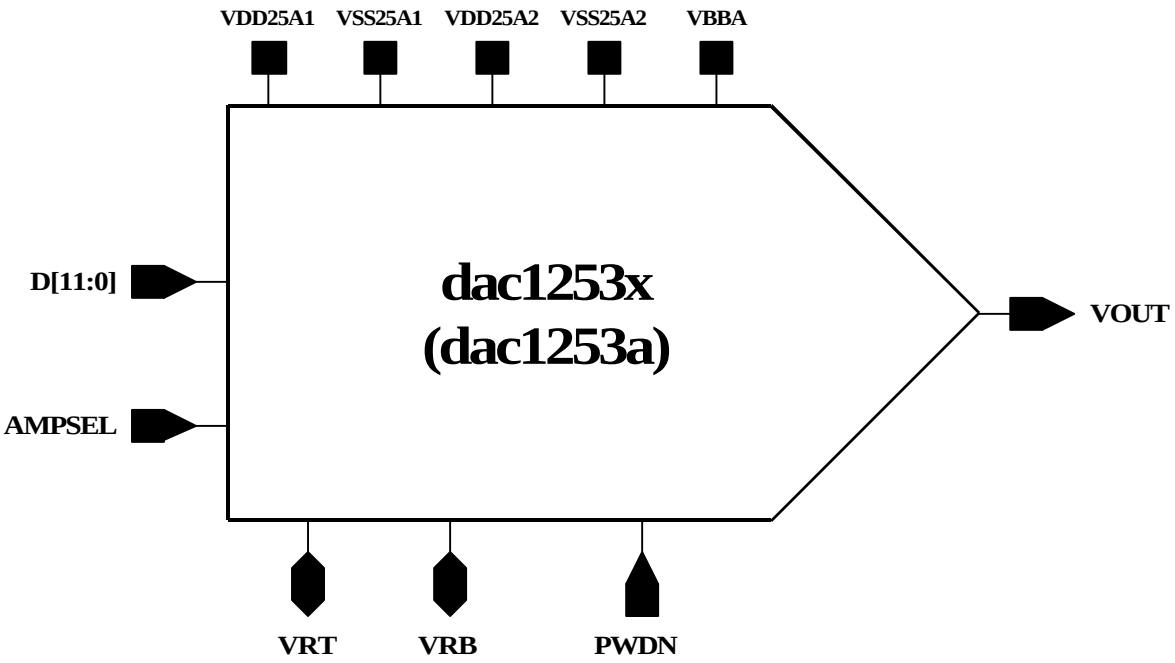
CORE PIN DESCRIPTION

Name	I/O Type	I/O Pad	Pin Description
D[11:0]	DI	picc_abb	Digital Input Data (12bit) D[11]: MSB, D[0]: LSB
AMPSEL	DI	picc_abb	Amp Selection (Low: 2.5V Amp)
PWDN	DI	picc_abb	Power Down (Active Low)
VRT	AB	pia_abb	Voltage Reference Top
VRB	AB	pia_abb	Voltage Reference Bottom
VOUT	AO	poa_abb	Analog Voltage Output
VDD25A1	AP	vdd2t_abb	Analog Power (+2.5V)
VSS25A1	AG	vdd2t_abb	Analog Ground (0.0V)
VDD25A2	DP	vdd2t_abb	Digital Power (+2.5V)
VSS25A2	DG	vss2t_abb	Digital Ground (0.0V)
VBBA	AG	vbb_abb	Analog Sub Bias (0.0V)

I/O TYPE ABBR.

— AI: Analog Input
— DI: Digital Input
— AO: Analog Output
— DO: Digital Output
— AB: Analog Bidirectional
— DB: Digital Bidirectional
— AP: Analog Power
— DP: Digital Power
— AG: Analog Ground
— DG: Digital Ground

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	VDD (VDD25A1, VDD25A2)	3.3	V
Analog Output Voltage	VOUT	VSS25A1 to VDD25A1	V
Digital Input Voltage	D[11:0]	VSS25A2 to VDD25A2	V
Reference Voltage	VRT VRB	VDD25A1 VSS25A1	V
Operating Temperature Range	Topr	0 to 70	°C

NOTES:

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS(VSS25A1 or VSS25A2 or VBBA) unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD25A1 - VSS25A1 VDD25A2 - VSS25A2	2.375	2.5	2.625	V
Supply Voltage Difference	VDD25A1 - VDD25A2	-0.1	0.0	0.1	V
Reference Voltage	VRT VRB	- VSS25A1	- -	VDD25A1 -	V
Digital Input 'Low' Voltage Digital Input 'High' Voltage	VIL VIH	- 0.7VDD	- -	0.3VDD -	V
Operating Temperature	Topr	0	-	70	°C

NOTES:

1. It is strongly recommended that to avoid power latch-up all the supply pins (VDD18A1 , VDD18A2) be driven from the same source.
2. Digital Input: VDD → VDD25A2

DC ELECTRICAL CHARACTERISTICS

(Converter Specifications: VDD25A1=VDD25A2=2.5V, VSS25A1=VSS25A2=VBBA=0V, AMPSEL=Low, PWDN=High, Top=25°C, VRT=2.5V, VRB=0.0V unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Resolution	Bit	-	12	-	Bits	-
Differential Linearity Error	DLE	-	1.0	-	LSB	-
Integral Linearity Error	ILE	-	4.0	-	LSB	-
Zero Scale Error[1]	V_{ZSE}	-	5	-	mV	VRT=2.5V , VRB=0.0V
Full Scale Voltage Error[2]	V_{FSE}	-	5	-	mV	
Maximum Output Voltage	Vo_{MAX}	-	2.499	-	V	Vo_{MAX} = VOUT(D[11:0]=High)
LSB Size	V_{LSB}	-	0.61	-	mV	V_{LSB} = Vo_{MAX} / 4095

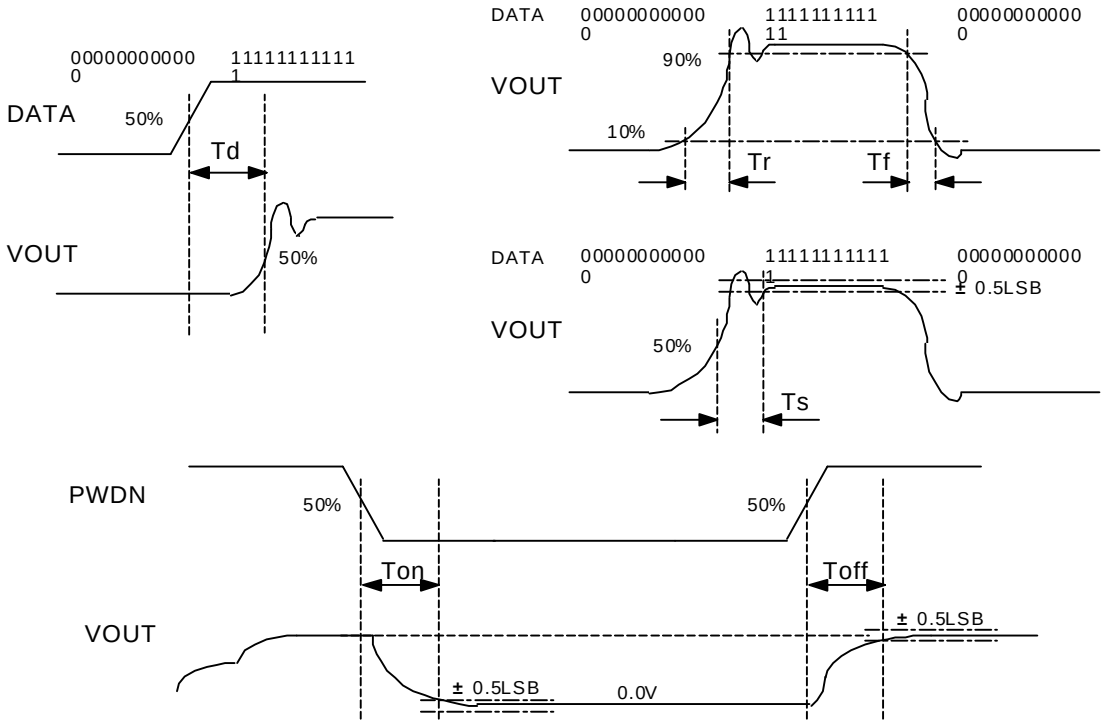
NOTES:
1. V_{ZSE} = VOUT(D[11:0]=Low) - VRB
2. V_{FSE} =VOUT(D[11:0]=High) - {(VRT-VRB) × 4095/4096 + VRB}

AC ELECTRICAL CHARACTERISTICS

(Converter Specifications: VDD25A1=VDD25A2=2.5V, VSS25A1=VSS25A2=VBBA=0V, load cap=25pF AMPSEL=Low, Top=25°C, VRT=2.45V, VRB=0.05V unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Supply Current	Ivdd1	-	0.89	-	mA	Ivdd1 = I_{VDDA} + I_{VDDD} VRT=2.5V, VRB = 0.0V Data Input: All Low or All High
Supply Current	Ivdd2	-	1.22	-	mA	Ivdd2 = I_{VDDA} + I_{VDDD} Data Input: All Low or All High
Supply Current (Power Down Mode)	Ivdd3	-	-	10	uA	Ivdd3 = I_{VDDA} + I_{VDDD} Data Rate = 2MHz Load cap = 25pF, PWDN=LOW
Short Circuit Current	I_{SC}	-	12	-	mA	VOUT: VSSA or VDDA Data Input: All High or All Low
Analog Output Delay	Td	-	65	-	ns	Data Rate = 2MHz Data: All LOW → All HIGH
Analog Output Rise Time	Tr	-	100	-	ns	Data Rate = 2MHz Data: All LOW → All HIGH
Analog Output Fall Time	Tf	-	100	-	ns	Data Rate = 2MHz Data: All HIGH → All LOW
Analog Output Settling Time	Ts	-	500	-	ns	Data Rate = 2MHz Data: All LOW → All HIGH
Power Down On Time	Ton	-	500	-	ns	PWDN: HIGH → LOW
Power Down Off Time	Toff	-	500	-	ns	PWDN: LOW → HIGH

TIMING DIAGRAM



1. Output delay is measured from the 50% point of the rising edge of input data to the full scale transition.
2. Settling time is measured from the 50% point of full scale transition to the output remaining within ±1/2 LSB.
3. Output rise/fall time is measured between the 10% and 90% points of full scale transition.

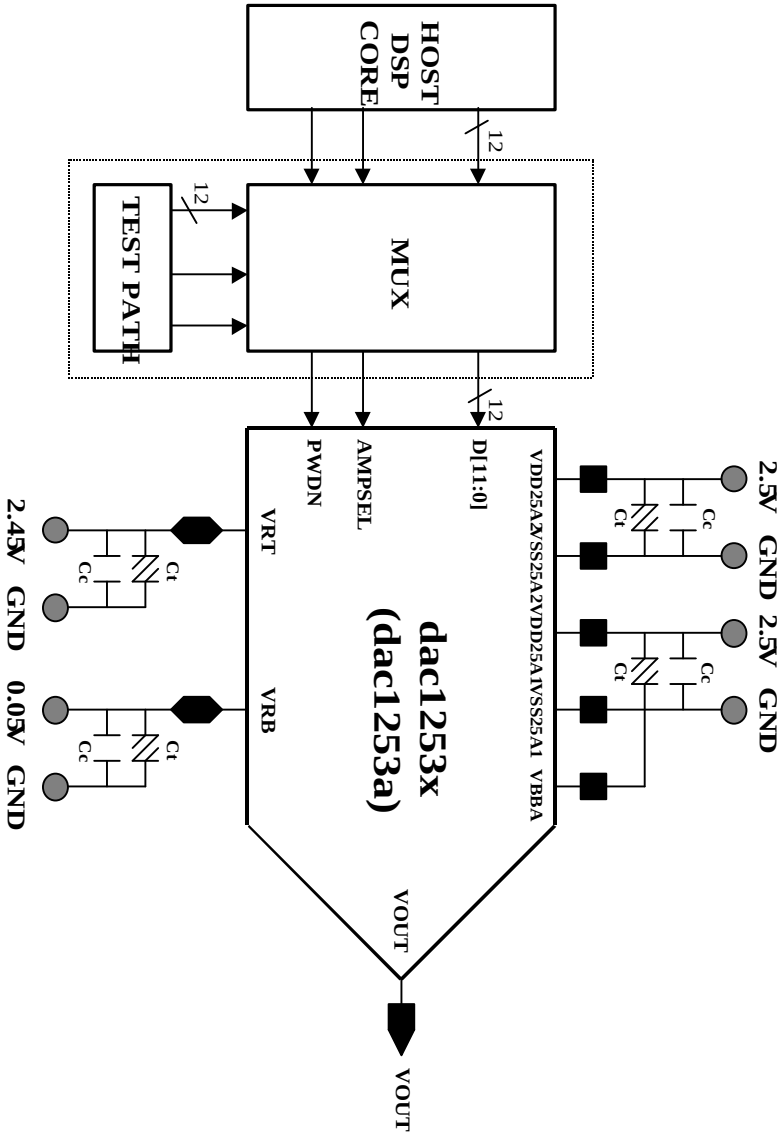
FUNCTIONAL DESCRIPTION

1. The dac1253x(dac1253a) has a 12bit R-string block, two decoders, two OP amps, and control block.
2. The digital outputs of two decoders decide the voltage level of R-string block.

$$V_{Rstring} = \frac{VRT - VRB}{2^{12}} \sum_{n=0}^{11} \left(2^n \times D[n]\right) + VRB$$

3. The two OP amps have different supply voltages. One is operated at 2.5V supply voltage and the other is operated at 1.8V supply voltage. The CNTRL block controls several conditions which are the OP amp selection, and power down mode. If you use the dac1253x(dac1253a) at 2.5V supply voltage, next conditions is needed. (AMPSEL=Low, PWDN=High)
4. The dac1253x(dac1253a) is able to be operated at 1.8V power supply but its mode is a test mode. Therefore no data at 1.8V power supply is written in data sheet.
5. Normal Conditions: VRT=2.45V , VRB=0.05V, AMPSEL=Low , PWDN=High
   You can change the voltages of VRT and VRB to 2.5V and 0.0V , but the performance of dac1253x(dac1253a)
   will be degraded.
6. In power down mode, only analog current ($I_{VDDA25A1}$) is reduced and reference current (Ivrt) is always dissipated.

CORE EVALUATION GUIDE



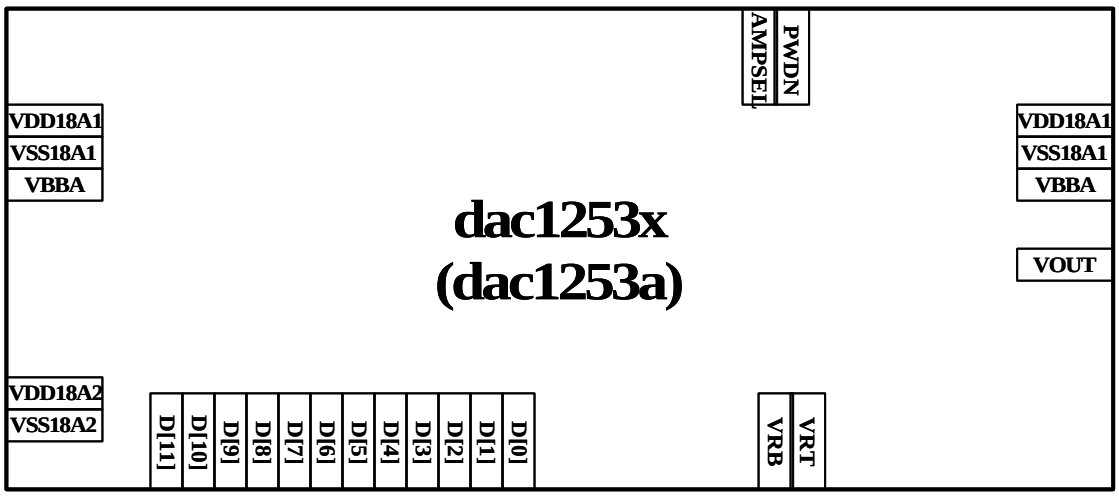
Location	Description
Ct	10µF Tantalum Capacitor
Cc	0.1µF Ceramic Capacitor

TESTABILITY

Whether you use MUX or the internal logic for testability, it is required to be able to select the values of digital inputs (D[11:0]). See above figure. Only if it is, you can check the main function. (Linearity)

Normal Test Condition: VRT=2.45V, VRB=0.05V, AMPSEL=Low, PWDN=High

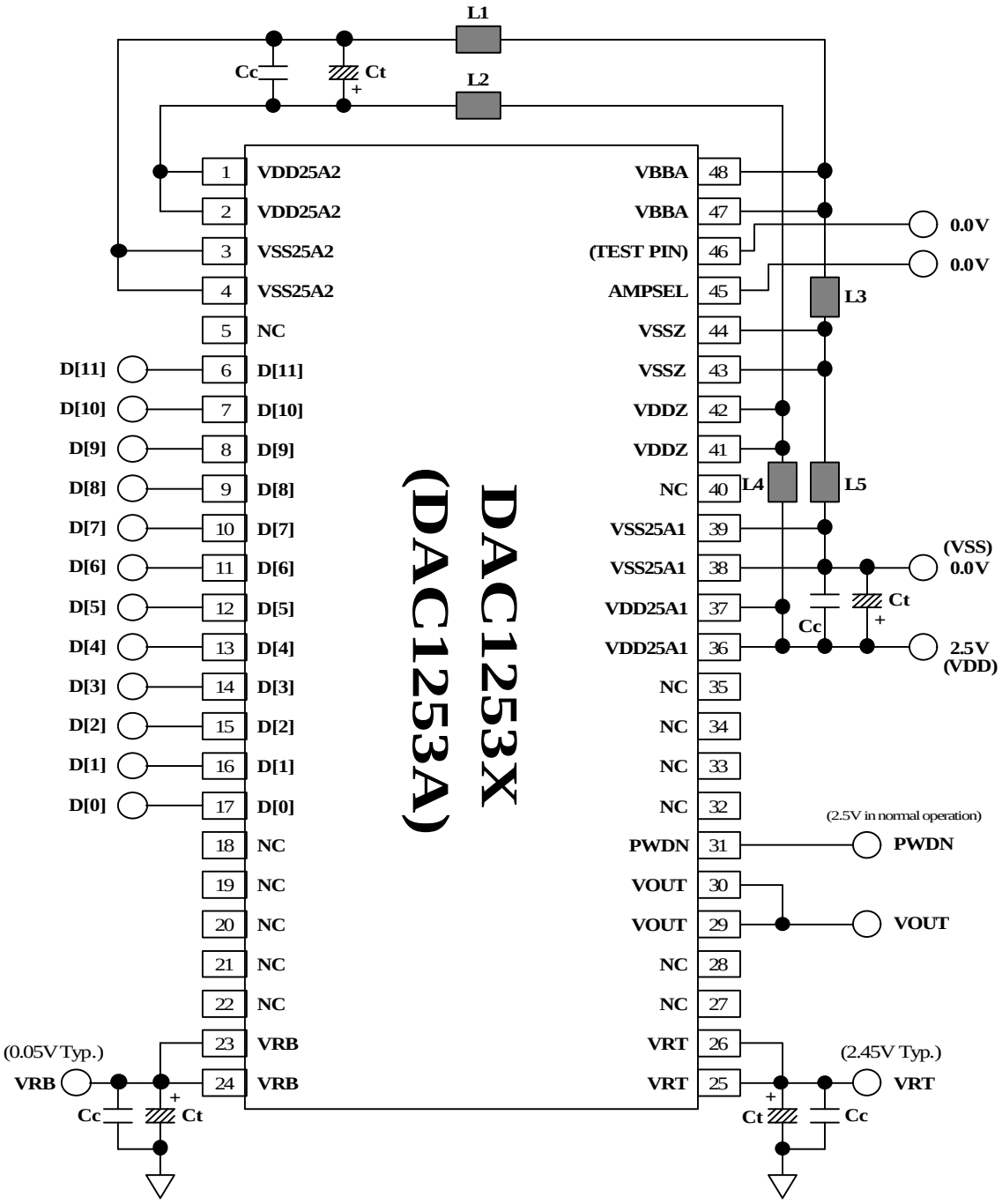
CELL INFORMATION



Pin Name	Property	Pin Usage	Pin Layout Guide
D[11:0]	DI	Internal / External	1. Digital Input Signal lines must have same length to reduce propagation delay.
AMPSEL	DI	Internal / External	
PWDN	DI	Internal / External	
VRT	AB	External	1. Voltage reference lines (VRT and VRB) must be wide metal to reduce voltage drop of metal lines. 2. VOUT signal should not be crossed by any signals and should not run next to digital signals to minimize capacitive coupling between the two signals.
VRB	AB	External	
VOUT	AO	Internal / External	
VDD25A1	AP	External	1. It is recommended that you use thick analog power metal. When connected to PAD, the path should be kept as short as possible. 2. Digital power and analog power are separately used.
VSS25A1	AG	External	
VDD25A2	DP	External	
VSS25A2	DG	External	
VBBA	AG	External	

1. It is recommended that you use thick analog power metal. when connecting to PAD, the path should be kept as short as possible.
2. Digital power and analog power are separately used.
3. When the core block is connected to other blocks, it must be double guard-ring using N-well and P+ active to remove the substrate and coupling noise. In that case, the power metal should be connected to PAD directly.
4. The Bulk power is used to reduce the influence of substrate noise.
5. Digital input signal lines must be same length to reduce the difference of delay.

PACKAGE CONFIGURATION



Location	Description
Ct	10uF Tantalum Capacitor
Cc	0.1uF Ceramic Capacitor
L1~L5	Ferrite Bead (0.1mh)

PACKAGE PIN DESCRIPTION

Name	Pin No	I/O Type	Pin Description
VDD25A2	1,2	DP	Digital Power (2.5V)
VSS25A2	3,4	DG	Digital Ground (0.0V)
D[11:0]	6~17	DI	Digital Input Data
VRB	23,24	AB	Voltage Reference Bottom (0.05V)
VRT	25,26	AB	Voltage Reference Top (2.45V)
VOUT	29,30	AO	Analog Voltage Output
PWDN	31	DI	Power Down Mode (Low Active)
VDD25A1	36,37	AP	Analog Power (2.5V)
VSS25A1	38,39	AG	Analog Ground (0.0V)
VDDZ	41,42	AP	Pad Power (2.5V)
VSSZ	43,44	AG	Pad Ground (0.0V)
AMPSEL	45	DI	Amp Selection Mode (Low: 2.5V Amp Selected)
(TEST PIN)	46	DI	This pin must be connected to ground (0.0V)
VBBA	47,48	AG	Analog Sub Bias (0.0V)
NC	5,18,19 20,21,22,27 28,32,33,34 35,40	DO	No Connection

I/O TYPE ABBR.

— AI: Analog Input
— DI: Digital Input
— AO: Analog Output
— DO: Digital Output
— AB: Analog Bidirectional
— DB: Digital Bidirectional
— AP: Analog Power
— DP: Digital Power
— AG: Analog Ground
— DG: Digital Ground

PC BOARD LAYOUT CONSIDERATION

1. PC BOARD CONSIDERATIONS

To minimize noise on the power lines and the ground lines, the digital inputs need to be shielded and decoupled. This trace length between groups of VDD (VDD25A1,VDD25A2) and VSS (VSS25A1,VSS25A2) pins should be as short as possible so as to minimize inductive ringing.

2. SUPPLY DECOUPLING AND PLANES

For the decoupling capacitor between the power line and the ground line, 0.1uF ceramic capacitor is used in parallel with a 10uF tantalum capacitor. The digital power plane(VDD25A2) and analog power plane(VDD25A1) are connected through a ferrite bead, and also the digital ground plane(VSS25A2) and the analog ground plane(VSS25A1). This ferrite bead should be located within 3inches of the DAC1253X(DAC1253A). The analog power plane supplies power to the DAC1253X(DAC1253A) of the analog output pin and related devices.

FEEDBACK REQUEST

We appreciate your interest in out products. If you have further questions, please specify in the attached form. Thank you very much.

DC / AC Electrical Characteristic					
Characteristics	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
Supply Voltage				V	
Power dissipation				mW	
Resolution				Bits	
Analog Output Voltage				V	
Operating Temperature				°C	
Output Load Capacitor				pF	
Output Load Resistor				kΩ	
Integral Non-Linearity Error				LSB	
Differential Non-Linearity Error				LSB	
Maximum Conversion Rate				MHz	

Voltage Output DAC					
Reference Voltage TOP BOTTOM				V	
Analog Output Voltage Range				V	
Digital Input Format	Binary Code or 2's Complement Code				

Current Output DAC					
Analog Output Maximum Current				mA	
Analog Output Maximum Signal Frequency				kHz	
Reference Voltage				V	
External Resistor for Current Setting (RSET)				kΩ	
Pipeline Delay				sec	

— Do you want power down mode?
— Do you want internal reference voltage (BGR)?
— Which do you want serial input data type or parallel input data type?
— Do you need 3.3V or 5V power supply in your system?

HISTORY CARD

Version	Date	Modified Items	Comments
Ver 1.2	99.12.06	Version updated. All pictures except timing diagram are drawn with power-point. Paper size is A4 but below vacancy is 35. pad name correction: 1t -> 2t NOBUF deleted	
Ver 1.3	99.12.10	Version updated. All pictures except timing diagram are re-drawn with power-point. (power pin symbol) Absolute Maximum Rating: DA[11:0], DB[11:0] -> D[11:0] DC Electrical Characteristics: VRT=2.5V, VRB=0.0V	All pictures are redrawn because of Explore Zip Virus!!
Ver 1.4	99.12.12	Version updated. All texts are re-written to subject/contents style All texts are re-written to editing mode.	Reference data sheet Lee Jong Hwa
Ver 1.5	00.02.22	Version updated. page 8: dac1253x(core name) → DAC1253X(chip name) page 9: VRT/VRB: AI → AB, VBBA : AB → AG	
Ver 1.6	01.03.28	Version Updated. page 11: °C → kΩ (Output Load Resistor)	
Ver 1.7	02.05.13	Version Updated. page 3: Absolute Maximum Rating is modified. page 7: Phantom Cell Information is modified. page 11: W → kΩ and question is modified.	
Ver 1.8	03..6.20	Version updated. Page 5: measured → is measured VDD18A1 → VDD25A1	