GENERAL DESCRIPTION

This core is a CMOS hexa-channel 10bit D/A converter for general & video. The DAC1243X-AL core is in the Samsung 0.25um 2.5V process. Digital inputs are coded as binary. Each DAC channel includes power down control and the ability sense output load. An external(optional) or 0.7V reference voltage (VBIAS) and a external resister define the full-scale current together. It uses the two of current-segment and -weighted.

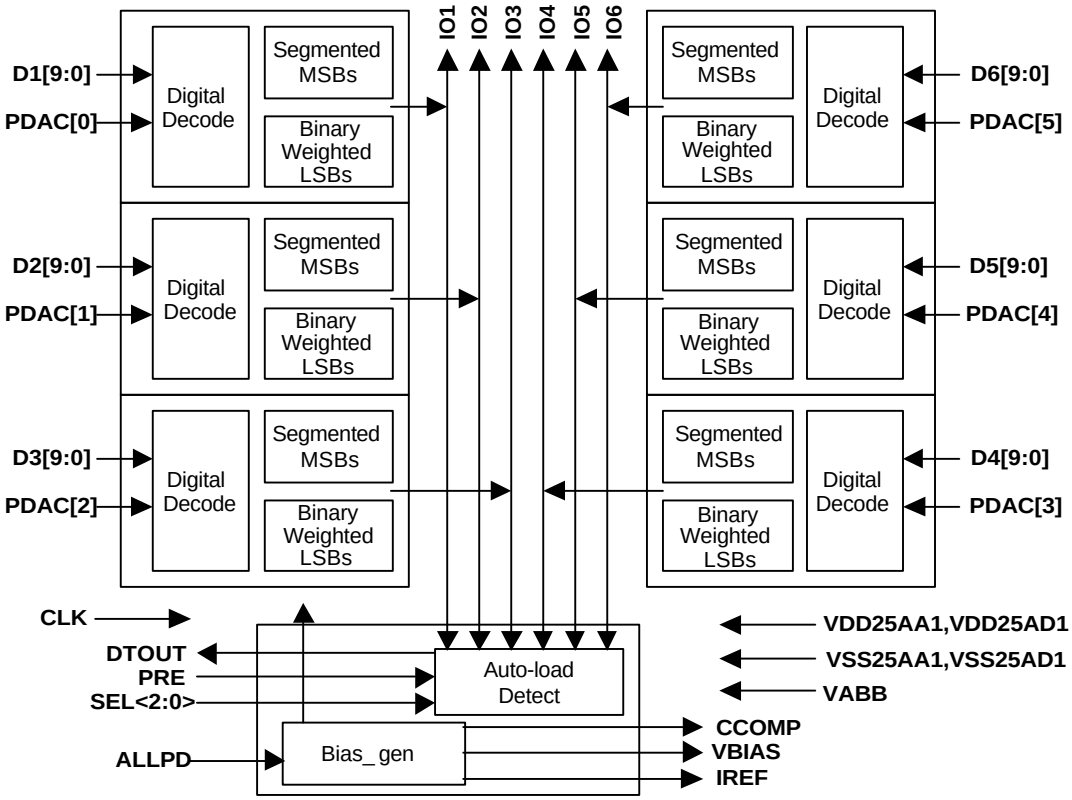
FEATURES

- Maximum conversion rate is 40MSPS
- +2.5V CMOS monolithic construction
- ±0.75LSB differential linearity (typical)
- ±1.0LSB integral linearity (typical)
- External or internal voltage reference (Including Band Gap Reference Block)
- Hexa Channel DAC
- 10-Bit parallel Straight Binary Digital input per channel
- DAC auto-load detection circuitry
- Temperature: 0 ~ 70°C
- Each channel Power_Down

TYPICAL APPLICATIONS

- High Definition Television(HDTV)
- High Resolution Color Graphics
- Hard Disk Driver (HDD)
- CAE/CAD/CAM
- Image Processing
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM



Ver 1.3 (Aug. 2000)

PIN CONFIGURATION

Name	I/O Type	I/O Pad	Pin Description
PDAC[5:0]	DI	piar50_abb	Individual DAC power down control. When activated (high), the corresponding DAC is disabled.
CLK	DI	picc_abb	DAC master clock. Input data is sampled with the rising edge of CLK.
PRE	DI	piar50_abb	Control strobe for the DAC auto-load detection comparator. When PRE transitions high-to-low, the auto-load detect circuit evaluates its selected input. Appropriate settling time must be allowed before the comparator output (DTOUT) is used. When not used, PRE should be left high.
D1[9:0] D2[9:0] D3[9:0] D4[9:0] D5[9:0] D6[9:0]	DI	picc_abb	10-bit straight binary digital input for each DAC channel.
ALLPD	DI	piar50_abb	Power down control for Bandgap and all six DACs. A high level disables all six DACs plus the bandgap reference regardless of the states of PDAC0-5
DTOUT	DO	pot8_abb	Comparator output for detection of resistive load at DAC output. A low at the detect output indicates that the output voltage of the selected channel is above 0.53V and therefore that no load is attached.
CCOMP	AB	poa_bb	Internal DAC compensation node. Connect external 0.1uF cap to VDD25AA1.
IRSET	AB	poa_bb	External resistor from this node to VSS25AA1 defines the full scale output current for the DACs.
VBIAS	AB	poa_bb	External reference voltage output.

I/O TYPE ABBR.

— AI: Analog Input
— DI: Digital Input
— AO: Analog Output
— DO: Digital Output
— AB: Analog Bidirectional
— DB: Digital Bidirectional
— AP: Analog Power
— DP: Digital Power
— AG: Analog Ground
— DG: Digital Ground

Name	I/O Type	I/O Pad	Pin Description
VDD25AA1	AP	vdd2t_bb	Analog Power (needs 3 pads)
VSS25AA1	AG	vss2t_abb	Analog Ground (needs 3 pads)
VDD25AD1	DP	vdd2t_abb	Digital Power
VSS25AD1	DG	vss2t_abb	Digital Ground
VABB	AG	vbb_abb	Substrate Bias(the same with ground level)
IO1	AO	poa_bb	1st Analog Current Output
IO2	AO	poa_bb	2nd Analog Current Output
IO3	AO	poa_bb	3rd Analog Current Output
IO4	AO	poa_bb	4th Analog Current Output
IO5	AO	poa_bb	5th Analog Current Output
IO6	AO	poa_bb	6th Analog Current Output

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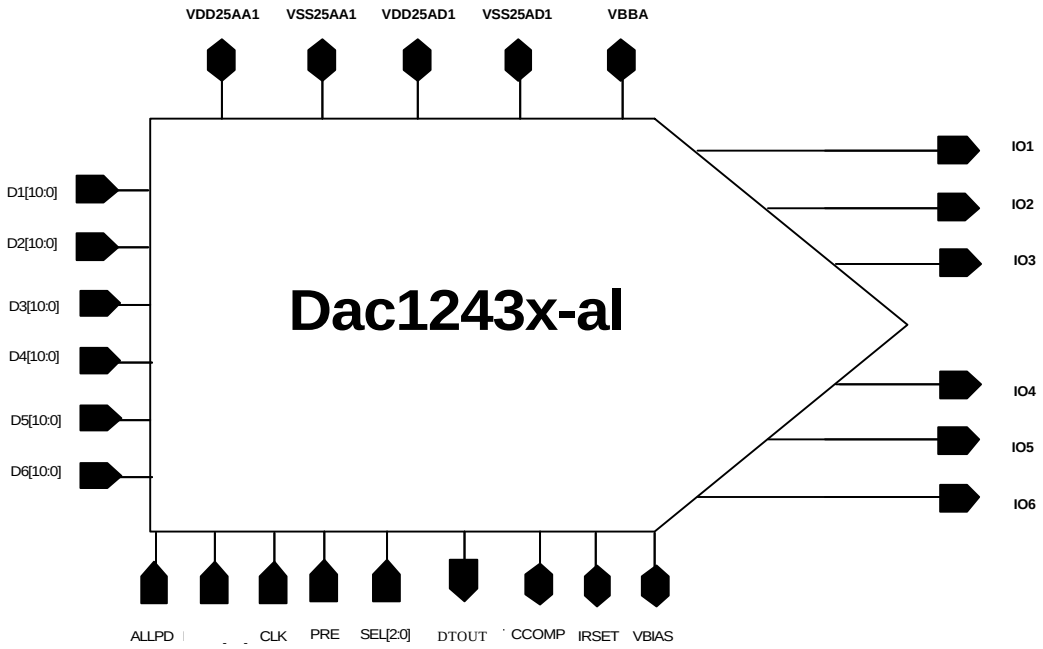
CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	VDD25AA1 - VSS25AA1 VDD25AD1 - VSS25AD1	2.5	V
Voltage on Any Digital Pin	CLK	VSS25AD1-0.25 to VDD25AD1+0.25	V
Storage Temperature Range	T_{stg}	-45 ~ 125	°C

NOTES:

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to GND unless otherwise specified
3. Applied voltage must be limited to specified range.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage	VDD25AD1,VDD25AA1	2.25	2.5	2.75	V
Digital Input Voltage High	V_{IH}	1.75	2.5	-	V
Digital Input Voltage Low	V_{IL}	-	0.0	0.75	V
Operating Temperature Range	Topr	0	25	70	°C
Output Load(effective)	R_L	-	37.5	-	Ω
Reference Load(effective) Resistor	Rset	-	658	-	Ω
Reference Voltage	V_{BIAS}	-	0.7	-	V
Data Input Setup Time	T_S	4	-	-	ns
Data Input Hold Time	T_H	1	-	-	ns
Clock Cycle Time	T_{CLK}	25	-	-	ns
Clock Pulse Width High	T_{PWH}	12	-	-	ns
Clock Pulse Width Low	T_{PWL}	12	-	-	ns
Zero_level Voltage	V_{OZ}	-10	-5	+10	mV
IRSET Current	I_{REF}	0.9	1.06	1.1	mA

NOTE: It is strongly recommended that all the supply pins (VDD25AA1,VDD25AD2) be powered from the same source and all the ground pins(VSS25AA1,VSS25AD1,VABB) avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Resolution	-	-	-	10	Bits
Full Scale Current per Channel	Ifs	-	34	-	mA
Differential Linearity Error	DLE	-	±0.75	±1.0	LSB
Integral Linearity Error	ILE	-	±1.0	±2.0	LSB
Monotonicity	-	Guaranteed			-
Output Compliance	VOC	0	-	+1.3	V
Power Dissipation	PDISS	-	600	700	mW

NOTES:

1. Converter Specifications (unless otherwise specified) : VDD25AA1=VDD25AD1=2.5V VSS25AA1=VSS25AD1=GND, Ta=25°C, Rset=658Ω, R_{LOAD1}=R_{LOAD2}=R_{LOAD3}==R_{LOAD4}=R_{LOAD5}=R_{LOAD6}=37.5Ω, CCCOMP=0.1μF
2. TBD: To Be Determined

AC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Analog DAC output capacitance	C_{IN}	0	10	20	pF
Minimum delay from SEL[2:0] transition to PRE transition low	T_{selL}	100	-	-	ns
Minimum delay from PRE transition low to valid DTOUT output	T_{DET_VAL}	100	-	-	ns
Minimum Pulse width low for PRE	T_{SPWL}	200	-	-	ns
Mismatching	mm	-	11	-	LSB
Power Supply Rejection Ratio(5.8KHz)	PSRR	35	45	-	dB
Conversion Rate	F_{CON}	-	30	40	MHz
Analog Output Delay	Td	-	10	-	ns
Analog Output Rise Time	Tr	-	5	-	ns
Analog Output Fall Time	Tf	-	5	-	ns
Analog Output Settling Time	Tset	-	60	-	ns
Clock & Data Feedthrough	FDTHR	25	30	-	dB
Glitch Impulse	GI	-	±100	±200	pv×sec
Pipeline Delay	Top	0.5	0.7	1.0	CLK
Supply Current	Is	190	210	230	mA

NOTES:

1. The above parameters are not tested through the temperature range, but these are guaranteed over the full temperature range.
2. Clock & data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs.
3. Settling time does not include clock and data feedthrough . Glitch impulse include clock and data feedthrough.

This is hexa 10bit 40MSPS digital to analog data converter and uses current-segment architecture for 6bits of MSB sides and binary-weighted architecture for 6bits of LSB side. It contains of 1st latch block, decoder block,2nd latch block, OPA block, CM(current mirror)block ,BGR(Band Gap Reference) block, Auto-load detect block and analog switch block, etc.

This core uses reference current which decide the 1LSB current by dividing the reference current by 32times. So the reference current must be constant and it can be constant by using OPA block with high DC gain. The most significant block of this core is analog switch block and it must maintain the uniformity at each switch, so layout designer must care of it. And more than 90% of supply current is dissipated at analog switch block. And it uses samsung standard cell as all digital cell of latch, decoder and buffer, etc. And to adjust full current output range, you must decide the Rset value(connected to IRSET pin) and. Its voltage output can be obtained by connecting RL1(connected to IO1 pin) and RL2(connected to IO2 pin) ,RL3(connected to IO3 pin) and RL4(connected to IO4 pin), RL5(connected to IO5 pin and RL6(connected to IO6 pin).

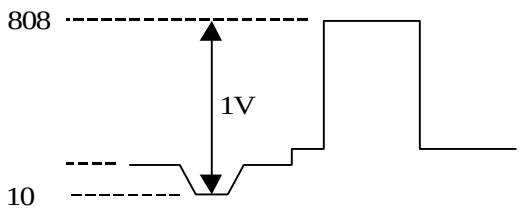
Its maximum output voltage limit is Compliance voltage. So you must decide the RL[6:1], Vbias and Rset carefully not to exceed the output voltage limit. It contains PDAC[5:0] pins for power-save of each channel and ALLPD for power-down mode of all blocks.

Even though one or two out of 6 channels enter power-save mode, the reference block(OPA block, CM block, BGR block) is still alive, but if ALLPD is activated(high), then all blocks of this core is disable regardless of PDAC[5:0], so at this case supply current is almost just about the sum of leakage. You cant check the BGR's output voltage by checking the VBIAS pin.

user can detect the presence of an expected load on each DAC output by configuring the DAC digital inputs such that the detection comparator threshold(0.53V) is a useful threshold for presence of load resistance. Set SEL[3:0] to select the appropriate DAC output. Transition PRE to low, wait for settling DTOUT value and return PRE back to high.

The IRSET pin creates a +0.7VDC reference that can be forced with an external reference voltage ap pin VBIAS. This voltage when combined with the external resistor attached to the IRSET pin sets the output current range for all six DACs. The following example shows how to create a 1Vpk-pk output for a 100 IRE NTSC signal. Any other required variations can easily be calculated from the supplied equations. Please remember that these are ideal equations, the mismatch tolerances from the data sheet should be taken into account for any calculations.

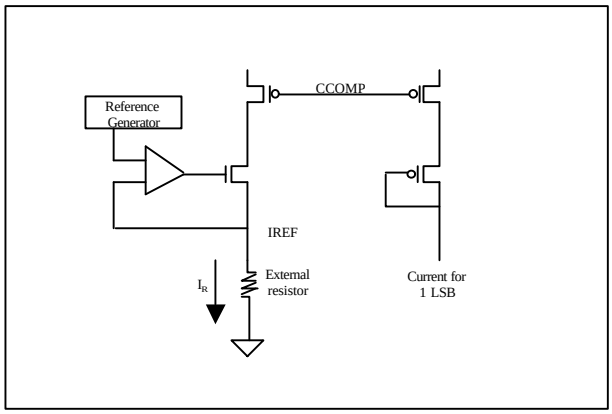
The <figure 1> diagram shows a typical relationship between DAC input and voltage output.



An example 10-bit DAC relationship
input code verse output level

< Figure 1 >

This <figure 2> diagram shows the basic bias-generator and analog current switch. From this diagram the number of DAC codes for a 1V delta output is: C100 = 808 - 10 = 798



< Figure 2 >

a standard doubly terminated 75 Ohm line is assumed :

$$I100 = \frac{V_{100}}{RLOAD} = \frac{1}{37.5} = 26.666mA$$

The relationship between the IR reference current and DAC output current is shown below.

IR = 32 LSB

From the previous equation we have:

$$RSET = \frac{IRSET}{IR} = \frac{0.7V}{1.069mA} = 654W$$

Summation of all equations gives:

$$RSET = \frac{IRSET \times C100 \times RLOAD}{32 \times V100}$$

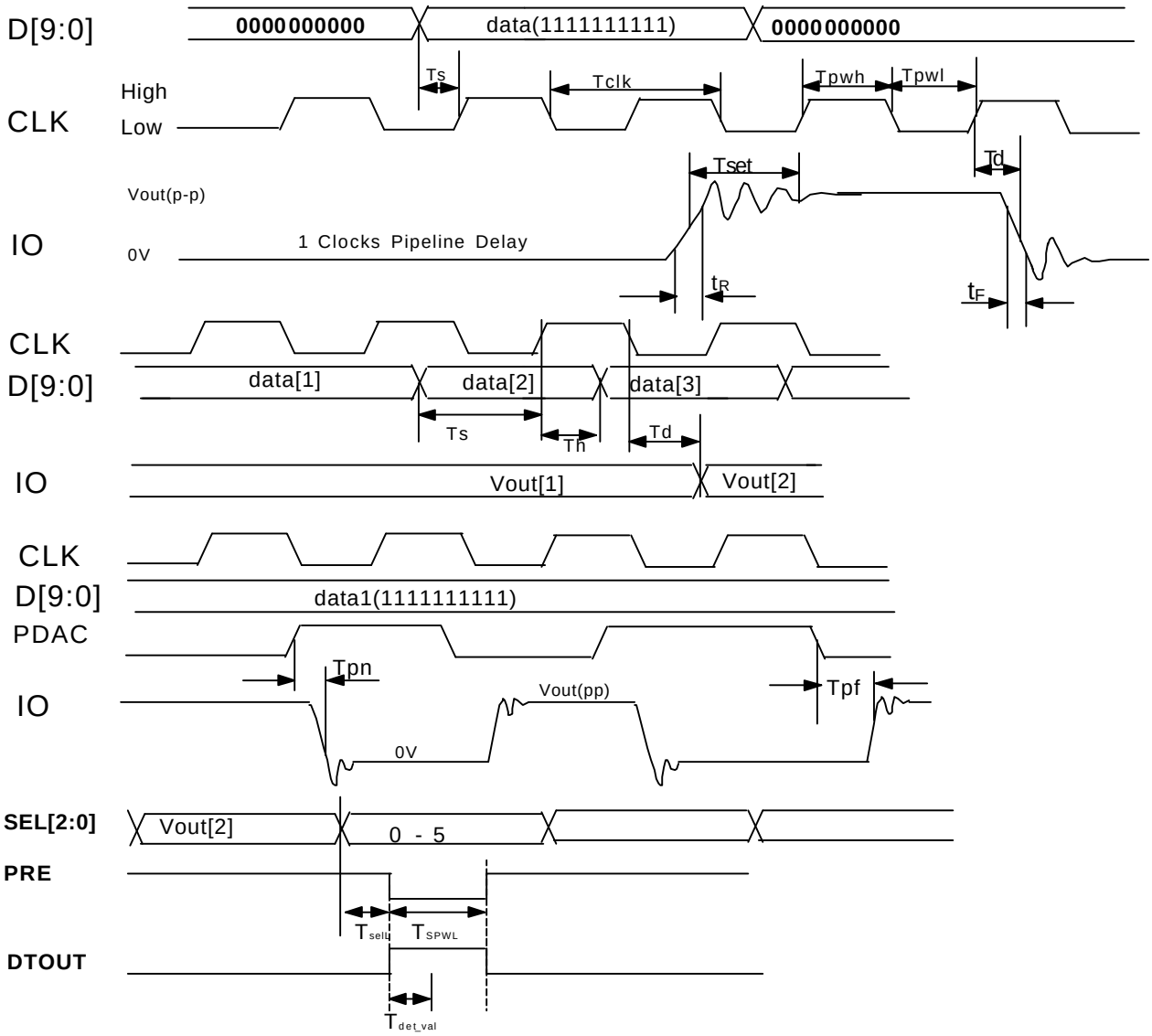
For most video applications an external resistor of 649Ω(+/- 1%) would be selected when driving doubly terminated loads (37.5Ω), and an external resistor of 1.3KΩ (+/- 1%) would be selected when driving loads of 75Ω, in order to have 798 DAC codes correspond to a 1V delta output voltage swing. Then the DAC output levels and the associated codes are as shown below.

Table 1:Summary of DAC Voltage and Codes

Signal Level	CVBS/LUMA DAC Code	IRE Value	DAC Voltage
Max output	1023	137.2	1.282V
100% White	810	100	1.015V
Black	282	7.37	353mV
Sync	12	-40	15mV
White - Black	570	100	714mV delta
White - Wync	798	140	1V delta
Color burst	228	40	285mV delta

DAC voltages assume the standard 140 IRE = 1V. Numbers shown are for NTSC type video with a pedestal.

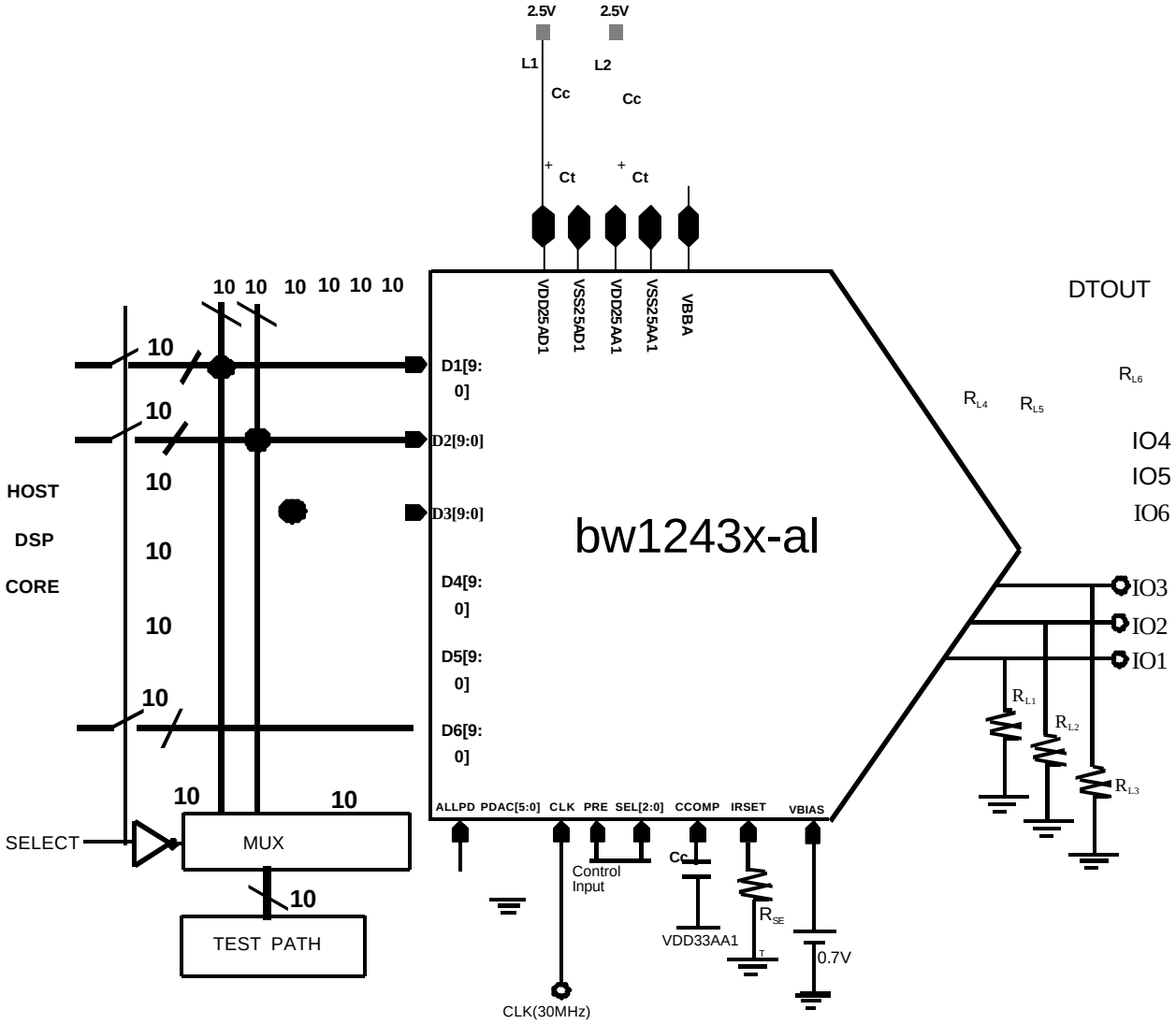
TIMING DIAGRAM



NOTES:

1. The Behavioral Modeling is provided by Verilog
2. Output delay(Td) measured from the 50% point of the rising edge of CLK to the full scale transition.
3. Settling time(Tset) measured from the 50% point of full scale transition to the output remaining within ±1LSB iteration.
4. Output rising(Tr)/falling(Tf) time measured between the 10% and 90% points of full scale transition.
5. Any power_down doesn't need clock signal.
6. PD1(PD2,PD3, ¼,PD6) makes the 1st(2nd,3rd, ¼,6th) channel down respectively when it is high.
7. PD1,PD2,PD3,PD4,PD5 and PD6 have absolutely no relations among them.
8. ALLPD makes all of the blocks disable regardless of PDAC[5:0].
9. The minimum Pulse Width Low of ALLPD should be longer than 1ms.
10. The minimum Pulse Width Low of PDAC<5:0> should be longer than 50ns.
11. The minimum Pulse Width Low of ALLPD and PDAC<5:0> should be longer than 20ns.

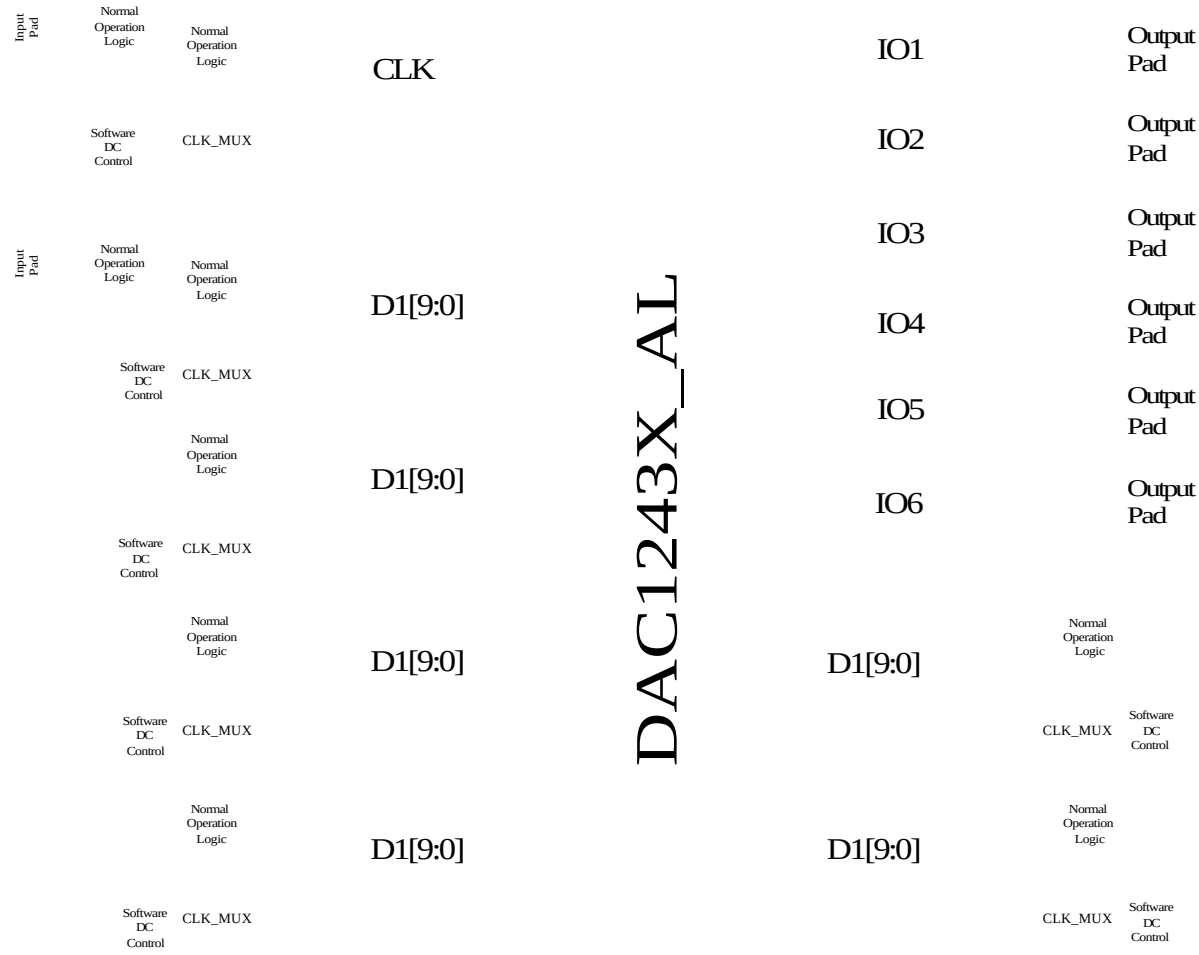
CORE EVALUATION GUIDE



- You must use more than two PADs for VDD33AA11 'cause it's current is more than about 81mA.

Location	Description
Cc	0.1µF
Ct	10µF
R_{SET}	658Ω
R_{L1}, R_{L4}	37.5Ω
R_{L2}, R_{L5}	37.5Ω
R_{L3}, R_{L6}	37.5Ω
V_{BIAS}	0.7V

CORE EVALUATION GUIDE



You must use more than two PADs for VDD33AA11 'cause it's current is more than about 81mA.

Location	Description
Cc	0.1μF
Ct	10μF
R_{SET}	658Ω
R_{L1}	37.5Ω
R_{L2}	37.5Ω
R_{L3}	37.5Ω
V_{BIAS}	0.7V

1. ABOUT TESTABILITY
   If you want to test it over full spec via all channel in main chip(that is, when it is used as a block of main chip) you must add many pins(for 60pins of digital inputs, 6pins of analog outputs, etc) at the main chip to test this DAC block. But usually it is nearly impossible 'cause the total number of pins at main chip is limited. So more efficient method for testing this DAC block is needed. We offer two ways of testing efficiently here as a reference.
   But remember this is not the best thing. You can test it by your own testing method.
2. FIRST METHOD OF TESTABILITY
   The first way is adding only extra 10PADs for 10bit parallel digital inputs and 3PADs for channel selecting and path selecting. You can check six channels one by one, that is you can test only one channel at one time. Therefore you can test all three channels by turn but cannot check all channel at one time. And this method needs extra MUX and switch blocks for testing.

   Furthermore we can assure all channels by testing only one channel because all the six channels have same architecture and share the same analog reference
   block(OPAMP, CM, BGR). This characteristic makes it simple to test this DAC block(when it is embedded in main chip) by adding another 10PADs for parallel digital inputs and 3PADs for selecting one channel analog switch block of DAC out of three channels.
3. SECOND METHOD OF TESTABILITY
   If above extra 13PADs are burden on you, then you can test it by this second method to reduce the extra PADs for testing. What is different from above method is that this way needs only 2 extra PADs (one for 1bit serial digital input and the other for clock signal), but you must insert extra serial to parallel converter block for converting 1bit 10times high speed digital input to 10bit parallel digital inputs. And this block may need considerable area. And this method also needs extra 3PADs for channel selecting and path selecting.
4. ANALYSIS
   The voltage applied to VBIAS is measured at IRSET node . And the voltage value is proportioned to the reference current value of resistor which is connected to IRSET node. So you can estimate the full scale current value by measuring the voltage, and check the DC characteristics of the OPAMP. For reference, as VBIAS voltage applied to VBIAS pin is given at IRSET node, the current flowing through RSET resistor (connected to IRSET pin) is given as VREF/RSET.

   If the voltage applied to VBIAS pin is not same with IRSET node, you can say "This DAC chip does not work properly", because the internal OPAMP block makes the two node voltage(IFEF pin, VBIAS pin) equal. And you have to check the COMP node to see the desired voltage on it. If the desired voltage is not measured, you can check the DAC output by applying a desired voltage to the COMP pin instead of compensation capacitor directly.
   If you use internal reference voltage(BGR's output voltage) instead of external Vbias by setting the BGRSW low, you can check the BGR's output by checking the VBIAS pin voltage.

PC BOARD LAYOUT CONSIDERATIONS

- **PC Board Considerations**

To minimize noise on the power lines and the ground lines, the digital inputs need to be shielded and decoupled. This trace length between groups of vdd (VDD33AA1,VDD33AD1) pins short as possible so as to minimize inductive ringing.

- **Supply Decoupling and Planes**

For the decoupling capacitor between the power line and the ground line, 0.1mF ceramic capacitor is used in parallel with a 10mF tantalum capacitor. The digital power plane(VDD33AD1) and analog power plane (VDD33AA1) are connected through a ferrite bead, and also the digital ground plane(VSS33AD1) and the analog ground plane(VSS33AA1). This ferrite bead should be located within 3inches of the DAC1243x-AL. The analog power plane supplies power to the DAC1243X-AL of the analog output pin and related devices.

- **Analog Signal Interconnect**

To minimized noise pickup and reflections due to impedance mismatch, the DAC1243X-AL should be located as close as possible to the output connector.

The line between DAC output and monitor input should also be regarded as a transmission line. Due to the fact, it can cause problems in transmission line mismatch. As a solution to these problems, the double-termination methods used.

By using this, both ends of the termination lines are matched, providing an ideal, non-reflective system.

CORE LAYOUT GUIDE (OPTIONAL)

Layout DAC core replacement

- It is recommended that you use thick analog power metal. when connecting to PAD, the path should be kept as short as possible, and use branch metal to connect to the center of analog switch block.
- It is recommended that you use thick analog output metal (at least more than 25mm) when connecting to PAD, and also the path length should be kept as short as possible.
- Digital power and analog power are separately used.
- When it is connected to other blocks, it must be double shielded using N-well and P+ active to remove the substrate and coupling noise. In that case, the power metal should be connected to PAD directly.
- Bulk power is used to reduce the influence of substrate noise.
- You must use more than two pins for VDD33AA11 because it require much current dissipation(about 93mA)
- It is recommended that analog metal line(including IRSET,VBIAS,IO[1:3],IOB[1:3]) and analog power metal line should be layouted alone and should not mixed with other noisy digital metal lines.
- If this core is used as a function block in larger main chip, you can join digital power metal of this core with the main digital power instead of using new digital power pad for this core. But you must use new analog power pad for the analog power of this core.

FEEDBACK REQUEST

We appreciate your interest in out products. If you have further questions, please specify in the attached form. Thank you very much.

DC / AC Electrical Characteristic

Characteristics	Min	Typ	Max	Unit	Remarks
Supply Voltage				V	
Power dissipation				mW	
Resolution				Bits	
Analog Output Voltage				V	
Operating Temperature				°C	
Output Load Capacitor				mF	
Output Load Resistor				Ω	
Integral Non-Linearity Error				LSB	
Differential Non-Linearity Error				LSB	
Maximum Conversion Rate				MHz	
Voltage Output DAC					
Reference Voltage TOP BOTTOM				V	
Analog Output Voltage Range				V	
Digital Input Format		Binary Code or 2's Complement Code			
Current Output DAC					
Analog Output Maximum Current				mA	
Analog Output Maximum Signal Frequency				MHz	
Reference Voltage				V	
External Resistor for Current Setting(RSET)				Ω	
Pipeline Delay				sec	

— Do you want to Internal Reference Voltage(BGR)?
— Which do you want to Serial Input TYPE or parallel Input TYPE?
— Do you need 3.3v and 5v power supply in your system?
— How many channels do you need(BW1221L is dual channel DAC)?

HISTORY CARD

Version	Date	Modified Items	Comments
Ver 1.0		Newly registered by circuit designer Koo Hyung-Woan	
Ver 1.3	00.08.05	Port Name change (PDAC[6:1]->PDAC[5:0]), Add history card	