GENERAL DESCRIPTION

This core is a CMOS quad-channel 10bit 75MSPS D/A converter for general & video applications. The dac1350x core is implemented in the Samsung 0.18um 3.3V CMOS process. Digital inputs are coded as straight binary. Each dac channel includes dependent power down control and the ability to sense output load. An external(optional) or internal 0.7V reference voltage (VREFOUT) and a single external resister define the full-scale output current together. It uses the two architecture of current-segment and binary-weighted.

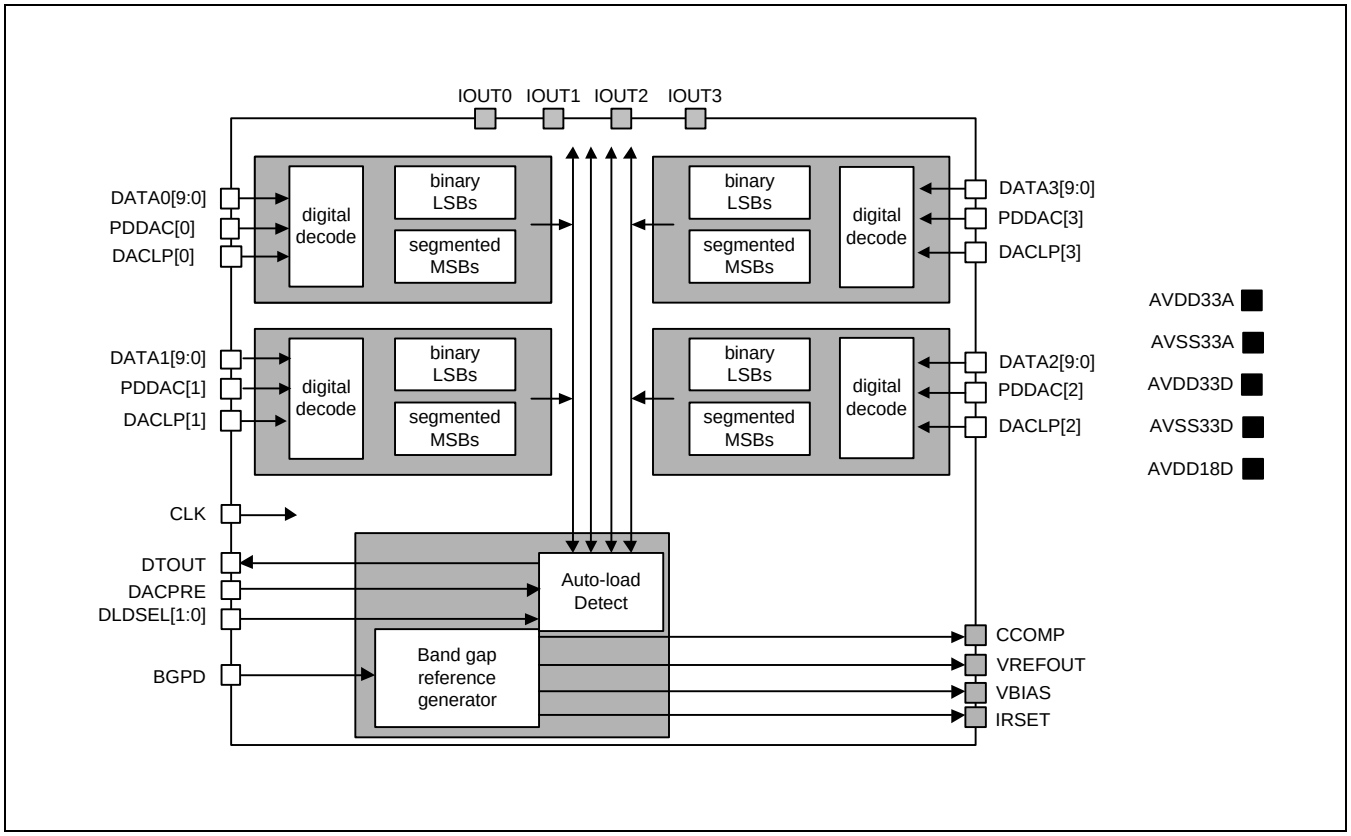
FEATURES

— Maximum conversion rate is 75MSPS
— +3.3V CMOS monolithic construction
— ±1 LSB differential linearity (max)
— ±2 LSB integral linearity (max)
— External or internal voltage reference (Including Band Gap Reference Block)
— 10-Bit parallel digital input
— DAC auto-load detection circuitry
— Temperature : 0 ~ 70°C
— Each channel Power_Down
— Power Dump Mode

TYPICAL APPLICATION

— High Definition Television(HDTV)
— High Resolution Color Graphics
— Image Processing

FUNCTIONAL BLOCK DIAGRAM



Ver 1.8 (May. 2002)

CORE PIN DESCRIPTION

Pin Name	I/O Type	I/O Pad	Pin Description
INPUTS			
PDDAC[3:0]	DI	picc_abb	Individual DAC power down control. When activated(high), the corresponding DAC is disabled.
DACLP[3:0]	DI	picc_abb	Low power current dumping mode control for each DAC. When selected (high enables low power mode) the corresponding DAC will run at reduced power with a slight loss in performance.
CLK	DI	picc_abb	DAC master clock. Input data is sampled with the rising edge of **CLK**.
DACPRE	DI	picc_abb	Control strobe for the DAC auto-load detection comparator. When **DACPRE** transitions high-to-low, the auto-load detect circuit evaluates its selected input. Appropriate settling time must be allowed before the comparator output **(DTOUT)** is used. When not used, **DACPRE** should be left high.
DATA0[9:0] DATA1[9:0] DATA2[9:0] DATA3[9:0]	DI	picc_abb	10-bit straight binary digital input for each DAC channel.
BGPD	DI	picc_abb	Power down control for Bandgap and all quad DACs. A high level disables all quad DACs plus the bandgap reference regardless of the states of **PDDAC0,PDDAC1,PDDAC2,PDDAC3**
DLDSEL[1:0]	DI	picc_abb	Selection control for external DAC auto-load detection. Enable of load for IOUT0 is selected LDSEL[1:0]="00", IOUT2 is DLDSEL[1:0]="01", IOUT1 is DLDSEL[1:0]="10", IOUT3 is DLDSEL[1:0]="11"
OUTPUT			
DTOUT	DO	pot8_abb	Comparator output for detection of resistive load at DAC output. A low at the detect output indicates that the output voltage of the selected channel is above 0.53V and therefore that no load is attached.
IOUT0 IOUT1 IOUT2 IOUT3	AO	phoa_abb	Analog Current Output for each of the four DACs
REFERENCES			
CCOMP	AB	phoa_abb	Connect external 0.1uF cap to **AVDD33A**.
IRSET	AB	phoa_abb	External resistor from this node to **AVSS33A** defines the full scale output current for the DACs.
VBIAS	AB	phoa_abb	Connect external 0.1uF cap and 100ohm resistor to **AVDD33A**.
VREFOUT	AB	phoa_abb	internal / external voltage reference output

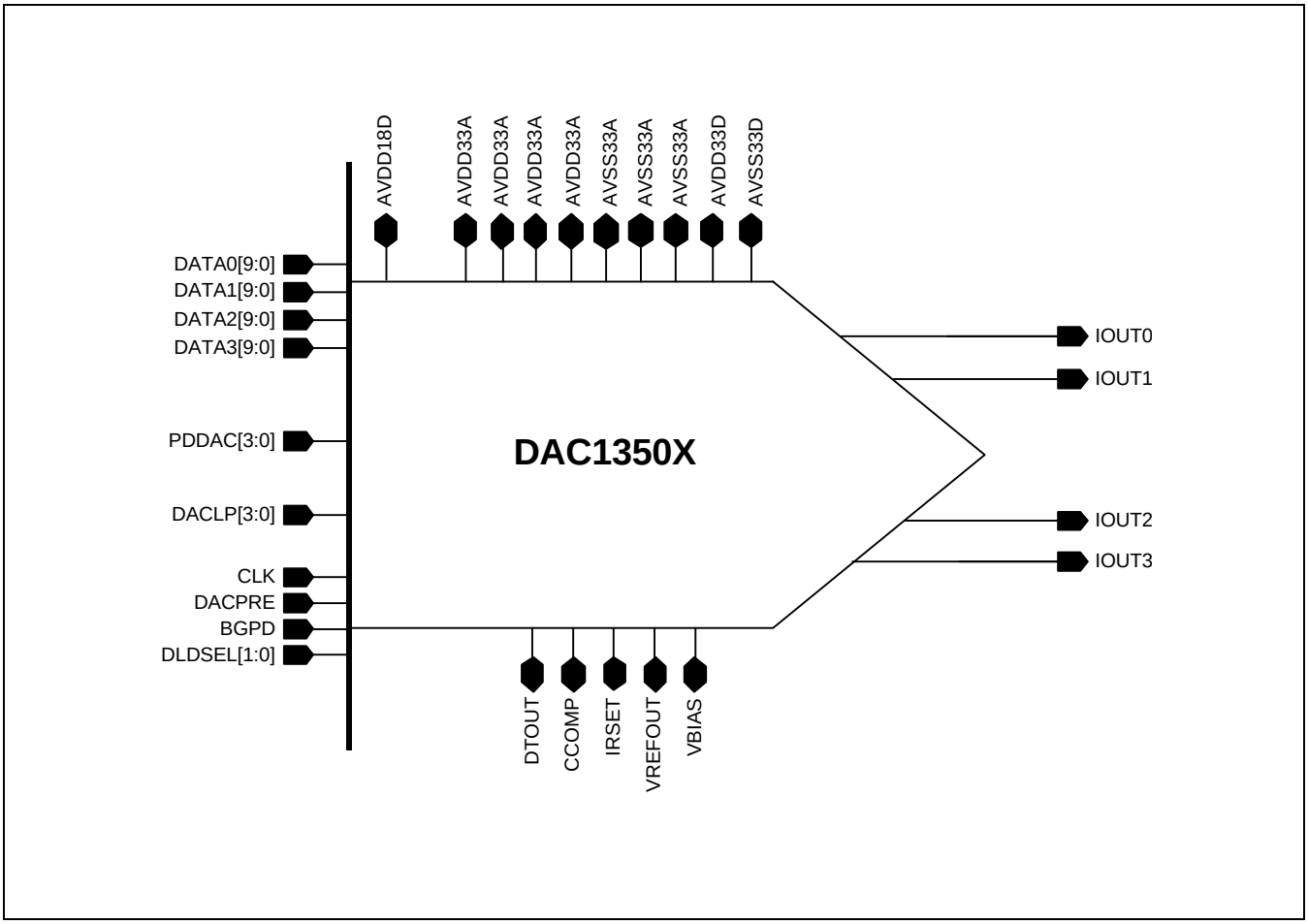
CORE PIN DESCRIPTION (Continued)

Pin Name	I/O Type	I/O Pad	Pin Description
POWER			
AVDD33A	AP	vdd3t_abb	Analog Power (NEEDS 3 PIN)
AVSS33A	AG	vss3t_abb	Analog Ground (NEEDS 3 PIN)
AVDD33D	DP	vdd3t_abb	Digital Power
AVSS33D	DG	vss3t_abb	Digital Ground
AVDD18D	DP	–	Digital interface Power

I/O Type Abbr.

— AI: Analog Input
— DI: Digital Input
— AO: Analog Output
— DO: Digital Output
— AB: Analog Bi-direction
— DB: Digital Bi-direction
— AP: Analog Power
— AG: Analog Ground
— DP: Digital Power
— DG: Digital Ground

CORE CONFIGURATION



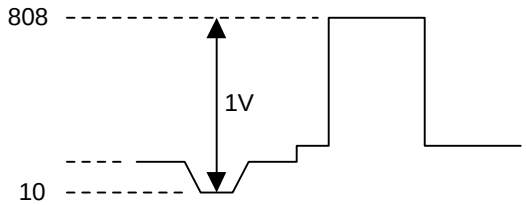
FUNCTIONAL DESCRIPTION

This is quad 10bit 75MSPS digital to analog data converter and uses current-segment architecture for 4-bits in MSB sides and binary-weighted architecture for 6-bits in LSB sides. It contains of 1'st latch block, decoder block , 2'nd latch block , OPA block , CM (current mirror) block , BGR (Band Gap Reference) block, Auto-load detect block and analog switch block, etc. This core uses reference current which decide the 1LSB current by dividing the reference current by 32times. So the reference current must be constant and it can be constant by using OPA block with high DC gain. The most significant block of this core is analog switch block and it must maintain the uniformity at each switch, so layout designer must care of it. And more than 90% of supply current is dissipated at analog output side. And it uses samsung standard cell as all digital cell of latch, decoder and buffer, etc. And to adjust full current output range, you must decide the Rset value(connected to IRSET pin) and. Its voltage output can be obtained by connecting RL1(connected to IOUT0 pin) and RL2(connected to IOUT1 pin) ,RL3(connected to IOUT2 pin) and RL4(connected to IOUT3 pin) Its maximum output voltage limit is Compliance voltage. So you must decide the RL[4:1], VREFOUT and Rset carefully not to exceed the output voltage limit. It contains PDDAC[3:0] pins for power-save of each channel and BGPD for power-down mode of all blocks. Even though one or two out of 4 channels enter power-save mode, the reference block(OPA block,CM block, BGR block) is still alive, but if BGPD is activated(high), then all blocks of this core is disable regardless of PDDAC[3:0], so at this case supply current is almost just about the sum of leakage. You cant check the BGR's output voltage by checking the VREFOUT pin.

The user can detect the presence of an expected load on each DAC output by configuring the DAC digital inputs such that the detection comparator threshold(0.53V) is a useful threshold for presence of load resistance. Set DLDSEL[1:0] to select the appropriate DAC output. Transition PRE to low, wait for settling DTOUT value and return PRE back to high.

The IRSET pin creates a +0.7[V] DC reference that can be forced with an external reference voltage pin VREFOUT. This voltage when combined with the external resistor attached to the IRSET pin sets the output current range for all quad DACs. The following example shows how to create a 1Vpk-pk output for a 100 IRE NTSC signal. Any other required variations can easily be calculated from the supplied equations. Please remember that these are ideal equations, the mismatch tolerances from the data sheet should be taken into account for any calculations.

The <Figure 1> diagram shows a typical relationship between DAC input and voltage output.



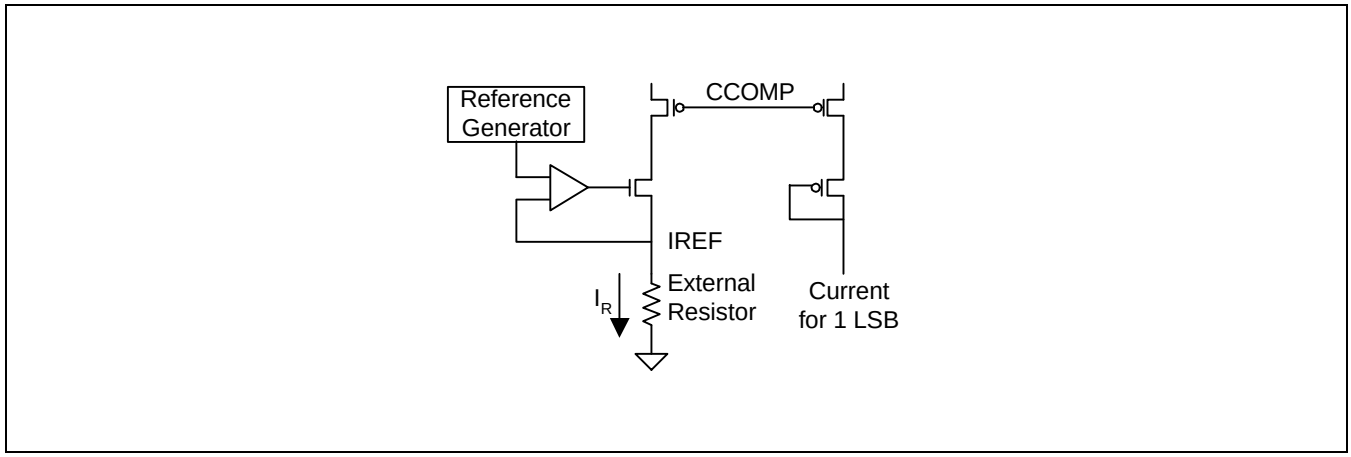
An example 10-bit DAC relationship
input code verse output level

<Figure 1>

<Figure 2> diagram shows the basic bias-generator and analog current switch.

From this diagram the number of DAC codes for a 1V delta output is :

C100 = 808 - 10 = 798



<Figure 2>

If a standard doubly terminated 75 Ohm line is assumed :

$$I_{100} = \frac{V_{100}}{R_{LODA}} = \frac{1}{37.5} = 26.666mA$$

The relationship between the IR reference current and DAC output current is shown below.

IR = 32 LSB

From the previous equation we have:

$$R_{SET} = \frac{IRSET}{I_R} = \frac{0.7V}{1.069mA} = 654\Omega$$

Summation of all equations gives :

$$R_{SET} = \frac{IRSET * C_{100} * R_{LODA}}{32 * V_{100}}$$

For most video applications an external resistor of 649Ω(+/- 1%) would be selected when driving doubly terminated loads (37.5Ω), and an external resistor of 1.3KΩ (+/- 1%) would be selected when driving loads of 75Ω, in order to have 798 DAC codes correspond to a 1V delta output voltage swing. Then the DAC output levels and the associated codes are as shown below.

Table 1. Summary of DAC Voltage and Codes

Signal Level	CVBS/LUMA DAC Code	IRE Value	DAC Voltage
Max output	1023	137.2	1.282V
100% White	810	100	1.015V
Black	282	7.37	353mV
Sync	12	-40	15mV
White - Black	570	100	714mV delta
White - Sync	798	140	1V delta
Color burst	228	40	285mV delta

NOTE: DAC voltages assume the standard 140 IRE = 1V. Numbers shown are for NTSC type video with a pedestal.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Values	Unit
Supply Voltage	AVDD33A - AVSS33A AVDD33D - AVSS33D	-0.5 to 4.5	V
Voltage on Any Digital Pin	CLK	AVSS33D - 0.3 to AVDD33D + 0.3	V
Storage Temperature Range	Tstg	-45 to 125	°C

NOTES:

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to GND unless otherwise specified
3. Applied voltage must be limited to specified range.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol(Name)	Min	Typ	Max	Unit
Operating Supply Voltage	AVDD33D,AVDD33A	3.0	3.3	3.6	V
Digital Input Voltage High	V_{IH}	0.7*VDD	2.5	-	V
Digital Input Voltage Low	V_{IL}	-	0.0	0.3*VDD	V
Operating Temperature Range	T_{opr}	0	25	70	°C
Output Load(effective)	R_L	-	37.5	-	Ω
Reference Load(effective) Resistor	Rset	-	570	-	Ω
Internal Reference Voltage	V_{refout}	0.63	0.7	0.77	V
Data Input Setup Time	T_S	4	-	-	ns
Data Input Hold Time	T_H	1	-	-	ns
Zero_level Voltage	V_{OZ}	-5	0	+5	mV
IRSET Current	I_{REF}	1.0	1.22	1.5	mA

NOTE: It is strongly recommended that all the supply pins (AVDD33A,AVDD33D) be powered from the same source and at all the ground pins (AVSS33A, AVSS33D) avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Resolution	-	-	-	10	Bits
Full Scale Current per Channel	Ifs	31.32	34.8	38.26	mA
Differential Linearity Error	DLE	-1.0	+0.4	+1.0	LSB
Integral Linearity Error	ILE	-2.0	+1.5	±2.0	LSB
Monotonicity	-	Guaranteed	-		
Output Compliance	VOC	0	-	+1.4	V
Power Dissipation	PDISS	-	50	100	uA

NOTE: Converter Specifications (unless otherwise specified) : AVDD33A=AVDD33D=3.3V
AVSS33A=AVSS33D=GND, 0°C< Temperature range < 70°C, Rset=570 [ohm],
Rload1=Rload2=Rload3=Rload4 37.5 ohm resistor are connected to analog ground (AVSS33A).
CCOMP=0.1uF capacitor is connected to analog power(AVDD33A).
VBIAS = 0.1uF capacitor in series 100ohm resistor is connected to analog power(AVDD33A).

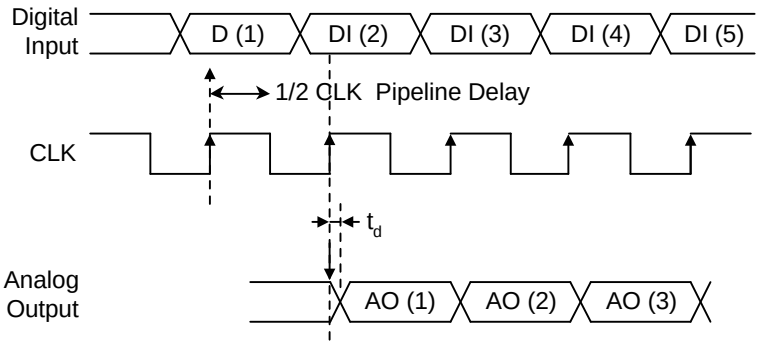
AC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Minimum delay from SEL[1:0] transition to PRE transition low	T_{selL}	100	-	-	ns
Minimum delay from DACPRE transition low to valid DTOUT output	T_{DET_VAL}	100	-	-	ns
Minimum Pulse width low for PRE	T_{SPWL}	200	-	-	ns
DAC to DAC Mismatch	mm	-2.5	-	2.5	%
DAC to DAC Mismatch for any PD case.	mm	-2.5	-	2.5	%
Cross Talk[1]	XTALK	-	-15	-10	dB
Power Supply Rejection Ratio	PSRR	-40	-45	-	dB
Conversion Rate	F_{CON}	75	30	-	MHz
Analog Output Delay	Td	-	10	-	ns
Analog Output Rise Time	Tr	-	1	-	ns
Analog Output Fall Time	Tf	-	1	-	ns
Analog Output Settling Time	Tset	-	33	-	ns
Clock & Data Feed-through	FDTHR	25	30	-	dB
Signal-to-Noise Ratio	SNDR	40	47	-	dB
Total Harmonic Distortion	THD	45	50	-	dB
Glitch Impulse	Gl	-	±100	±200	pv*sec
Pipeline Delay	Top	-	0.5	-	CLK
Supply Current	Is	-	150	200	mA

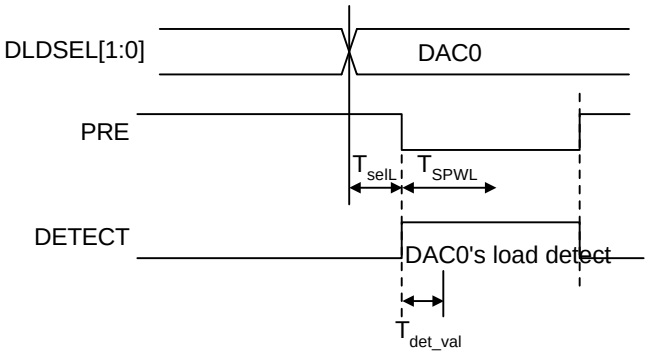
NOTES:
1. The above parameters are not tested through the temperature range, but these are guaranteed over the full temperature range.
2. DAC to DAC Cross-talk is measured by holding one DAC high while the other three are making low to high and high to low transitions.

TIMING DIAGRAM

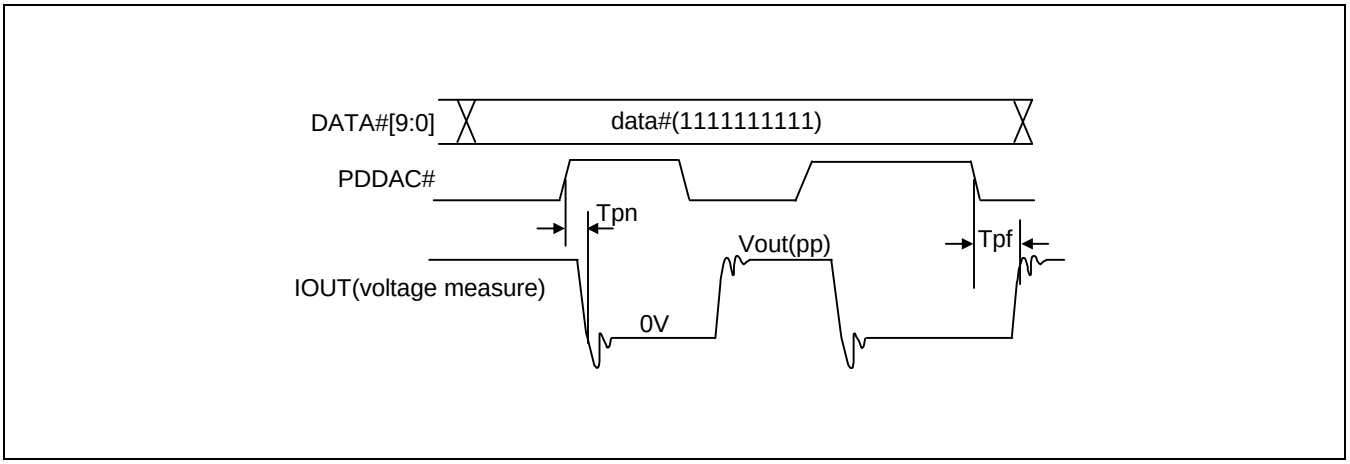
Analog Output Delay



Load Detection Timing



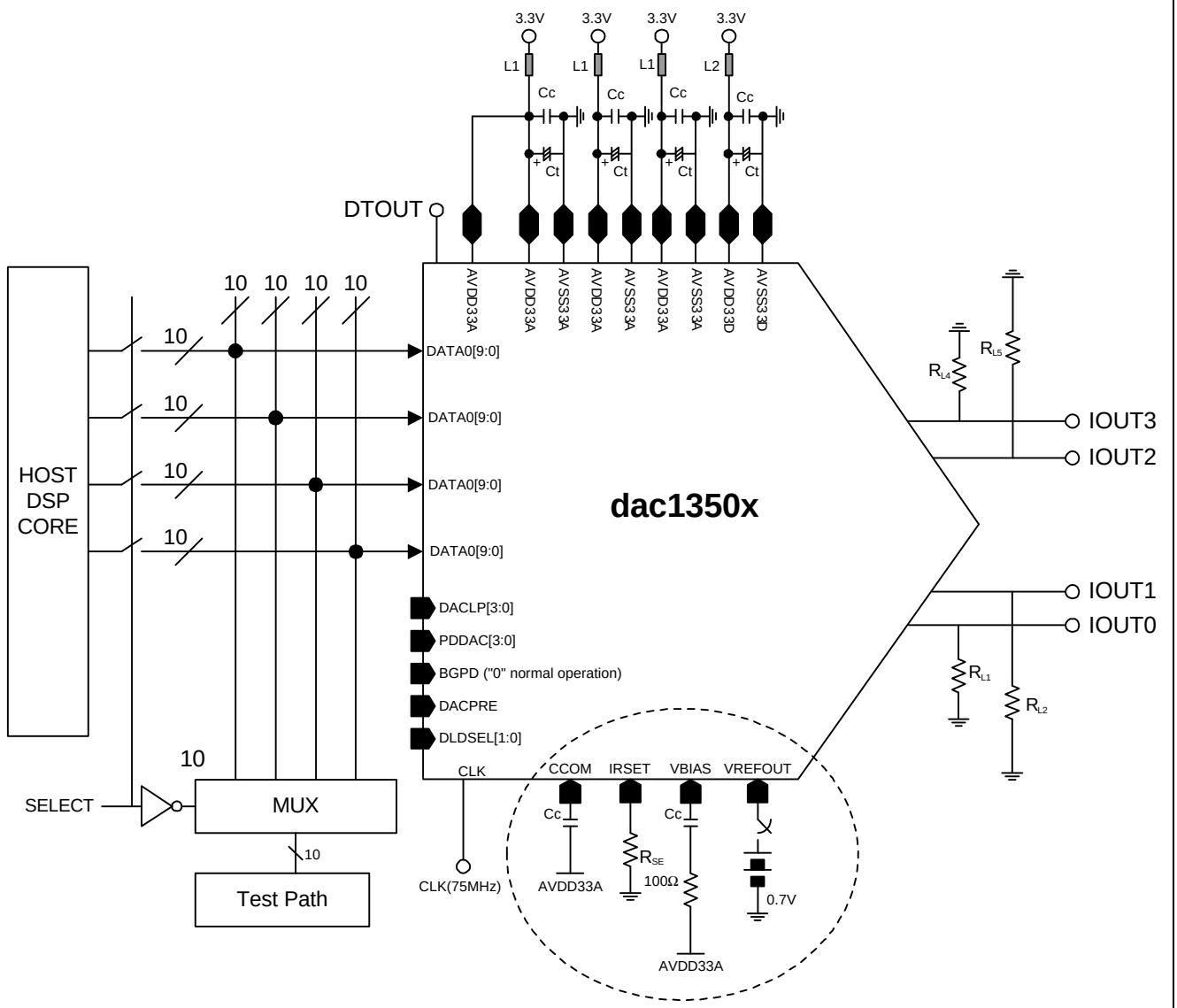
Power Down Timing



NOTES:

1. The Behavioral Modeling is provided by Verilog.
2. Output delay(Td) measured from the 50% point of the rising edge of CLK to the full scale trasition.
3. Settling time(Tset) measured from the 50% point of full scale transition to the output remaining within ±1LSB iteration.
4. Output rising(Tr)/falling(Tf) time measured between the 10% and 90% points of full scale transition.
5. Any power_down doesn't need clock signal.
6. PDDAC# makes the channel down respectively when it is high.
7. PDDAC# have absolutely no relations among them.
8. BGPD makes all of the blocks disable regardless of PDDAC#.
9. The minimum Pulse Width Low of BGPD should be longer than 500us.
10. The minimum Pulse Width Low of PDDAC# should be longer than 50us.
11. The minimum Pulse Width Low of BGPD and PDDAC# should be longer than 20ns.

CORE EVALUATION GUIDE



NOTE: You must use more than two 3PADs for AVDD33A because it's current is more than about 150mA.

Location	Description
Cc	0.1mF
Ct	10mF
R_{SET}	570Ω
$R_{L1}/R_{L2}/R_{L3}/R_{L4}$	37.5Ω

1. ABOUT TESTABILITY

If you want to test it over full specifications via all channel in main chip(that is, when it is used as a block of main chip) you must add many pins(for 60pins of digital inputs, 6pins of analog outputs, etc) at the main chip to test this DAC block. But usually it is nearly impossible 'cause the total number of pins at main chip is limited. So more efficient method for testing this DAC block is needed. We offer two ways of testing efficiently here as a reference. But remember this is not the best thing. You can test it by your own testing method.

2. FIRST METHOD OF TESTABILITY

The first way is adding only extra 10PADs for 10bit parallel digital inputs and 3PADs for channel selecting and path selecting. You can check quad channels one by one, that is you can test only one channel at one time. Therefore you can test all three channels by turn but cannot check all channel at one time. And this method needs extra MUX and switch blocks for testing. Furthermore we can assure all channels by testing only one channel because all the quad channels have same architecture and share the same analog reference block(OPAMP, CM, BGR). This characteristic makes it simple to test this DAC block(when it is embedded in main chip) by adding another 10PADs for parallel digital inputs and 3PADs for selecting one channel analog switch block of DAC out of three channels.

3. SECOND METHOD OF TESTABILITY

If above extra 13PADs are burden on you, then you can test it by this second method to reduce the extra PADs for testing. What is different from above method is that this way needs only 2 extra PADs(one for 1bit serial digital input and the other for clock signal), but you must insert extra serial to parallel converter block for converting 1bit 10times high speed digital input to 10bit parallel digital inputs. And this block may need considerable area. And this method also needs extra 3PADs for channel selecting and path selecting.

4. ANALYSIS

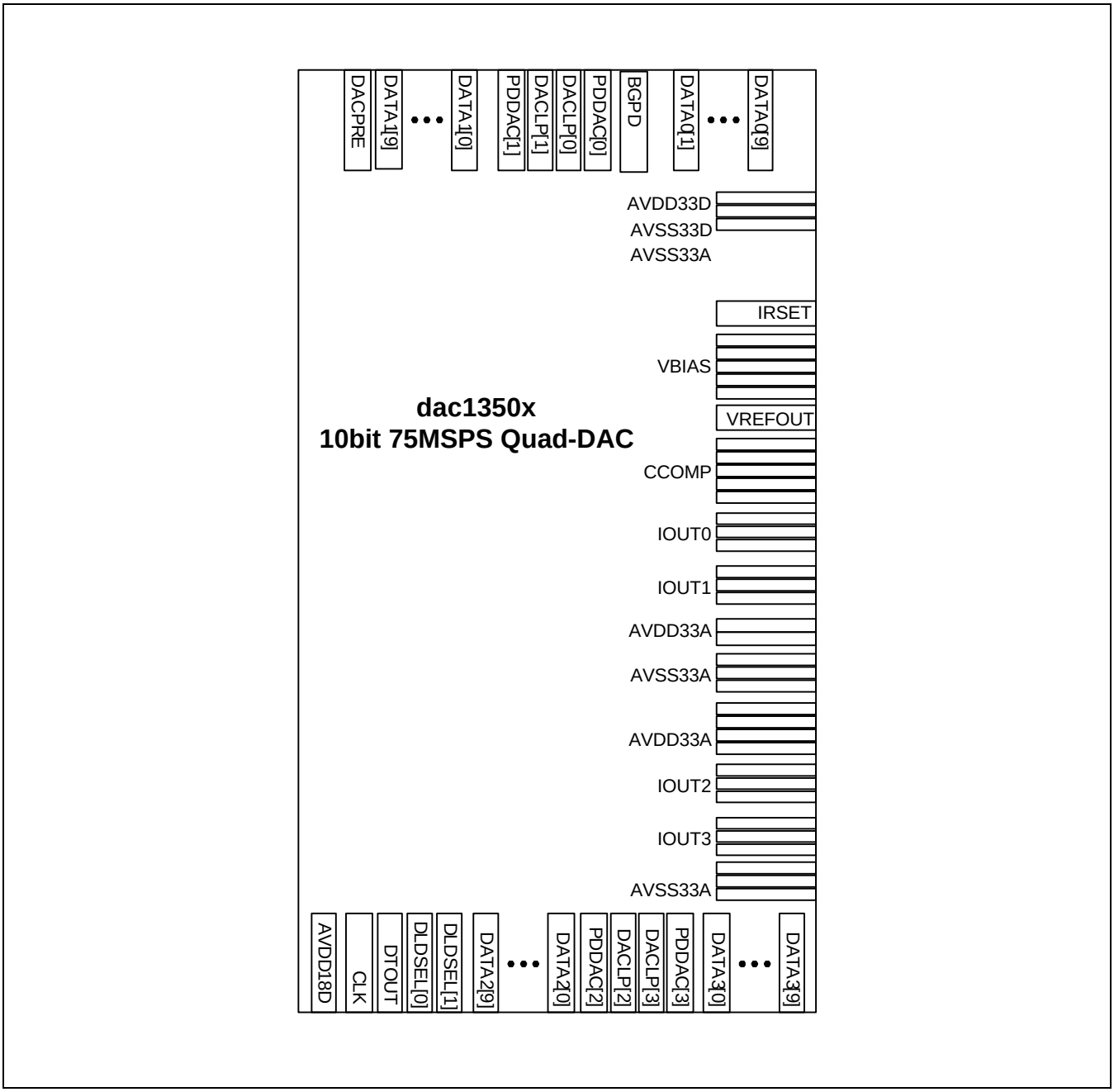
The voltage applied to VREFOUT is measured at IRSET node . And the voltage value is proportioned to the reference current value of resistor which is connected to IRSET node. So you can estimate the full scale current value by measuring the voltage, and check the DC characteristics of the OPAMP. For reference, as V_{BIAS} voltage applied to VREFOUT pin is given at IRSET node, the current flowing through R_{SET} resistor(connected to IRSET pin) is given as V_{REF}/R_{SET}.

If the voltage applied to VREFOUT pin is not same with IRSET node, you can say "This DAC chip does not work properly", because the internal OPAMP block makes the two node voltage(IRSET pin, VREFOUT pin) equal. And you have to check the CCOMP node to see the desired voltage on it. If the desired voltage is not measured, you can check the DAC output by appling a desired voltage to the CCOMP pin instead of compensation capacitor directly.

If you use internal reference voltage(BGR's output voltage) instead of external Vbias by setting the BGRSW low, you can check the BGR's output by checking the VBIAS pin voltage.

PHANTOM CELL INFORMATION

— Pins of the core can be assigned externally (Package pins) or internally (internal ports) depending on design methods.
The term "External" implies that the pins should be assigned externally like power pins.
The term "External/internal" implies that the applications of these pins depend on the user.



Pin Name	Pin Usage	Pin Layout Guide
AVDD33A	External	- Maintain the large width of lines as far as the pads.
AVSS33A	External	- place the port positions to minimize the length of power lines.
AVSS33D	External	- Do not merge the analog powers with another power from other blocks.
AVDD33D	External	- Use good power and ground source on board.
IRSET	External	- Maintain the larger width and the shorter length as far as the pads.
VREFOUT	External	- Separate from all other digital lines.
VBIAS	External	
CCOMP	External	
IOUT0	External	
IOUT3	External	
IOUT2	External	
IOUT1	External	
DTOUT	External/Internal	- Separated from the analog clean signals if possible.
DLDSEL [1:0]	External/Internal	- Do not exceed the length by 1,000um.
BGPD	External/Internal	
CLK	External/Internal	
DACPRE	External/Internal	
DACLP[3:0]	External/Internal	
PDDAC[3:0]	External/Internal	
DATA3[9:0]	External/Internal	
DATA2[9:0]	External/Internal	
DATA1[9:0]	External/Internal	
DATA0[9:0]	External/Internal	

BOARD LAYOUT CONSIDERATIONS

1. PC Board Considerations

To minimize noise on the power lines and the ground lines, the digital inputs need to be shielded and de-coupled. This trace length between groups of vdd (AVDD33A,AVDD33A) pins short as possible so as to minimize inductive ringing.

2. Supply Decoupling and Planes

For the de-coupling capacitor between the power line and the ground line, 0.1mF ceramic capacitor is used in parallel with a 10mF tantalum capacitor.

The digital power plane(AVDD33A) and analog power plane(AVDD33A) are connected through a ferrite bead, and also the digital ground plane(AVSS33A) and the analog ground plane(AVSS33A). This ferrite bead should be located within 3inches of the dac1350x The analog power plane supplies power to the dac1350x of the analog output pin and related devices.

3. Analog Signal Interconnection

To minimized noise pickup and reflections due to impedance mismatch, the dac1350x should be located as close as possible to the output connector.

The line between DAC output and monitor input should also be regarded as a transmission line. Due to the fact, it can cause problems in transmission line mismatch. As a solution to these problems, the double-termination methods used By using this, both ends of the termination lines are matched, providing an ideal, non-reflective system.

LAYOUT GUIDE (OPTIONAL)

Layout DAC Core Replacement

- It is recommended that you use thick analog power metal. when connecting to PAD, the path should be kept as short as possible, and use branch metal to connect to the center of analog switch block.
- It is recommended that you use thick analog output metal(at least more than 25mm) when connecting to PAD, and also the path length should be kept as short as possible.
- Digital power and analog power are separately used.
- When it is connected to other blocks, it must be double shielded using N-well and P+ active to remove the substrate and coupling noise. In that case, the power metal should be connected to PAD directly.
- Bulk power is used to reduce the influence of substrate noise.
- You must use more than two pins for AVDD33A because it require much current dissipation(about 93mA)
- It is recommended that analog metal line(including IRSET,VREFOUT,IOUT0,IOUT1,IOUT2,IOUT3) and analog power metal line should be layout alone and should not mixed with other noisy digital metal lines.
- If this core is used as a function block in larger main chip, you can join digital power metal of this core with the main digital power instead of using new digital power pad for this core. But you must use new analog power pad for the analog power of this core.

FEEDBACK REQUEST

We appreciate your interest in our products. If you have further questions, please specify in the attached form. Thank you very much.

DC / AC Electrical Characteristic					
Characteristics	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
Supply Voltage				V	
Power dissipation				mW	
Resolution				Bits	
Analog Output Voltage				V	
Operating Temperature				°C	
Output Load Capacitor				μF	
Output Load Resistor				Ω	
Integral Non-Linearity Error				LSB	
Differential Non-Linearity Error				LSB	
Maximum Conversion Rate				MHz	

Voltage Output DAC					
Characteristics	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
Reference Voltage TOP BOTTOM				V	
Analog Output Voltage Range				V	
Digital Input Format	Binary Code or 2's Complement Code				

Current Output DAC					
Characteristics	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
Analog Output Maximum Current				mA	
Analog Output Maximum Signal Frequency				MHz	
Reference Voltage				V	
External Resistor for Current Setting (RSET)				Ω	
Pipeline Delay				sec	

— Do you want to Interal Reference Voltage(BGR)?

— Which do you want to Serial Input TYPE or parallel Input TYPE?

— Do you need 3.3v and 5v power supply in your system?

— How many channels do you need ?

HISTORY CARD

Version	Date	Modified Items	Comments
Ver 1.0		Newly registered by circuit designer Kwang-Hee Lee	
Ver 1.1	'01.08.05	pin map , absolute maximum power , operating power range.	
Ver 1.2	'01.08.28	Typo correction.	
Ver 1.3	'01.10.20	- IOUT1,IOUT2,IOUT3,IOUT4 → IOUT0,IOUT1,IOUT2,IOUT3 - DACLP0,1,2,3 → DACLP[3:0] - PDDAC0,1,2,3 → PDDAC[3:0] - remove AVBB pin - Connect 0.1uF cap between VBIAS and AVDD33A in CORE APPLICATION GUIDE - Power port AVDD33A(3EA) → 4EA	
Ver 1.4	'02.03.01	-Load detect selection sequence DLDSEL(00) ⇒ IOUT0 DLDSEL(01) ⇒ IOUT2 DLDSEL(10) ⇒ IOUT1 DLDSEL(11) ⇒ IOUT3	page2
Ver 1.5	'02.04.19	- Add New item - DAC to DAC Cross talk - DAC to DAC mismatching (±2.5%) - DAC to DAC mismatch for any power down signal(±2.5%) - Recommend connect resistor(100ohm) to VBIAS pin to AVDD33A in series capacitor(0.1uF) - Recommend resistor (Rset=570ohm) for I_{FS} = 34.8mA - PSRR = -40dB(min) - voltage reference variance 0.7V ±10%	
Ver1.6	'02.04.30	- Add New Item SNDR THD	
Ver1.7	'02.05.11	- Full Scale Current +/- 10% on page 6	
Ver1.8	'02.05.23	- Power Operation Voltage 3.1 ~ 3.5V ==> 3.0V ~ 3.6V	