

GENERAL DESCRIPTION

dac1269x is a CMOS 12Bit D/A converter for general application. This digital to analog converter has a R-string structure.

Its settling time is 500ns (Typical value).

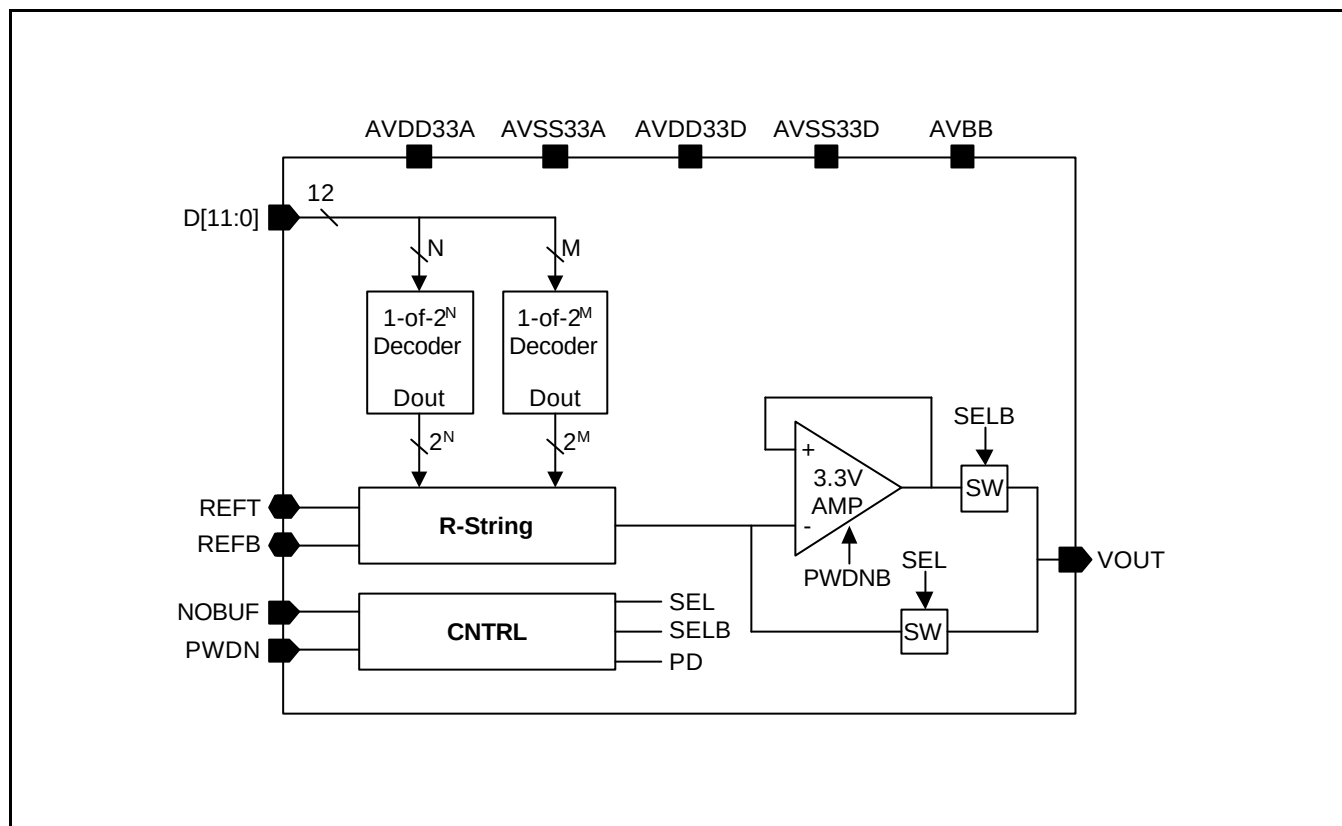
FEATURES

- Resolution : 12-Bit
- Differential Linearity Error : ± 1.0 LSB
- Integral Linearity Error : ± 2.0 LSB
- Settling Time : 500ns
- Low Power Consumption : 1.5mA
- Power Down Mode
- Operation Temperature Range : 0°C – 70°C
- Power Supply : 3.3V Single

TYPICAL APPLICATIONS

- Hard Disk Drive (HDD)
- Battery Operated Instruments
- Motor Control Systems
- General Applications

FUNCTIONAL BLOCK DIAGRAM



Ver 1.1 (Feb. 2002)

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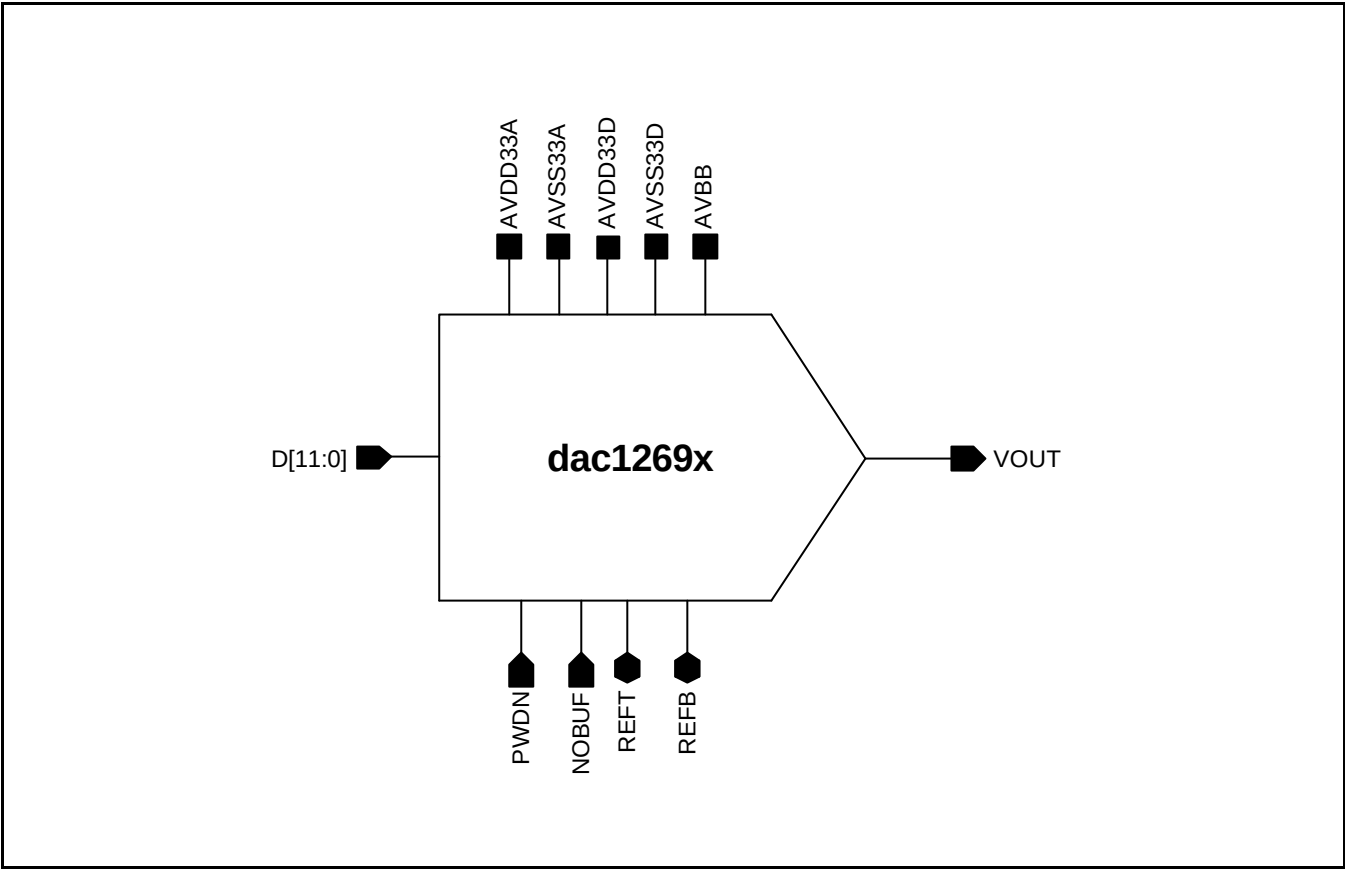
CORE PIN DESCRIPTION

Pin Name	I/O Type	I/O Pad	Pin Description
D[11:0]	DI	phicc_abb	Digital Input Data (12bit) D[11] : MSB , D[0] : LSB
NOBUF	DI	phicc_abb	Amp Selection (High : No Amp)
PWDN	DI	phicc_abb	Power Down (Active High)
REFT	AB	phoa_abb	Voltage Reference Top(max:0.9×AVDD33A)
REFB	AB	phoa_abb	Voltage Reference Bottom(min:0.1×AVDD33A)
VOUT	AO	phoa_abb	Analog Voltage Output
AVDD33A	AP	vdd3t_abb	Analog Power (+3.3V)
AVSS33A	AG	vdd3t_abb	Analog Ground (0.0V)
AVDD33D	DP	vdd3t_abb	Digital Power (+3.3V)
AVSS33D	DG	vss3t_abb	Digital Ground (0.0V)
AVBB	AG	vbb3_abb	Analog Sub Bias (0.0V)

I/O Type Abbr.

- AI: Analog Input
- DI: Digital Input
- AO: Analog Output
- DO: Digital Output
- AB: Analog Bi-direction
- DB: Digital Bi-direction
- AP: Analog Power
- AG: Analog Ground
- DP: Digital Power
- DG: Digital Ground

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	VDD (AVDD33A, AVDD33D)	4.5	V
Analog Output Voltage	VOU _T	VSS to VDD	V
Digital Input Voltage	D[11:0]	VSS to VDD	V
Reference Voltage	REFT REFB	VDD VSS	V
Operating Temperature Range	T _{opr}	-45 to 120	°C

NOTES:

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS (AVSS33A or AVSS33D or AVBB) unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	AVDD33A - AVSS33A AVDD33D - AVSS33D	3.15	3.3	3.45	V
Supply Voltage Difference	AVDD33A - AVDD33D	-0.1	0.0	0.1	V
Reference Voltage	REFT REFB	1.0 0.3	– –	3.0 2.0	V
Digital Input 'Low' Voltage	V _{IL}	VSS	–	0.3×VDD	V
Digital Input 'High' Voltage	V _{IH}	0.7×VDD	–	VDD	V
Operating Temperature	T _{opr}	0	–	70	°C

NOTES:

1. Be sure that the voltage of REFT should be 1.0V larger than that of REFB at least.
2. It is strongly recommended that to avoid power latch-up all the supply pins (AVDD33A, AVDD33D) be driven from the same source.

DC ELECTRICAL CHARACTERISTICS

(Converter Specifications : AVDD33A=AVDD33D=3.3V, AVSS33A=AVSS33D=AVBB=0V, NOBUF=Low, PWDN=Low, Top=25°C, REFT=3.3V, REFB=0.0V unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Resolution	Bit	1	–	12	Bits	–
Differential Linearity Error	DLE	–	0.5	1.0	LSB	–
Integral Linearity Error	ILE	–	4.0	6.0	LSB	–
Zero Scale Error ⁽¹⁾	V _{ZSE}	–	0	30	mV	REFT = 3.0 V, REFB = 0.3V
Full Scale Voltage Error ⁽²⁾	V _{FSE}	–	10	50	mV	
Maximum Output Voltage	V _{O_MAX}	–	3.0	3.2	V	V _{O_MAX} = VOUT(D[11:0]=High) Criteria = DNL < 1LSB

NOTES:

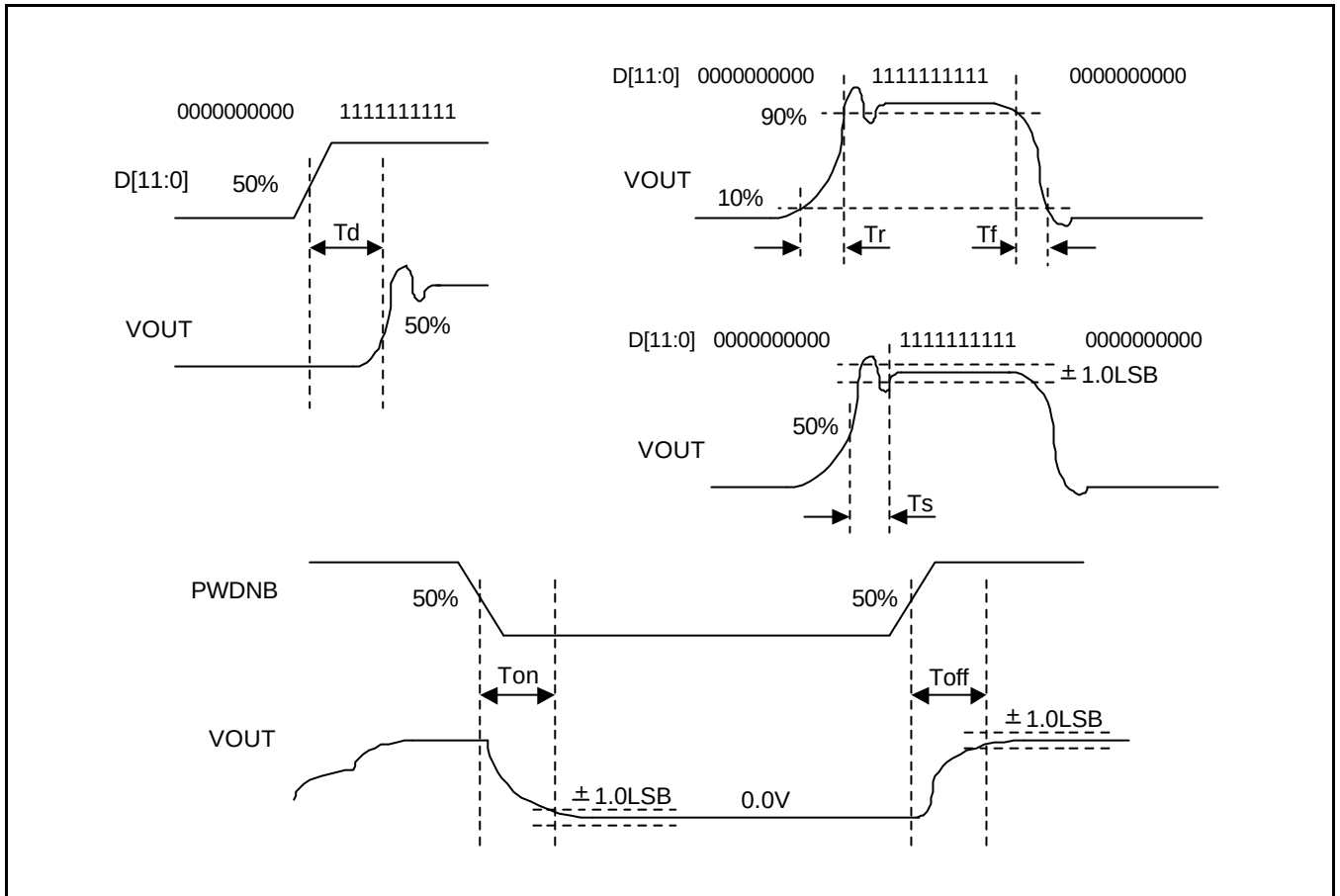
1. $V_{ZSE} = |VOUT(D[11:0] = Low) - REFB|$
2. $V_{FSE} = VOUT(D[11:0] = High) - \{(REFT-REFB) \times 4095/4096 + REFB\}$

AC ELECTRICAL CHARACTERISTICS

(Converter Specifications : AVDD33A=AVDD33D=3.3V, AVSS33A=AVSS33D=AVBB=0V, load cap=25pF, NOBUF=Low, Top=25°C, REFT=3.2V, VRB=0.1V unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Supply Current	I _{vdd1}	1.3	1.46	1.8	mA	I _{vdd1} = I _{VDDA} + I _{VDDD} VRT = 3.0V, VRB = 0.3V Data Input: 011111111111
	I _{vdd2}	1.3	2.0	2.5	mA	I _{vdd2} = I _{VDDA} + I _{VDDD} Data Input: All Low or All High
Supply Current (Power Down Mode)	I _{vdd3}	50	300	500	µA	I _{vdd3} = I _{VDDA} + I _{VDDD} Data Rate = 2MHz Load cap = 25pF, FWDN = High
Analog Output Delay	T _d	–	75	200	ns	Data Rate = 2MHz Data : All LOW → All HIGH
Analog Output Rise Time	T _r	–	140	200	ns	Data Rate = 2MHz Data : All LOW → All HIGH
Analog Output Fall Time	T _f	–	150	200	ns	Data Rate = 2MHz Data : All HIGH → All LOW
Analog Output Settling Time	T _s	–	270	500	ns	Data Rate = 2MHz Data : All LOW → All HIGH

TIMING DIAGRAM



NOTES:

1. Output delay measured from the 50% point of the rising edge of input data to the full scale transition.
2. Settling time measured from the 50% point of full scale transition to the output remaining within $\pm 1/2$ LSB.
3. Output rise/fall time measured between the 10% and 90% points of full scale transition.

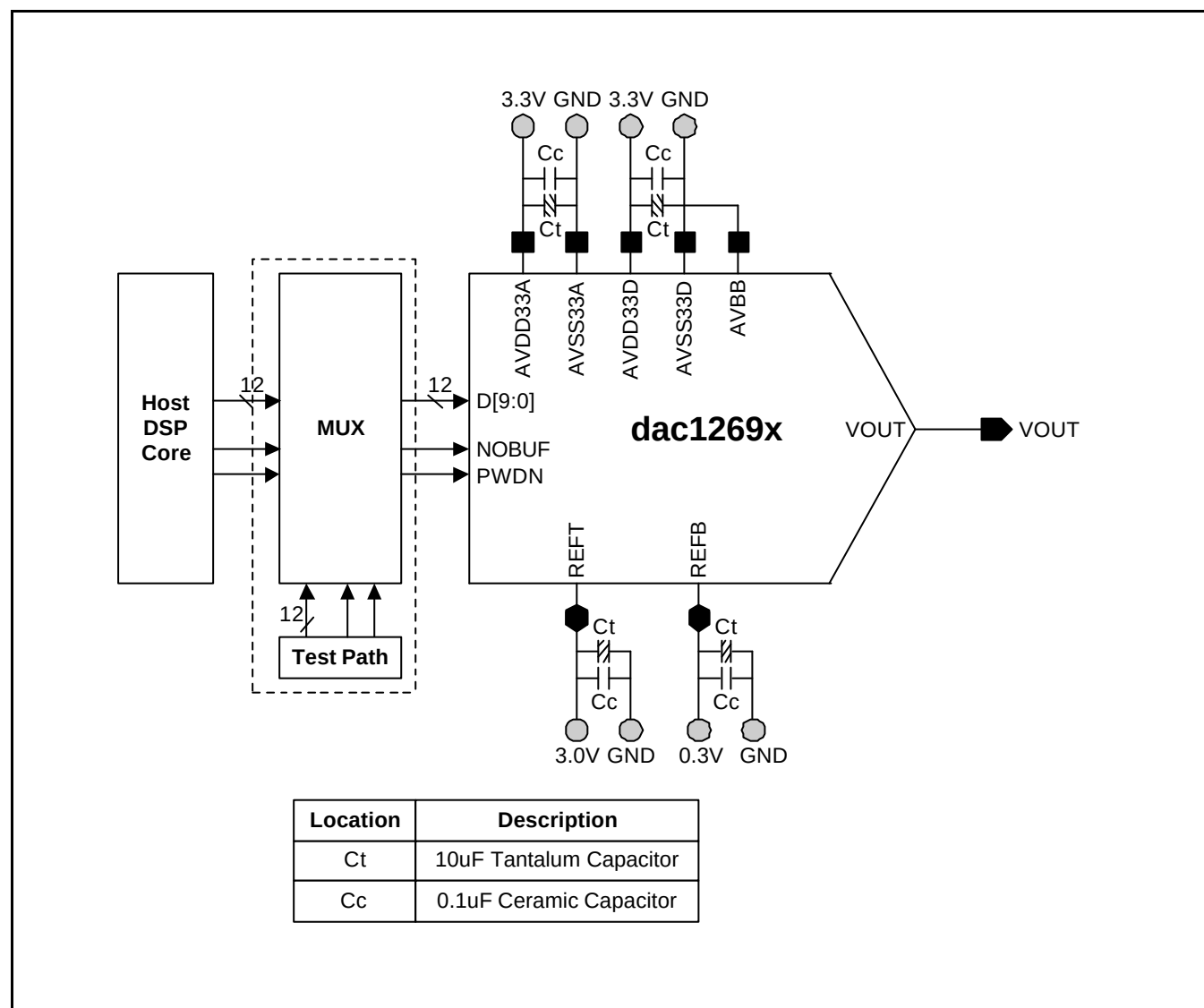
FUNCTIONAL DESCRIPTION

1. The dac1269x has a 12bit R-string block, two decoders, a OP amps, and control block.
2. The digital outputs of two decoders decide the voltage level of R-string block.

$$V_{Rstring} = \frac{REFT-REFB}{2^{12}} \sum_{n=0}^{11} (2^n \times D_n) + REFB$$

3. The CNTRL block controls several conditions which are the OP amp selection, and power down mode. If you use the dac1269x at 3.3V supply voltage with amp, next conditions is needed. (NOBUF=Low, PWDN=Low)
4. Normal Conditions : REFT=3.0V, REFB=0.3V, NOBUF=Low, PWDN=Low.
You can change the voltages of REFT and REFB to 3.3V and 0.0V, but the performance of dac1269x will be degraded.

CORE EVALUATION GUIDE

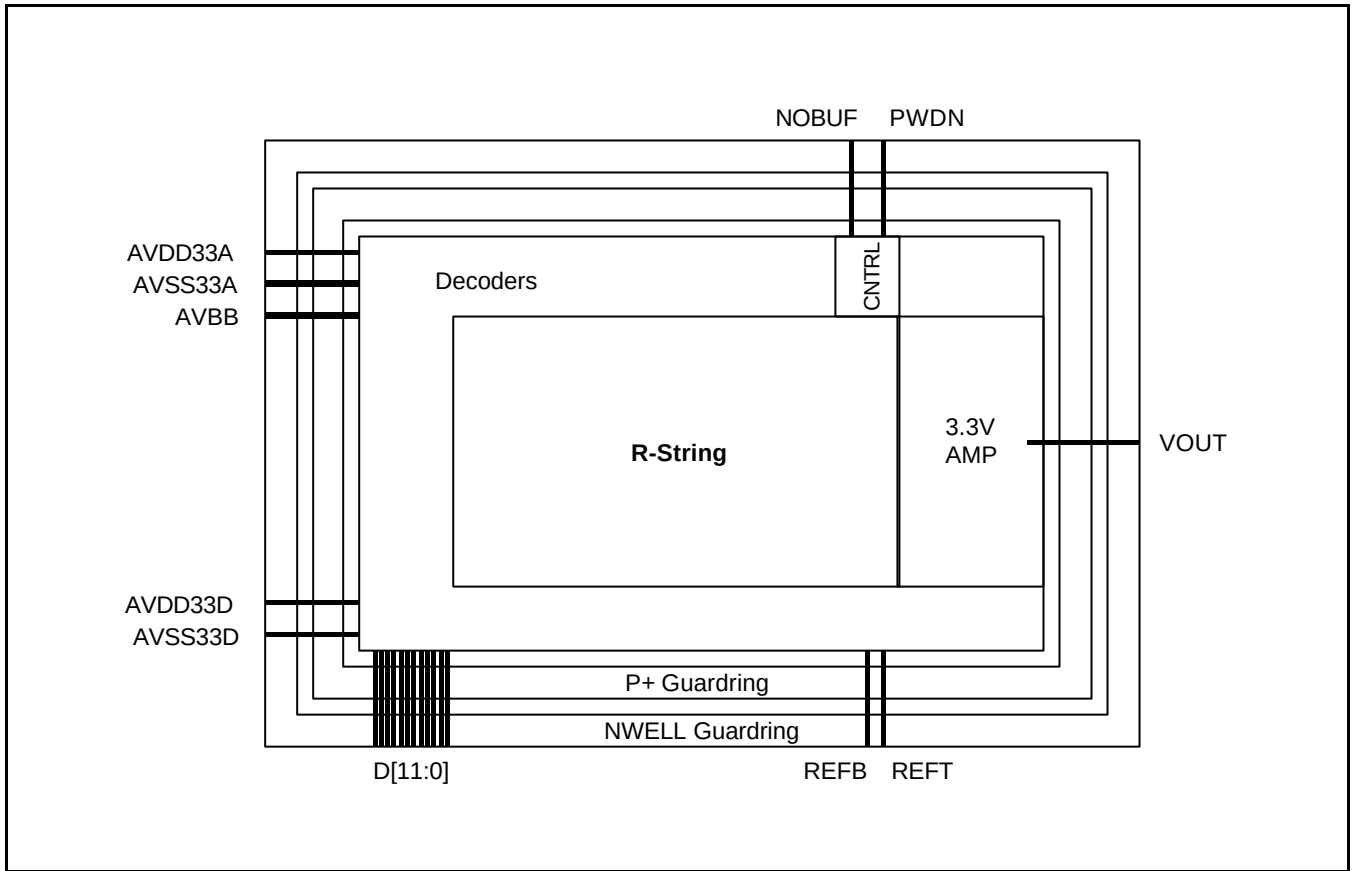


TESTABILITY

Whether you use MUX or the internal logic for testability, it is required to be able to select the values of digital inputs (D[11:0]).

See above figure. Only if it is, you can check the main function. (Linearity)
 Normal Test Condition : VRT=3.0V , REFB=0.3V , NOBUF=Low , PWDN=Low

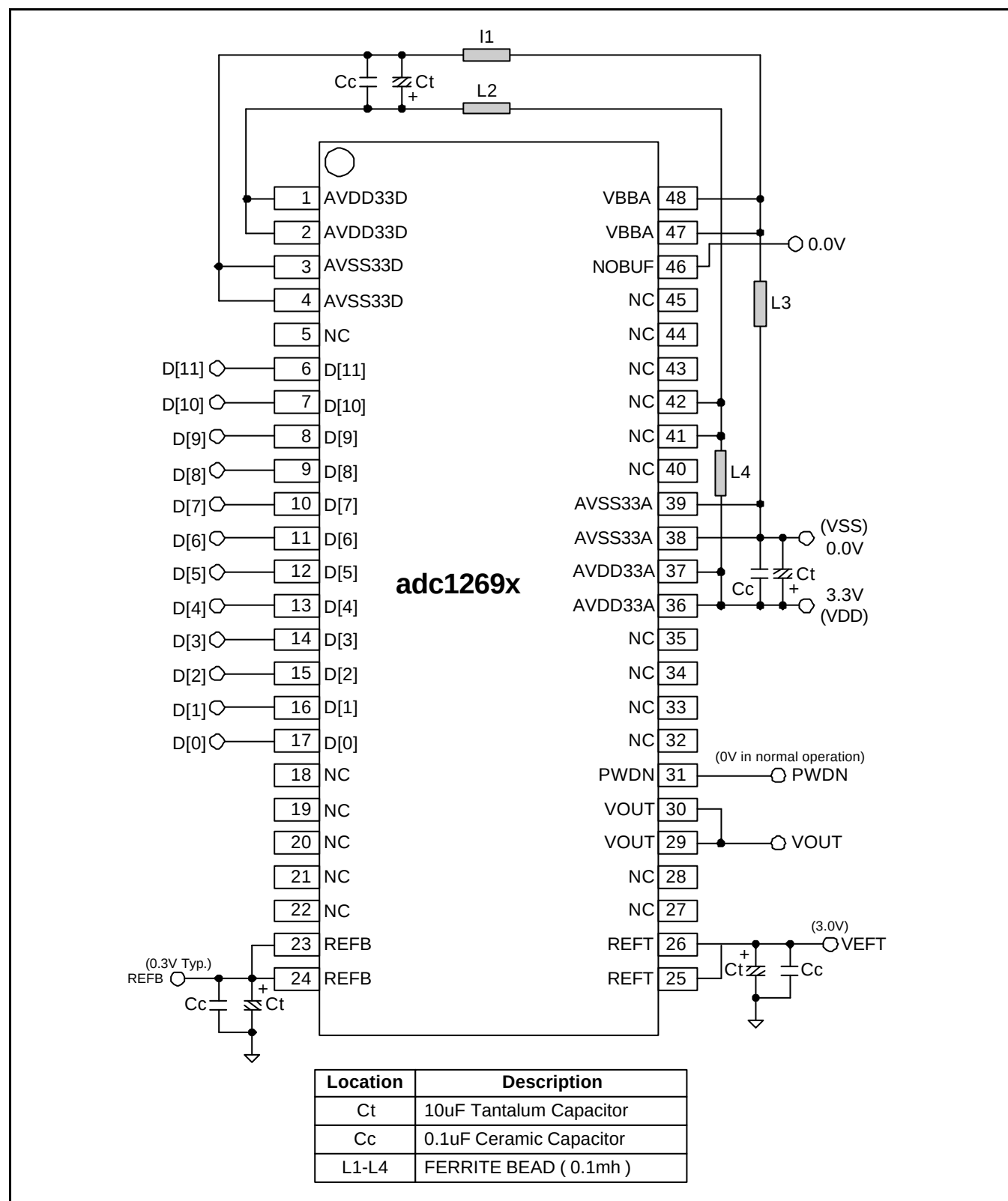
CORE LAYOUT GUIDE



NOTES:

1. It is recommended that you use thick analog power metal. when connecting to PAD, the path should be kept as short as possible.
2. Digital power and analog power are separately used.
3. When the core block is connected to other blocks, it must be double guard-ring using N-well and P+ active to remove the substrate and coupling noise.
In that case, the power metal should be connected to PAD directly.
4. The Bulk power is used to reduce the influence of substrate noise.
5. Digital input signal lines must be same length to reduce the difference of delay.

PACKAGE CONFIGURATION



PACKAGE PIN DESCRIPTION

NAME	PIN NO	I/O TYPE	PIN DESCRIPTION
AVDD33D	1,2	DP	Digital Power (3.3V)
AVSS33D	3,4	DG	Digital Ground (0.0V)
D[11:0]	6~17	DI	Digital Input Data
REFB	23,24	AB	Voltage Reference Bottom (0.3V)
REFT	25,26	AB	Voltage Reference Top (3.0V)
VOUT	29,30	AO	Analog Voltage Output
PWDN	31	DI	Power Down Mode (High Active)
AVDD33A	36,37	AP	Analog Power (3.3V)
AVSS33A	38,39	AG	Analog Ground (0.0V)
NOBUF	46	DI	Amp Selection Mode (Low : Amp(Buffer) Selected)
AVBB	47,48	AG	Analog Sub Bias (0.0V)
NC	5,18,19,20,21,22,27,28,32,33,34,35,40,41,42,43,44,45	DO	No Connection

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BOARD LAYOUT CONSIDERATION

1. PC Board Considerations

To minimize noise on the power lines and the ground lines, the digital inputs need to be shielded and decoupled. This trace length between groups of VDD (AVDD33A, AVDD33D) and VSS (AVSS33A, AVSS33D) pins should be as short as possible so as to minimize inductive ringing.

2. Supply Decoupling and Planes

For the decoupling capacitor between the power line and the ground line, 0.1uF ceramic capacitor is used in parallel with a 10uF tantalum capacitor. The digital power plane(AVDD33D) and analog power plane(AVDD33A) are connected through a ferrite bead, and also the digital ground plane(AVSS33D) and the analog ground plane(AVSS33A). This ferrite bead should be located within 3inches of the dac1269x. The analog power plane supplies power to the dac1269x of the analog output pin and related devices.

FEEDBACK REQUEST

We appreciate your interest in our products. If you have further questions, please specify in the attached form. Thank you very much.

DC / AC Electrical Characteristic					
Characteristics	Min	Typ	Max	Unit	Remarks
Supply Voltage				V	
Power dissipation				mW	
Resolution				Bits	
Analog Output Voltage				V	
Operating Temperature				°C	
Output Load Capacitor				pF	
Output Load Resistor				°C	
Integral Non-Linearity Error				LSB	
Differential Non-Linearity Error				LSB	
Maximum Conversion Rate				MHz	

Voltage Output DAC					
Characteristics	Min	Typ	Max	Unit	Remarks
Reference Voltage TOP BOTTOM				V	
Analog Output Voltage Range				V	
Digital Input Format	Binary Code or 2's Complement Code				

Current Output DAC					
Characteristics	Min	Typ	Max	Unit	Remarks
Analog Output Maximum Current				mA	
Analog Output Maximum Signal Frequency				kHz	
Reference Voltage				V	
External Resistor for Current Setting (RSET)				W	
Pipeline Delay				sec	

- Do you want to Power down mode?
- Do you want to Internal Reference Voltage (BGR)?
- Which do you want to serial input type or parallel input type?
- Do you need 1.8V, 2.5V, 3.3V or 5V power supply in your system?

HISTORY CARD

Version	Date	Modified Items	Comments
Ver 1.0	00.07.19	Newly registered by circuit designer Koo Hyung-Woan	
Ver 1.1	02.02.20	Modify the output range	