GENERAL DESCRIPTION

This is CMOS 10-bit D/A Converter for general applications. Its typical conversion rate is 165MHz and Supply voltage is 3.3V.

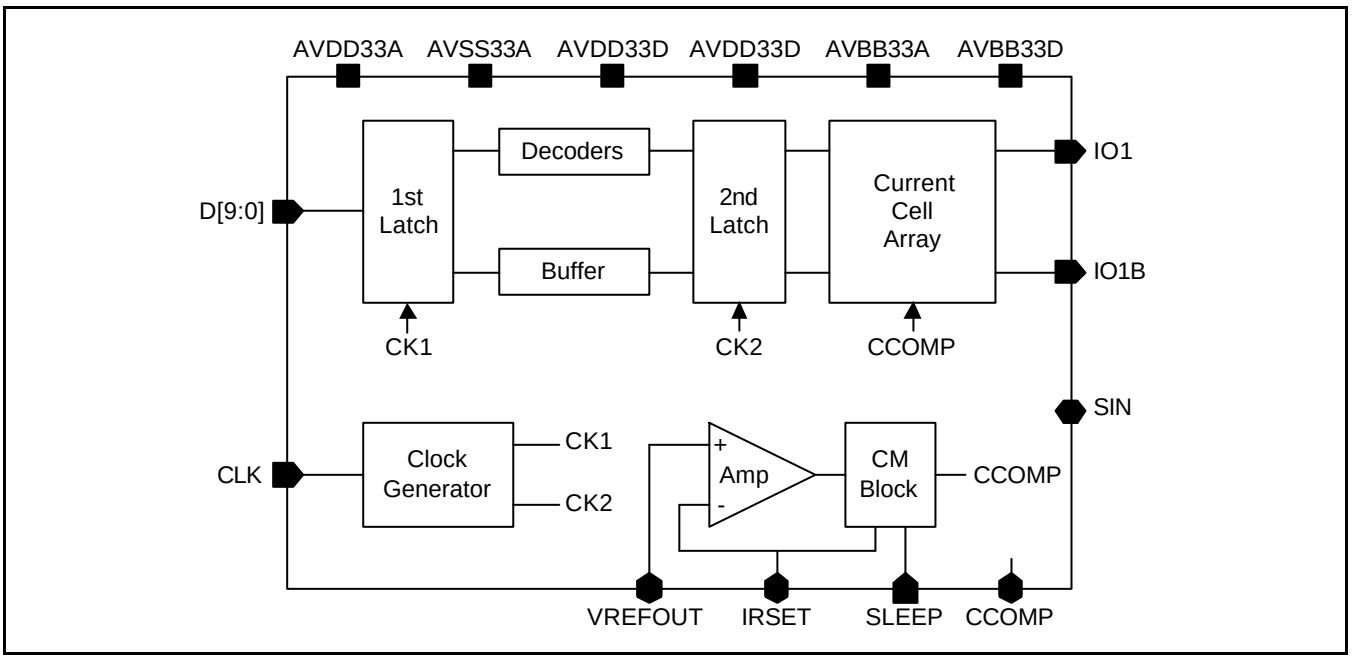
FEATURES

— 300MHz Operation
— +3.3V power supply
— BGR (Internal/External))
— 10-bit Voltage parallel Input
— Power Down mode (High active)

TYPICAL APPLICATIONS

— Graphic display
— General purpose high-speed
— Digital Camera

FUNCTIONAL BLOCK DIAGRAM



Ver 1.8 (Apr. 2002)

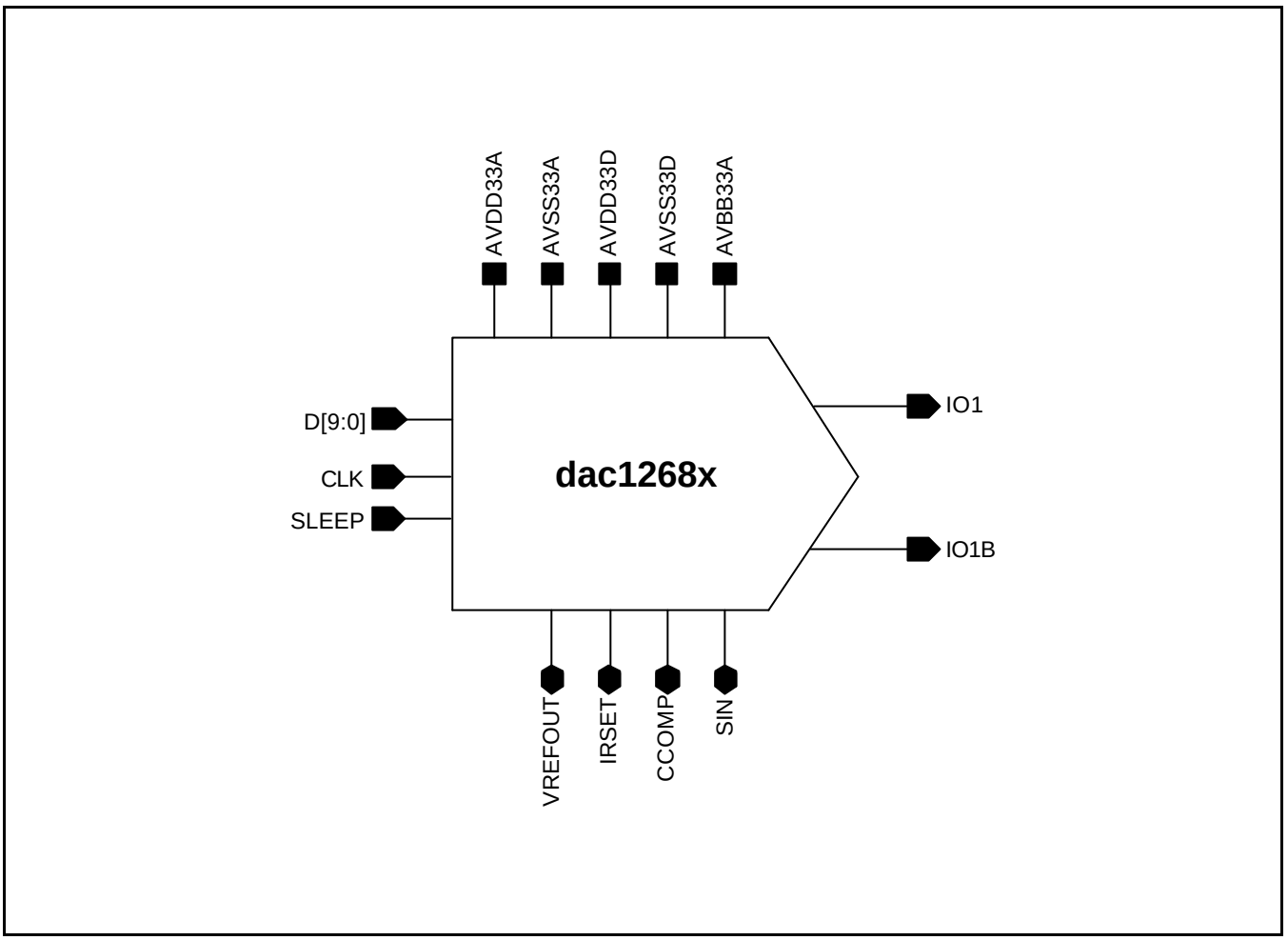
CORE PIN DESCRIPTION

Pin Name	I/O Type	I/O Pad	Pin Description
IO1,IO1B	AO	phoa_abb	Analog DAC output
D[9:0]	DI	phicc_abb	Digital input
CLK	DI	phicc_abb	Clock
SLEEP	DI	phicc_abb	Power down mode (hign active)
VREFOUT	AB	phoa_abb	Reference voltage input & monitoring
CCOMP	AB	phoa_abb	External capacitance connection
SIN	AB	phoa_abb	External capacitance connection
IRSET	AB	phoa_abb	external resistor connection
AVDD33D	DP	vdd3t_abb	Digital Power
AVSS33D	DG	vss3t_abb	Digital Ground
AVDD33A	AP	vdd3t_abb	Analog Power
AVSS33A	AG	vss3t_abb	Analog Ground
AVBB33A	AG	vbb3t_abb	Analog Bulk
AVBB33D	AG	vbb3_abb	Digital Bulk

I/O Type Abbr.

— AI: Analog Input
— DI: Digital Input
— AO: Analog Output
— DO: Digital Output
— AB: Analog Bi-direction
— DB: Digital Bi-direction
— AP: Analog Power
— AG: Analog Ground
— DP: Digital Power
— DG: Digital Ground

CORE CONFIGURATION



FUNCTIONAL DESCRIPTION

This is 10bit 165MSPS digital to analog data converter and uses segment architecture for 5bits of MSB sides , binary-weighted architecture for 5bits of LSB side and master slave architecture for 2bit of LSB. it contains of First latch block, decoder block Second latch block, AMP block ,BGR block, switch buffer block, SLEEP block for power down, CM (current mirror) block and analog switch block. This core uses reference current to decide the 1LSB current size by dividing the reference current by 32times. So the reference current must be constant and the switch's physical real size can be constant by using OPA block with high DC gain. The most significant block of this core is analog switch block and it must maintain the uniformity at each switch, so layout designer must care of the matching characteristics on analog switch and CM block. And more than 80% of supply current is dissipated at analog switch block and AMP block. And it uses samsung (SEC) standard cell as all digital cell of latch ,decoder and buffer. And to adjust full current output, you must decide the "Rset" resistor value (connected to IREF pin) and "Vbias" voltage value (connected to VREFOUT pin). Its voltage output can be obtained by connecting RL1(connected to IO1, IO1B pin) .

Linearity Error : Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Monotonicity : A D/A converter is monotonic if the output either increases or remains constants as the digital input increases.

Offset Error : The deviation of the output current from the ideal of zero is called offset error. For IO, 0mV output expected when the inputs are all 0s.

Gain Errors : The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Output Compliance Range : The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown resulting in nonlinear performance.

Settling Time : The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse : Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	AVDD33D, AVDD33A	-0.5 to 3.3	V
Voltage on any Digital Input Voltage	Vin	AVSS33A-0.3 to AVDD33A+0.3	V
Storage Temperature Range	Tstg	-55 to +150	°C

NOTES:

1. It is strongly recommended that to avoid power latch-up all the supply Pins(AVDD33A,AVSS33A) be driven from the same source.
2. Absolute Maximum Rating values applied individually while all other parameters are within specified operating conditions.
   Function operation under any of these conditions is not implied.
3. Applied voltage must be current limited to specified range.
4. Absolute Maximum Ratings are value beyond which the device may be damaged permanently. Normal operation is not guaranteed.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage	AVDD33A	3.0	3.3	3.6	V
Digital Input Voltage High	VIH	0.7×AVDD33A	–	–	V
Digital Input Voltage Low	VIL	–	–	0.3×AVDD33A	V
Operating Temperature Range	T_{OPR}	-40	33	85	°C

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Resolution	10	–	–	–	Bits
Differential Linearity Error	DLE	–	–	±1	LSB
Integral Linearity Error	ILE	–	–	±2	LSB
Monotonicity	Guaranteed				
Maximum Output Compliance	Voc	0	–	+1.2	V
Internal BGR Reference Voltage	–	0.63	0.7	0.77	V
Full Scale Output Current	Ifs	15.87	16.7	17.54	mA
Power Supply Current	Is	17	18.35	23	mA

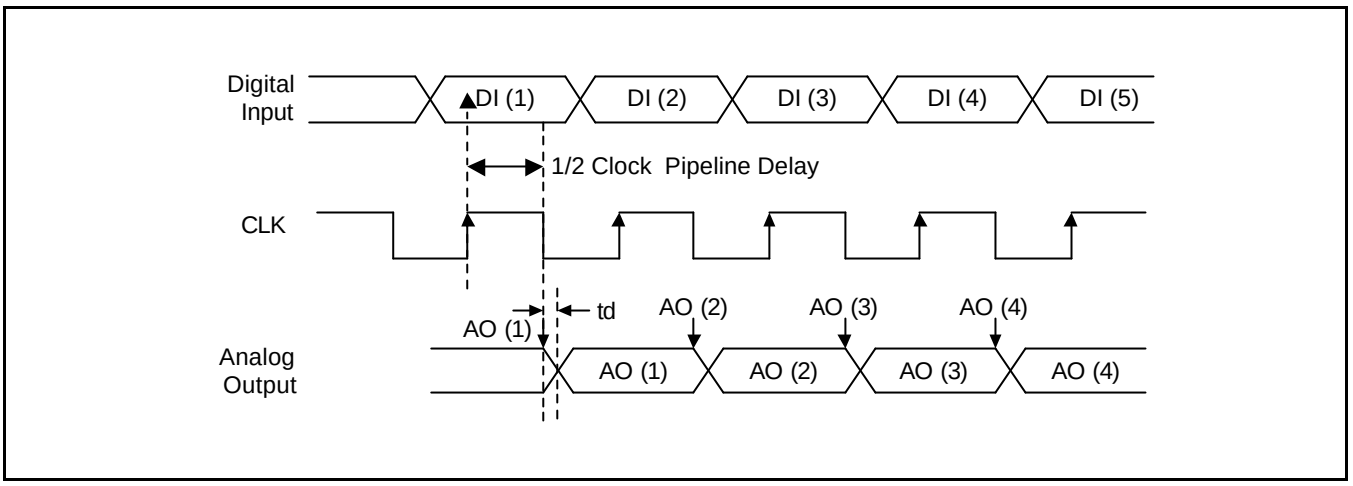
NOTES:
1. White to Black Pedestal Voltage can be changed by using external RSET resistor
2. Converter Specifications (unless otherwise specified)
   AVDD33A=3.3V AVDD33D=3.3V AVSS33A=GND AVSS33D=GND
   Ta=33°C C(load)=10pF VREFOUT=0.7V

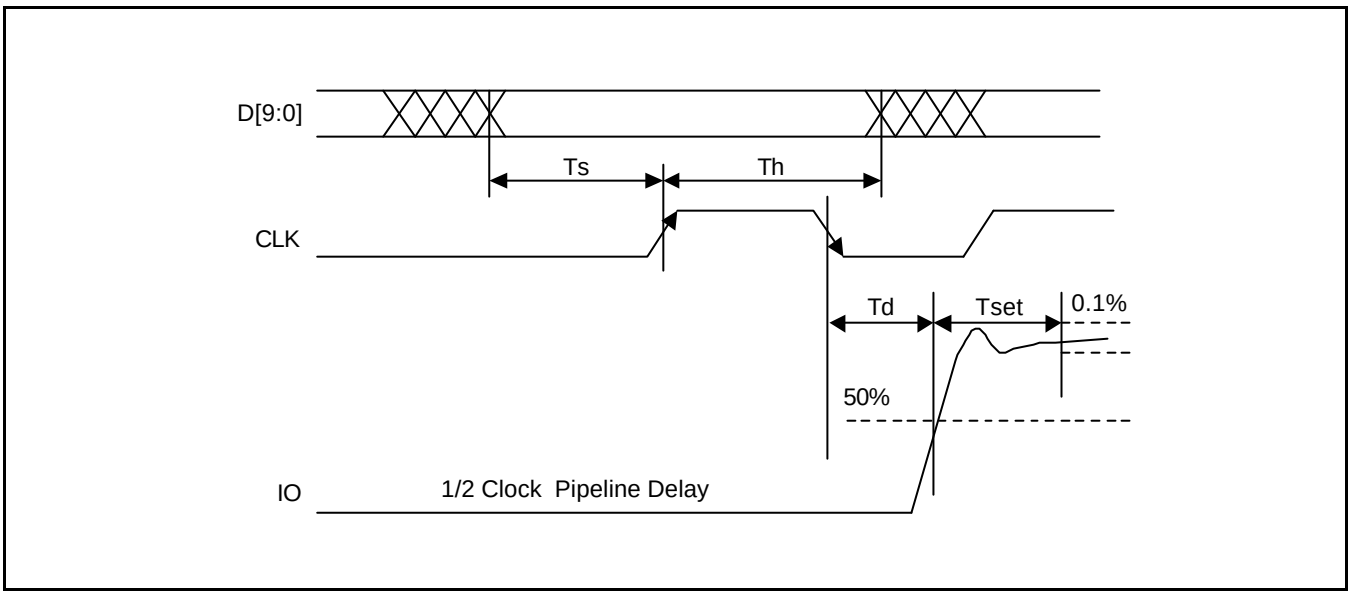
AC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Conversion Speed	Fop	165	–	–	MHz
Analog Output Delay	Td	–	0.5	2	ns
Analog Output Rise Time	Tr	–	0.24	2	ns
Analog Output Fall Time	Tf	–	0.98	2	ns
Analog Output Settling Time	Ts	–	114.5	200	ns
Glitch Impulse	GI	-100	31.7	100	pVsec
Setup Time	Ts	–	–	0.5	nsec
Hold Time	Th	–	–	0.5	nsec
THD (Total Harmonic Distortion)	THD	-55	-65	–	dB
SNDR (Fin=5MHz, Fck=160MHz)	SNDR	-48	-56	–	dB

NOTES:
1. The above parameters are guaranteed over the full temperature range.
2. Clock and data feed through is a function of the amount of overshoot and undershoot on the digital inputs. Settling time does not include clock and data feed through . Glitch impulse include clock and data feed through.
3. Setup and Hold Time are simulation values, not a test result.

TIMING DIAGRAM

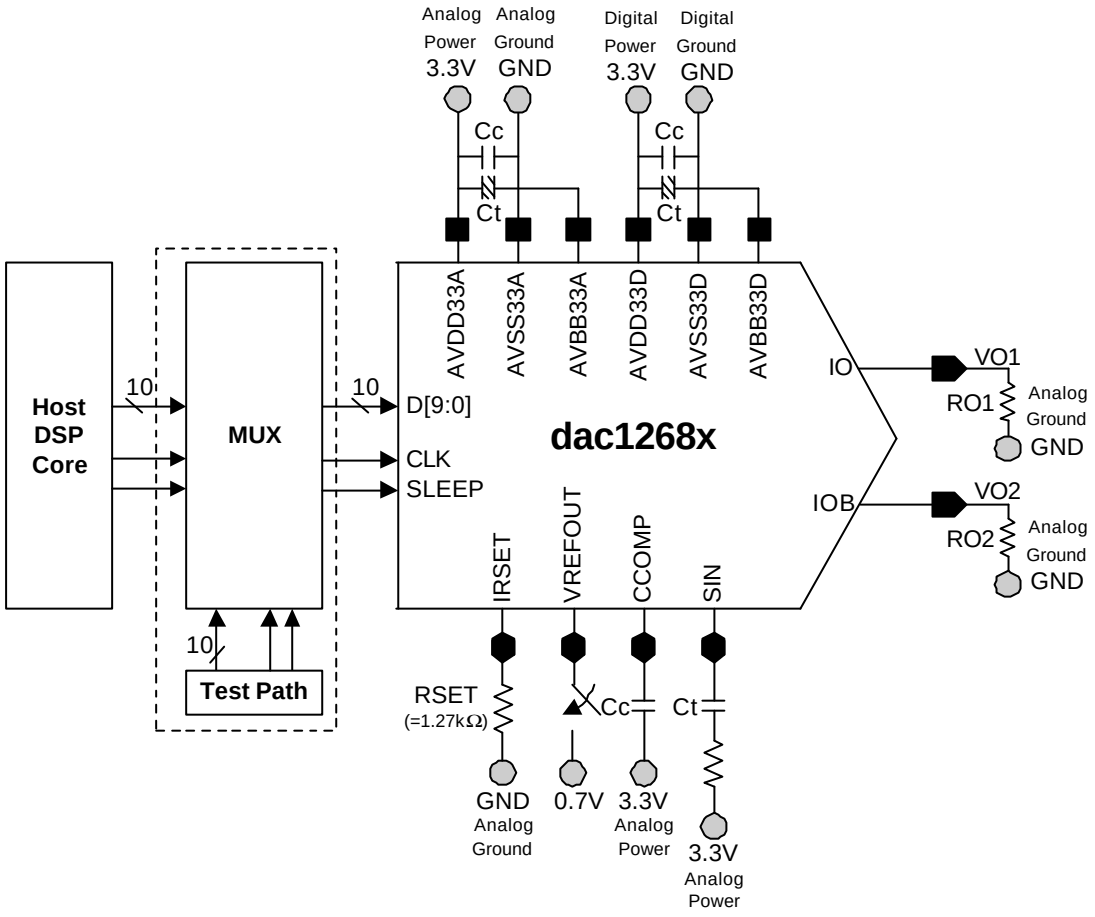




NOTES:

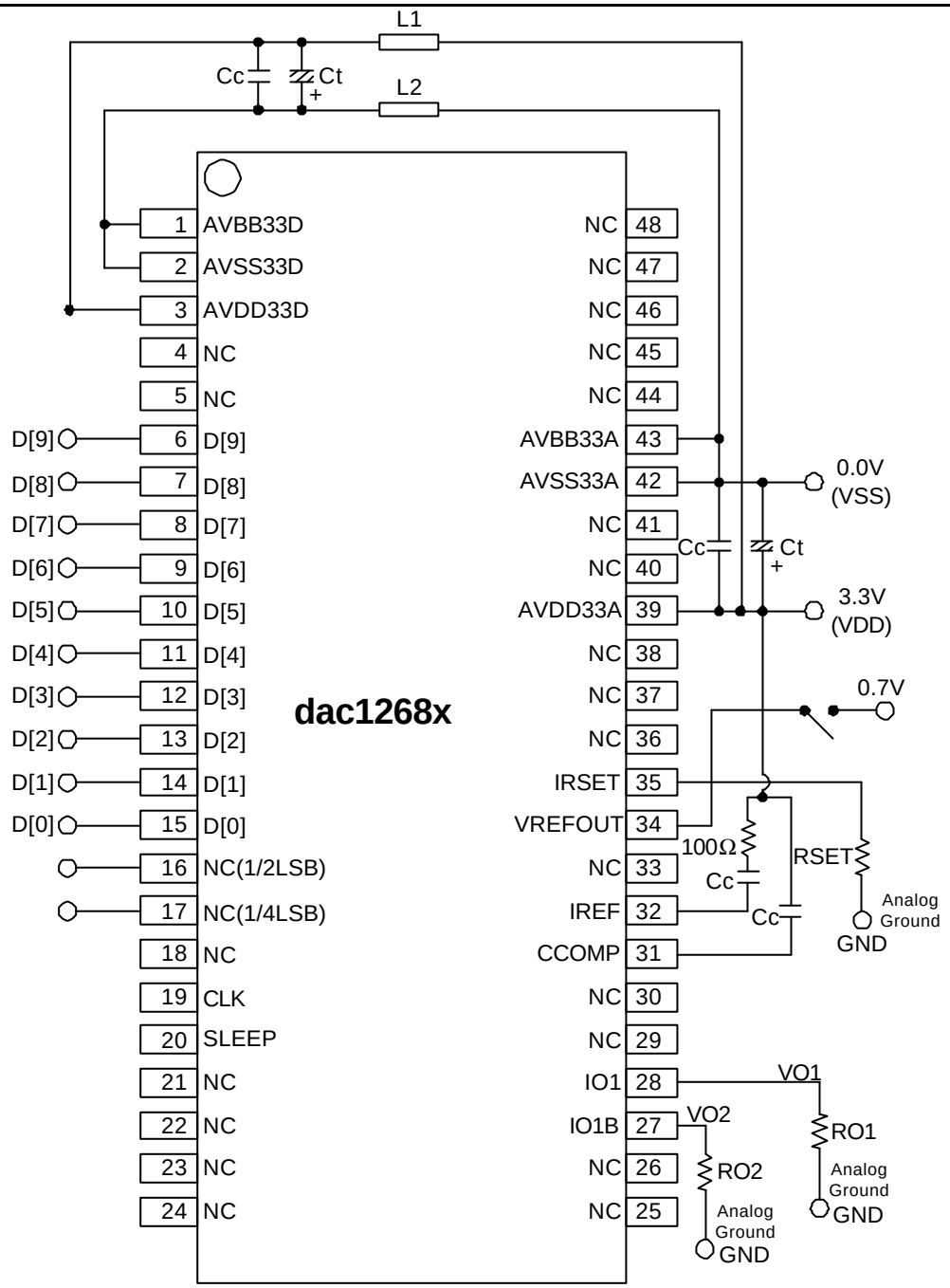
1. Output delay measured from the 50% point of the rising edge of CLK to the full scale transition
2. Settling time measured from the 50% point of full scale transition to the output remaining within ±1,2LSB.
3. Output rise/fall time measured between the 10% and 90% points of full scale transition.

CORE EVALUATION GUIDE



Location	Description
Cc	0.1uF
RSET	1.27kΩ
RO1, RO2	37.5Ω
Ct	10uF

TEST CHIP EVALUATION GUIDE



Location	Description
C1	10uF Capacitor
C2	0.1uF Ceramic Capacitor
Ro1, Ro2	37.5Ω Resistor
RSET	1270Ω 1% Metal File Resistor

NOTES

caution(1) :
1. This chip was originally made with the target of 12 bit resolution.
2. You should test this sample chip only as a single output that is probing only between ground and IO1 neglecting IO1B with applying GND to NC PIN(#16,#17).
3. If you want to test it as differential output you should apply as follows.
   – apply GND to NC(#16)
   – apply VDD to NC(#17)
   – then probe the output between IO1 and IO1B.
4. If you want single output (IO1), connect NC(#16,17) pin to VSS .

caution(2) : 1. Probe Pin #34,#35 , you will see 0.7V in these nodes.

Caution(4) : Pin #20(SLEEP)
1. In case of operating this chip properly, you have to put GND to this pin. If you want to check power down mode, apply VDD to this pin.

The voltage is scaled factor of 1/32 for VIDEO. The full scale current is given as the decimal value equivalent to the digital code.

1. Resolution

If you want to change the resolution, use as many appear bits as you want and connect the rest lower bits to the ground as above diagram which is 10bit application.

2. Output Range Alteration

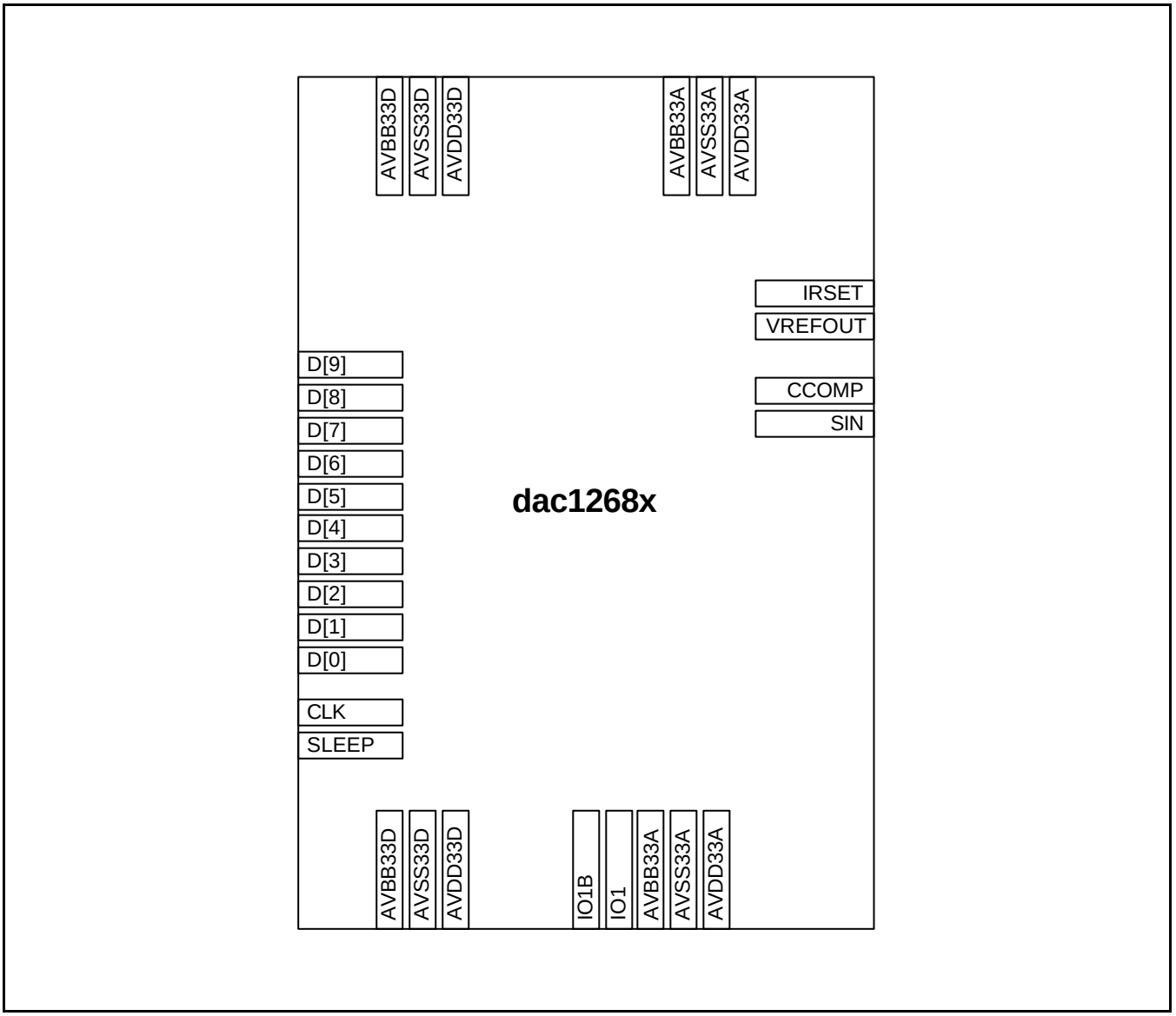
In order to change the output swing, use following equation.

Vout = {V(IRSET)/(RSET´32)} ´(DAC_CODE)´Rio

Output swing level is a function of V(IRSET), RSET, and Rio, The maximum output swing level is 0.66V.

PHANTOM CELL INFORMATION

Pins of the core can be assigned externally (Package pins) or internally (internal ports) depending on design methods.
The term "External" implies that the pins should be assigned externally like power pins.
The term "External/internal" implies that the applications of these pins depend on the user.



Pin Name	Pin Usage	Pin Layout Guide
VDDA	External	1. Maintain the large width of lines as far as the pads.
VSSA	External	2. Place the port positions to minimize the length of power lines.
VBB	External	3. Do not merge the analog powers with another power from other blocks.
VDDD	External	4. Use good power and ground source on board.
VSSD	External	
CCOMP	External	1. Do not overlap with digtal lines.
IRSET	External	2. Maintain the shortest path to pads.
SIN	External	3. Separate from all other analog signals.
IO1B	External	4. Maintain the larger width and the shorter length as far as the pads.
IO1	External	5. Separate from all other digital lines.
CLK	External/Internal	1. Separated from the analog clean signals if possible.
SLEEP	External/Internal	2. Do not exceed the length by 1,000um.
D[9]	External/Internal	3. In Phantom cell in case of many ports of one power name, you must drag
D[8]	External/Internal	the ports individually to PAD in parallel.
D[7]	External/Internal	4. Customer must use two PAD's individually for analog power ports because
D[6]	External/Internal	of PAD's current limitation.
D[5]	External/Internal	
D[4]	External/Internal	
D[3]	External/Internal	
D[2]	External/Internal	
D[1]	External/Internal	
D[0]	External/Internal	

FEEDBACK REQUEST

We appreciate your interest in out products. If you have further questions, please specify in the attached form. Thank you very much.

DC/AC Electrical Characteristic					
Characteristics	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
Supply Voltage				V	
Power dissipation				mW	
Resolution				Bits	
Analog Output Voltage				V	
Operating Temperature				°C	
Output Load Capacitor				pF	
Output Load Resistor				Ω	
Integral Non-Linearity Error				LSB	
Differential Non-Linearity Error				LSB	
Maximum Conversion Rate				MHz	

Voltage Output DAC					
Characteristics	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
Reference Voltage TOP BOTTOM				V	
Analog Output Voltage Range				V	
Digital Input Format	Binary Code or 2's Complement Code				

Current Output DAC					
Characteristics	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
Analog Output Maximum Current				mA	
Analog Output Maximum Signal Frequency				MHz	
Reference Voltage				V	
External Resistor for Current Setting (RSET)				Ω	
Pipeline Delay				sec	

— Do you want to Power down mode?

— Do you want to Internal Reference Voltage (BGR)?

— Which do you want to serial input data type or parallel input data type?

HISTORY CARD

Version	Date	Modified Items	Comments
Ver 1..0	00.05.20	Original version published	
Ver 1..1	00.07.20	DC spec TBD (to be determine) adding Scaling factor M=8 → M=128 modify Output voltage level Vmax=1V → Vmax=0.66 modify	
Ver 1.2	00.10.28	I/O pad vss3t_abb → vbb3t_abb	
Ver 1.3	00.11.20		
Ver 1.4	01.06.27	Core specification completion 12bit 300Mhz → 10bit 165MHz changing	
Ver.1.5	01.07.02	Typo correction (There are no spec modification)	
Ver 1.6	01.07.06	Test chip evaluation guide addition	
Ver 1.7	02.02.27	Internal BGR Reference Voltage range modified	
Ver 1.8	02.04.20	Add phantom cell guide	