GENERAL DESCRIPTION

The dac1267x is a CMOS 9Bit D/A converter for general applications. Its maximum conversion rate is 40MSPS and supply voltage is 1.8V single.

An external 0.7V voltage reference(VBIAS) and a single resistor (RSET) control the full-scale output current.

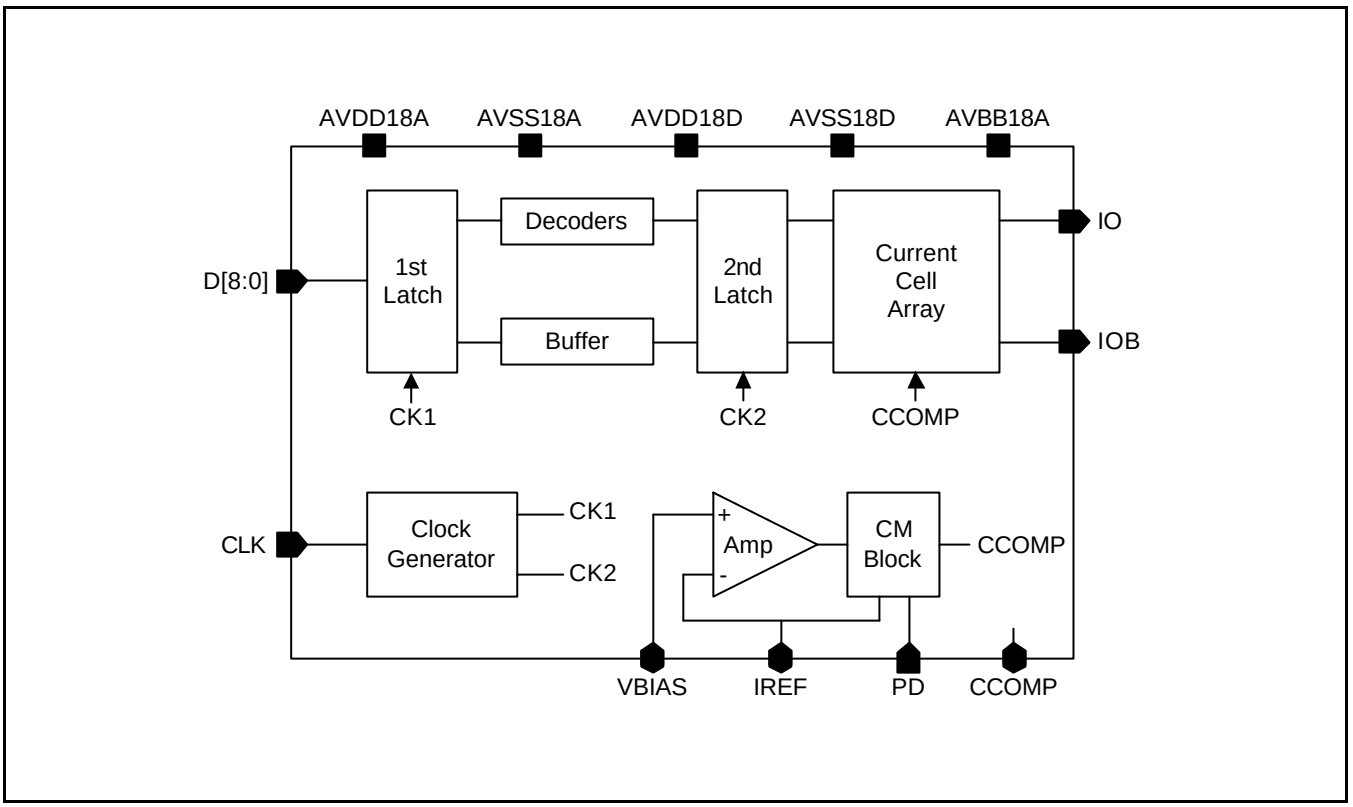
FEATURES

— 40 MSPS pipeline operation
— 1.8V CMOS monolithic construction
— ± 0.3LSB differential linearity error (typical)
— ±1.5LSB integral linearity error (typical)
— External voltage reference
— 9-Bit voltage parallel input

TYPICAL APPLICATIONS

— High Definition Television (HDTV)
— Hard Disk Drive
— High Resolution Color Graphics
— CAE/CAD/CAM

FUNCTIONAL BLOCK DIAGRAM



Ver 2.4 (Apr. 2002)

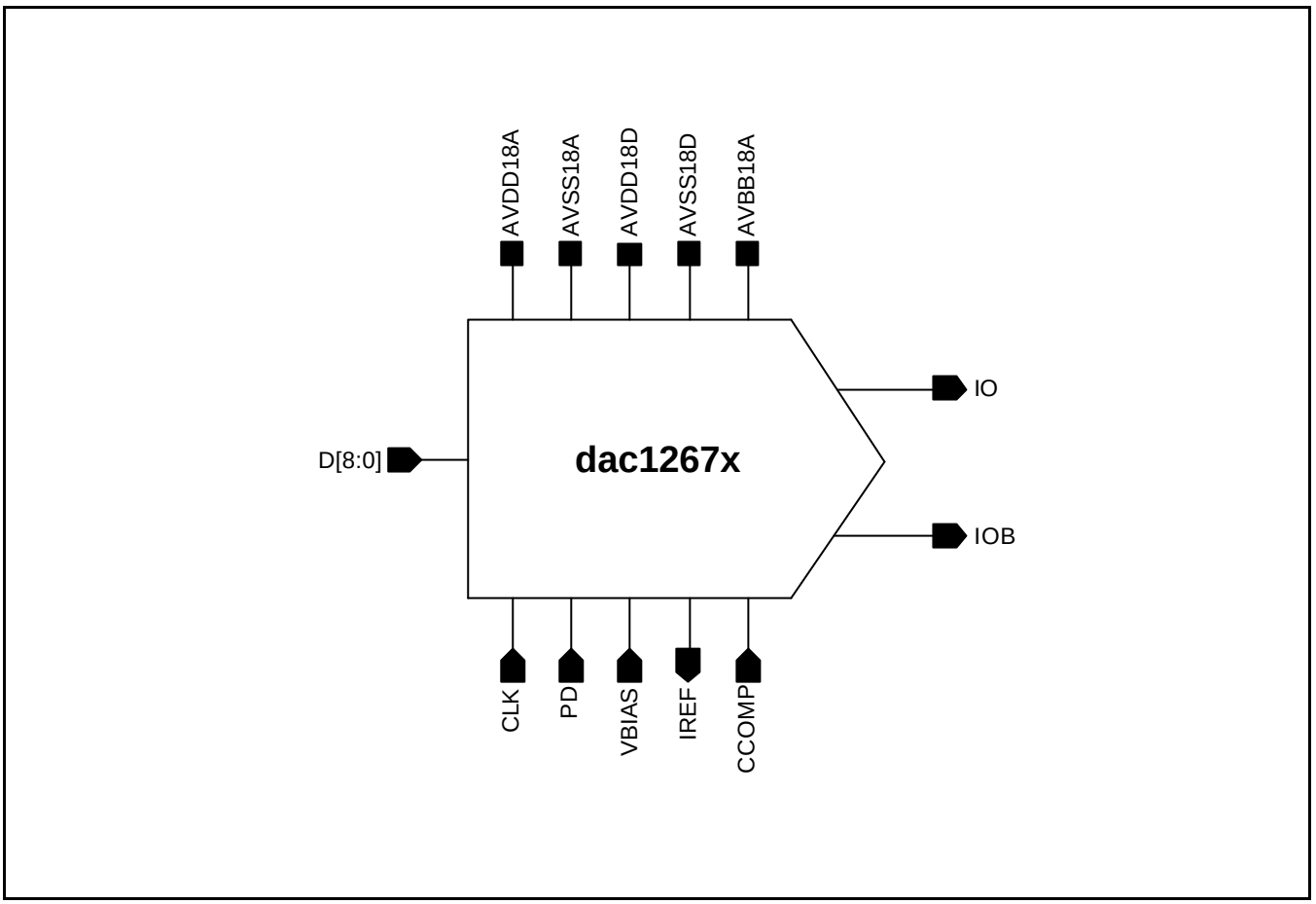
CORE PIN DESCRIPTION

Pin Name	I/O Type	I/O Pad	Pin Description
D[8:0]	DI	picc_abb	Digital Input
CLK	DI	picc_abb	Clock Input
PD	DI	picc_abb	High=power saving standby mode (normally = gnd)
VBIAS	AI	pia_abb	External Bias (0.7V)
IREF	AO	poa_abb	Full Scale Adjust Control
CCOMP	AI	pia_abb	Using Compensation Capacitor
IO	AO	poa_abb	Analog Output (output Range : 0.66Vpp)
IOB	AO	poa_abb	Analog Output (output Range : 0.66Vpp)
AVDD18A	AP	vdd1t_abb	Analog Power
AVSS18A	AG	vss1t_abb	Analog Ground
AVDD18D	DP	vdd1t_abb	Digital Power
AVSS18D	DG	vss1t_abb	Digital Ground
AVBB18A	AG	vbb_abb	Analog Ground (bulk bias)

I/O Type Abbr.

— AI: Analog Input
— DI: Digital Input
— AO: Analog Output
— DO: Digital Output
— AB: Analog Bi-direction
— DB: Digital Bi-direction
— AP: Analog Power
— AG: Analog Ground
— DP: Digital Power
— DG: Digital Ground

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	AVDD18D, AVDD18A	+2.5	V
Digital Input Voltage	Vin	AVSS18D-0.2 to VDD18D+0.2	V
Operating Temperature Range	Topr	-45 to +80	°C
Storage Temperature Range	Tstg	-55 to +150	°C

NOTES:

1. Absolute maximum rating values applied individually while another parameters are within specified operating condition. Function operation under any of these conditions is not implied.
2. Applied voltage must be current limited to specified range.
3. Absolute maximum ratings are value beyond which the device may be damaged permanently. Normal operation is not guaranteed.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage	AVDD18A-AVSS18A AVDD18D-AVSS18D	1.6	1.8	2.0	V
Digital Input Voltage High	VIH	0.8×VDD	–	–	V
Digital Input Voltage Low	VIL	–	–	0.2×VDD	V
Operating Temperature Range	T_{OPR}	0	–	70	°C
Output Load (effective)	RL	150			Ω
Reference Voltage	VBIAS	0.7			V
Clock Cycle Time	Tclk	25	–	–	ns
Clock Pulse Width High	Tpwh	12	–	–	ns
Clock Pulse Width Low	Tpwl	12	–	–	ns
IREF Current	Iref	291.6			uA

NOTES:

1. It is strongly recommended that to avoid power latch-up all the supply pins (AVDD18A, AVDD18D) be driven from the same source.
2. Voltage on any digital pin that goes below AVSS18D (Digital Ground) by less than 0.2V can induce destructive latch-up.

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Resolution	–	–	9	–	Bits
Differential Linearity Error	DLE	–	0.3	±1	LSB
Integral Linearity Error	ILE	–	1.5	±2	LSB
Monotonicity	–	Guaranteed			–
Zero level	Vz	0	–	3	mV
Full Scale	FS	0.55	0.678	0.75	V
Maximum Output Compliance	VOC	0	–	+0.8	V
External Reference Voltage	VBIAS	–	0.7	–	V

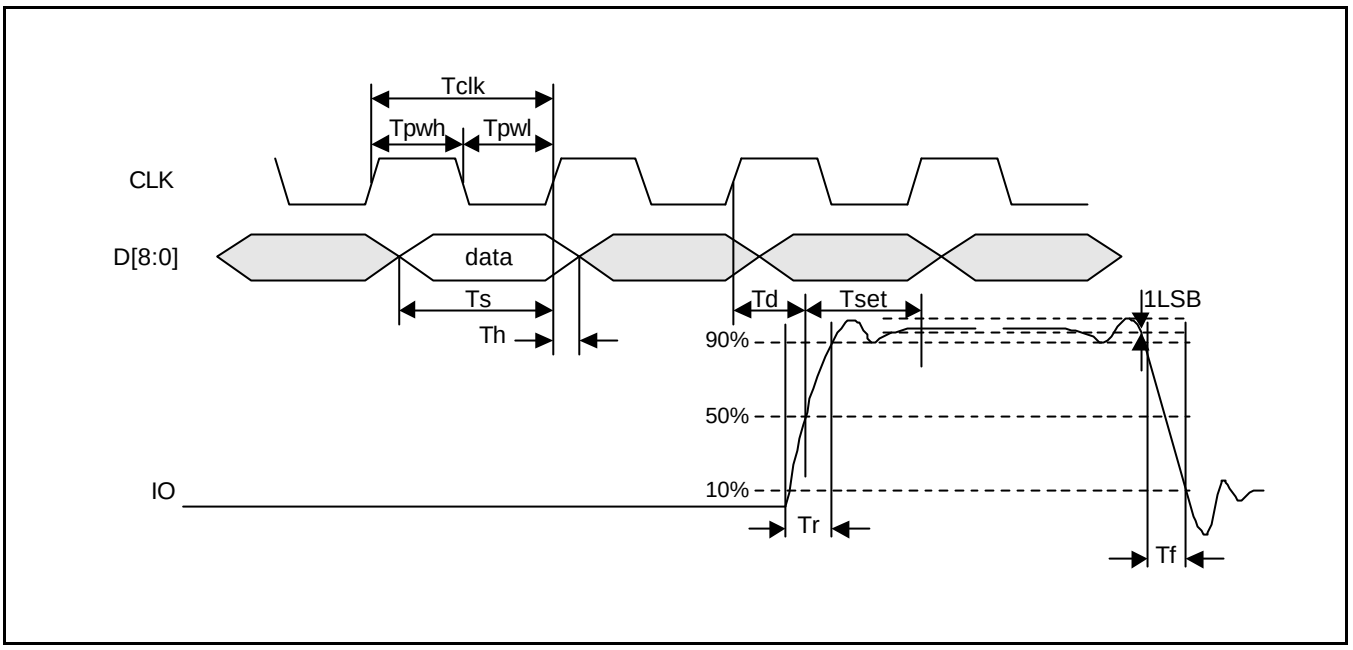
NOTE: Converter Specifications (unless otherwise specified)
AVDD18A=1.8V AVDD18D=1.8V
AVSS18A=GND AVSS18D=GND AVBB18A=GND
Ta=25°C
RL=150Ω, VBIAS=0.7V

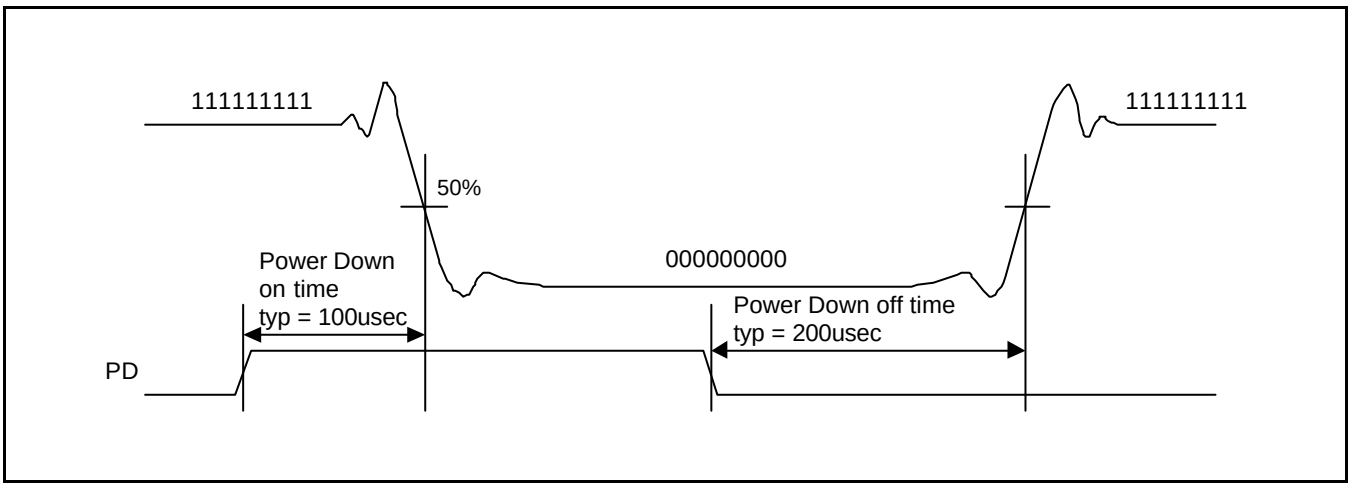
AC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Clock Rate	f_c	–	–	40	MHz
Digital Data Setup Time	Ts	2	–	–	ns
Digital Data Hold Time	Th	2	–	–	ns
Analog Output Delay Time	Td	–	3	–	ns
Analog Output Rise Time	Tr	–	12	15	ns
Analog Output Fall Time	Tf	–	13	15	ns
Analog Output Settling Time	Tset	–	91	115	ns
Clock and Data Feedthrough	FDTHR	-29	-27	-25	dB
Glitch Impulse	GI	90	114	146	pv-sec
Pipeline Delay	Tpd	–	2	–	Clocks
VDD Supply Current	Idd	–	6	8	mA
Spurious Free Dynamic Range	SFDR	-45	-50	-60	dB

NOTES:
1. The above parameters are not tested through the temperature range, but these are guaranteed over the full temperature range.
2. Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Settling time does not include clock and data feedthrough. Glitch impulse include clock and data feedthrough.

TIMING DIAGRAM

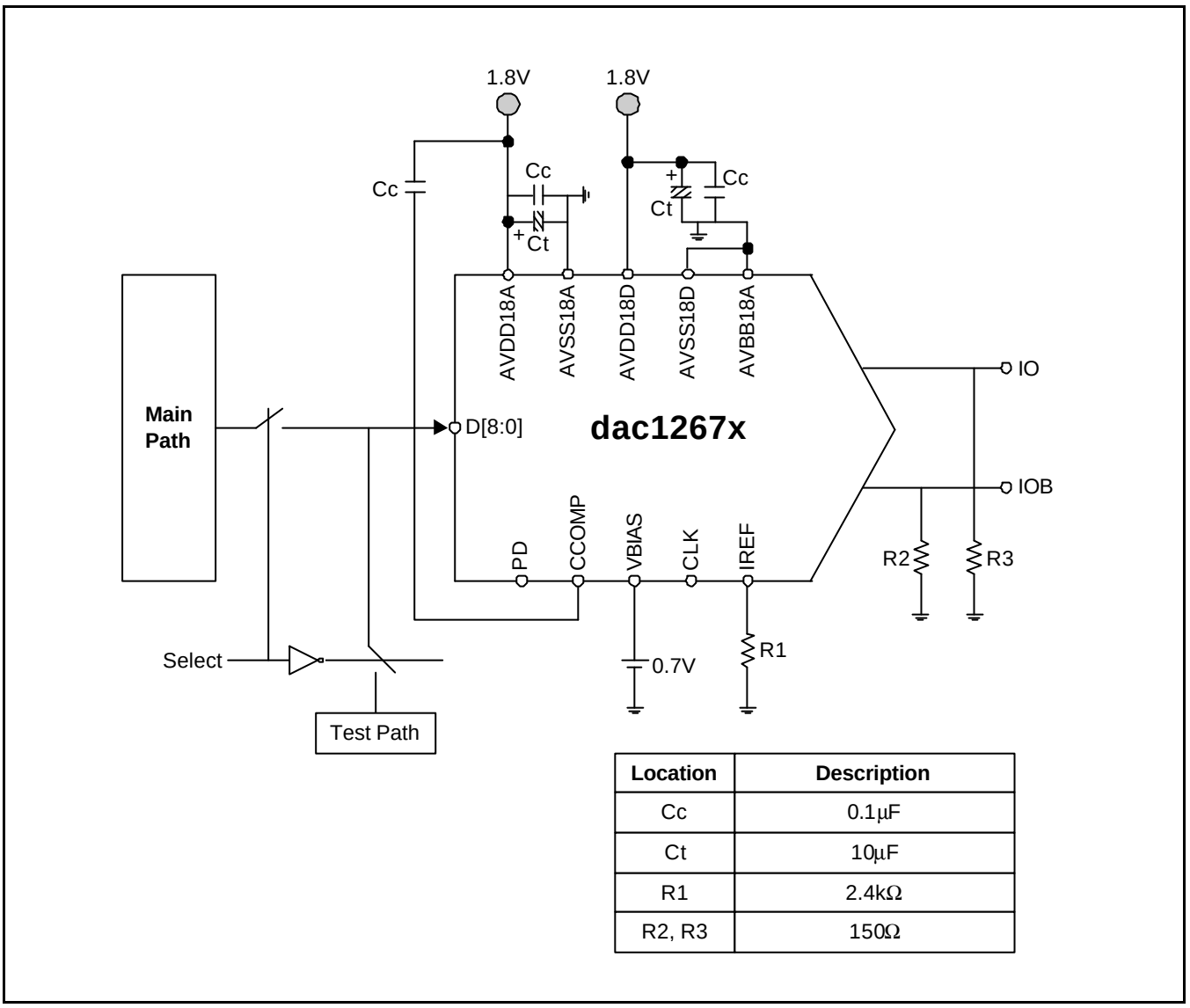




NOTES:

1. Output delay measured from the 50% point of the rising edge of CLK to the full scale trasition.
2. Settling time measured from the 50% point of full scale transition to the output remaining within ±1, ±2LSB.
3. Output rise/fall time measured between the 10% and 90% points of full scale transition.

CORE EVALUATION GUIDE



Location	Description
Cc	0.1μF
Ct	10μF
R1	2.4kΩ
R2, R3	150Ω

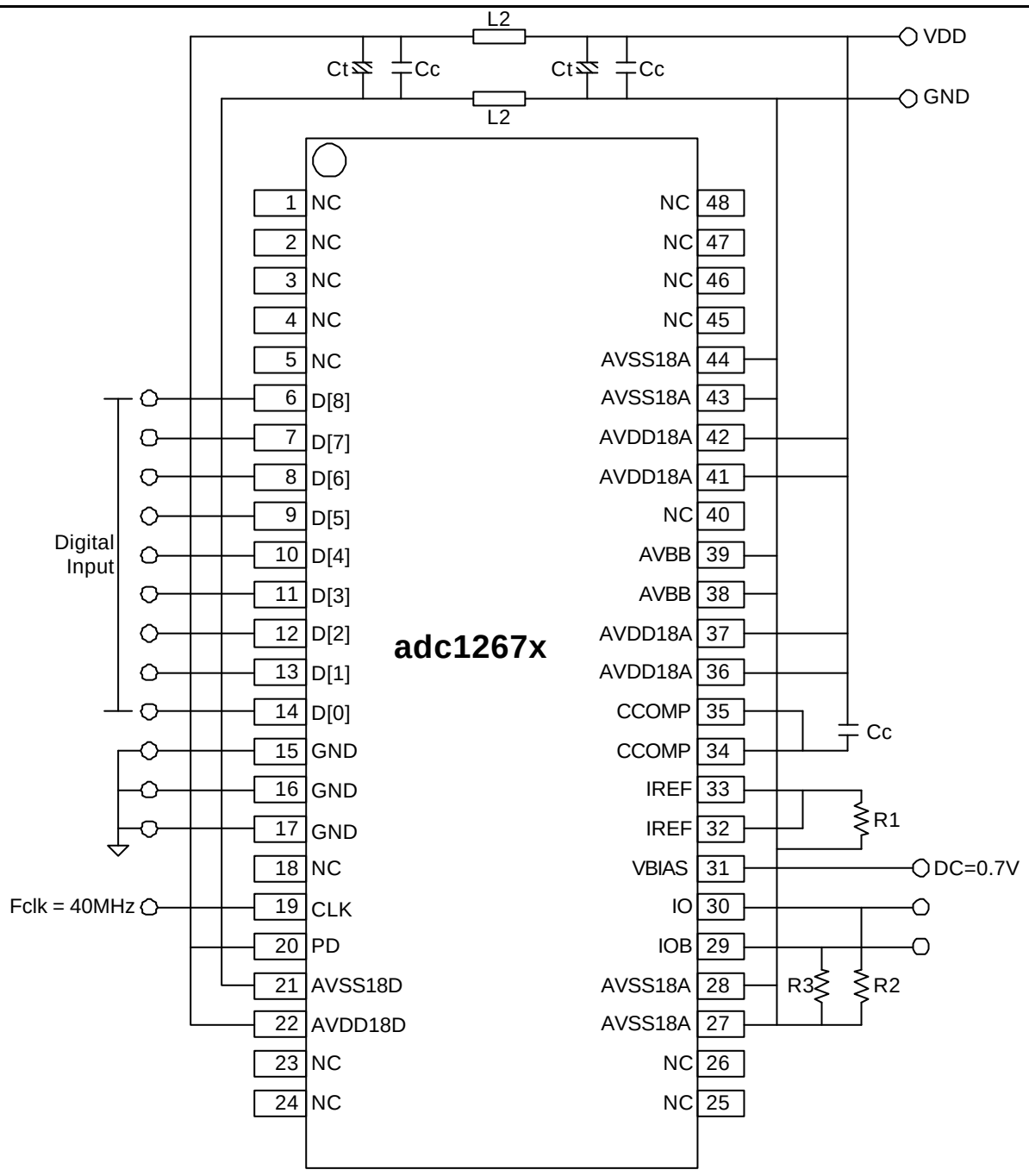
1. Testablitity

Whether you use MUX or the internal logic for testability, it is required to be able to select the values of digital inputs (D[0] – D[8]) See above figure. Only if it is, you can check the main function (Linearity), and output (IO, IOB), VBIAS, IREF and CCOMP pins are reserved for external use.

2. Analysis

The voltage applied to VBIAS is measured at IREF node. And, the voltage value is proportional to the reference current value of resistor which is connected to IREF node. So you can estimate the full scale current value by measuring the voltage, and check the DC characteristics of the OPAMP. For reference, as VREF applied to VBIAS node is given at IREF node, the current flow through RSET is given as VREF/RSET. The full scale current is given as the decimal value equivalent to the digital code.

PACKAGE CONFIGURATION



Location	Description
Ct	10uF Tantalum Capacitor
Cc	0.1uF Ceramic Capacitor
L1-L2	Ferrite Bead (0.1mh)
R1	2.4kΩ
R2, R3	150Ω

PACKAGE PIN DESCRIPTION

Name	Pin No	I/O Type	Pin Description
AVDD18A	36,37,41,42	AP	Analog Power
AVBB18A	38,39	AG	Analog Ground
AVSS18A	27,28,43,44	AG	Analog Ground
D[0] – D[8]	6–14	DI	Digital Input Data
PD	20	DI	Digital Input Data(Low)
AVDD18D	22	DP	Digital Power
AVSS18D	21	DG	Digital Ground
CLK	19	DI	Digital Input Data
IOB	29	AO	Analog Voltage Output This chip was developed for 12bit DAC, but finished to develop with 9bit DAC. When you may want to probe IOB, This chip will have the offset error corresponding to 7/8 LSB.
IO	30	AO	Analog Voltage Output
VBIAS	31	AI	Voltage Reference(0.7V)
IREF	32,33	AO	Analog DC current output Need an termination resistor
CCOMP	34,35	AI	Compensation capacitor
NC	1,2,3,4,5,18,23,24,25, 26,40,45,4647,48	DO	No Connection

BOARD LAYOUT CONSIDERATIONS

1. PC Board Considerations

To minimize Noise On The Power Lines and The Ground Lines, The Digital Inputs Need To Be Shielded and Decoupled. This Trace Length Between Groups of VDD (AVDD18A,AVDD18D) pins should be short as possible so as to minimize inductive ringing.

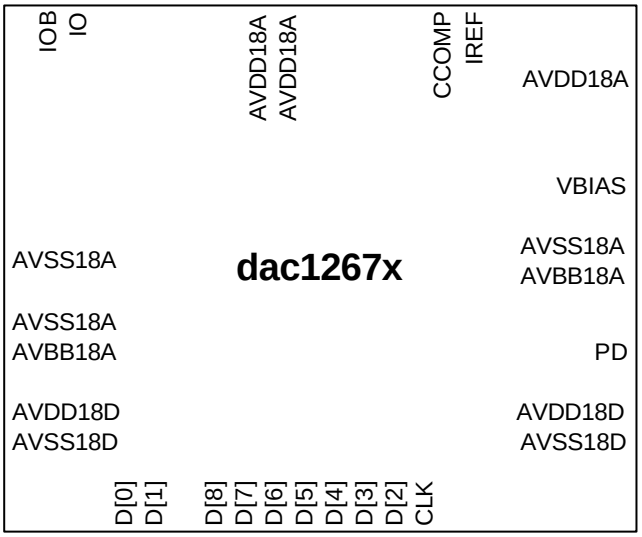
2. Supply Decoupling and Planes

For the decoupling capacitor between the power line and the ground line, a 0.1μF ceramic capacitor is used in parallel with a 10μF tantalum capacitor. The digital power plane (AVDD18D) and analog power plane (AVDD18A) are connected through a ferrite bead, and also the digital ground plane (AVSS18D) and the analog plane (AVSS18A). This ferrite bead should be located within 3inches of the dac1267x.

3. Analog Signal Interconnection

To minimize noise pickup and reflections due to impedance mismatch, the dac1267x should be located as close as possible to the output connector.
The line between DAC output and monitor input should also be regarded as a transmission line. Due to the fact, it can cause problems in transmission line mismatch. As a solution to these problems, the double-termination methods used. By using this, both ends of the termination lines are matched, providing an ideal, non-reflective system.

PHANTOM CELL INFORMATION



Pin Name	Property	Pin Usage	Pin Layout Guide
AVDD18A	AP	External	1. It is recommended that you use thick analog power metal (more than 10um each). When connected to PAD, each path should be kept as short as possible. 2. Digital Power and analog power must be used separately. 3. In Phantom cell in case of many ports of one power name, you must drag the ports individually to PAD in parallel. 4. Customer must use two PADs individually for analog power ports because of PAD's current limitation.
AVSS18A	AG	External	
AVDD18D	DP	External/Internal	
AVSS18D	DG	External/Internal	
AVBB18A	AG	External/Internal	
D[8:0]	DI	External/Internal	1.Digital input Signal lines must have same length to reduce propagation delay.
PD	DI	External/Internal	
IREF	AB	External	1. Analog Bi-direction line must be kept as short as possible. 2. Any other should not across these lines except power metal.
VBIAS	AB	External	
CCOMP	AB	External	
IO	AO	External	1. Analog output line should be kept as short as possible. 2. These lines must have the same metal length because of voltage drop through the metal line.
IOB	AO	External	
CLK	DI	External/Internal	1. Separated from the analog clean signals if possible. 2. Do not exceed the length by 100um.-

FEEDBACK REQUEST

We appreciate your interest in out products. If you have further questions, please specify in the attached form. Thank you very much.

DC/AC Electrical Characteristic					
Characteristics	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
Supply Voltage				V	
Power dissipation				mW	
Resolution				Bits	
Analog Output Voltage				V	
Operating Temperature				°C	
Output Load Capacitor				pF	
Output Load Resistor				Ω	
Integral Non-Linearity Error				LSB	
Differential Non-Linearity Error				LSB	
Maximum Conversion Rate				MHz	

Voltage Output DAC					
Characteristics	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
Reference Voltage TOP BOTTOM				V	
Analog Output Voltage Range				V	
Digital Input Format	Binary Code or 2's Complement Code				

Current Output DAC					
Characteristics	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
Analog Output Maximum Current				mA	
Analog Output Maximum Signal Frequency				MHz	
Reference Voltage				V	
External Resistor for Current Setting (RSET)				Ω	
Pipeline Delay				sec	

— Do you want Power down mode?

— Do you want Internal Reference Voltage (BGR)?

— Which do you want between serial input data type and parallel input data type?

— Do you need 3.3V and 1.8V power supply in your system?

HISTORY CARD

Version	Date	Modified Items	Comments
Ver 2.0	01.06.21	Modified Version DAC1267X was developed for 12bit 40MHz DAC, but test result didn't meet 12bit performance. So, the specifications of DAC1267X are modified to 9bit 40MHz DAC and datasheet is also modified.	
Ver 2.1	01.07.04	Modified Version Typo and wrong information are corrected.	
Ver 2.2	01.07.05	Typo correction.	
Ver 2.3	01.07.09	Modified Version Newly Updated	
Ver 2.4	02.04.22	Phantom Cell information update	