

GENERAL DESCRIPTION

The dac1264x_ra is a CMOS 10Bit D/A converter for general application. This digital to analog converter has a R-string structure.

Its settling time is 400ns (Typical value).

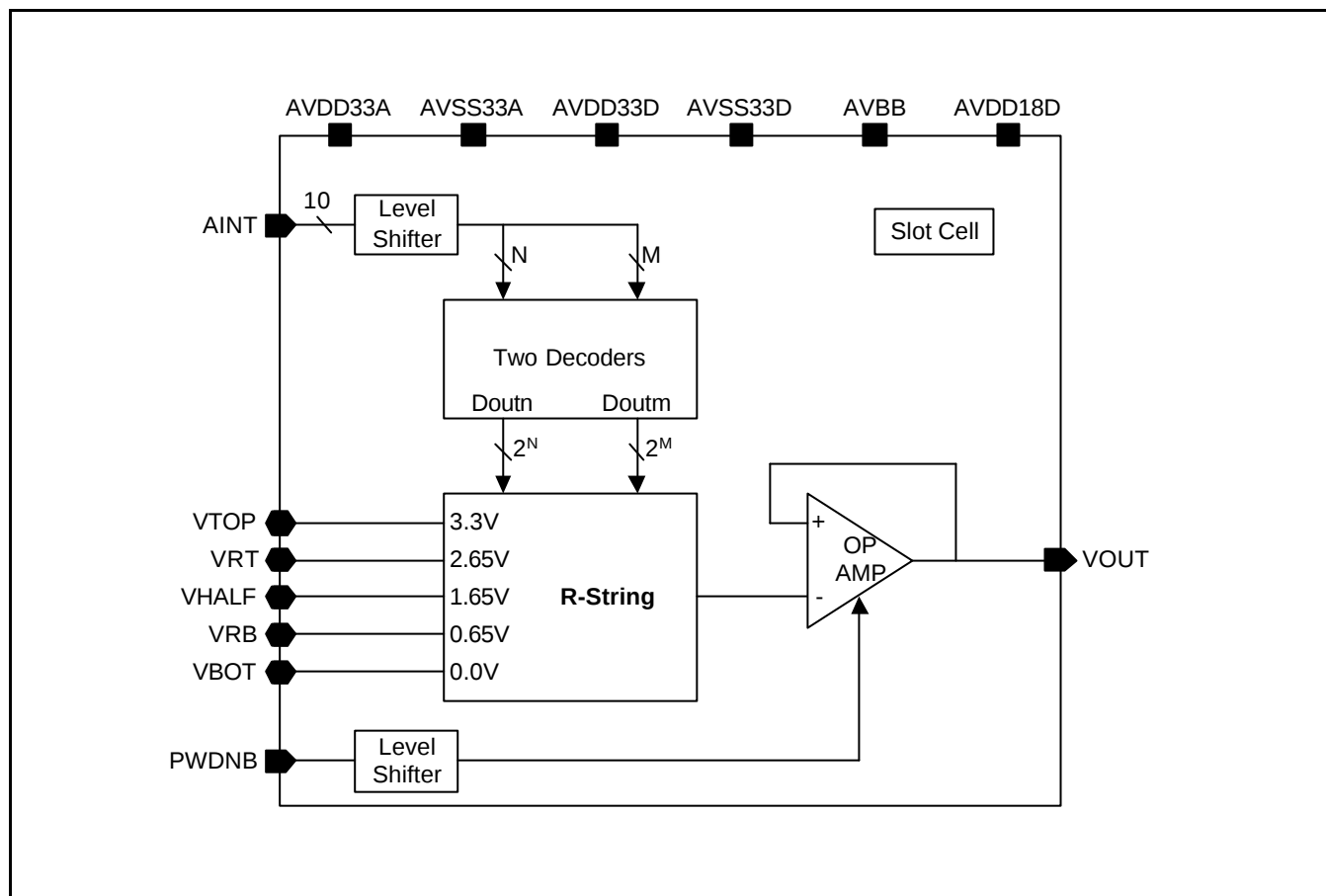
FEATURES

- Resolution : 10Bit
- Differential Linearity Error : ± 1.0 LSB
- Integral Linearity Error : ± 2.0 LSB
- Settling Time : 400ns
- Low Power Consumption : 3.0mA
- Power Down Mode
- Operation Temperature Range : 0°C – 70°C
- Power Supply : 3.3V Single
 : 1.8V (for Digital Input)

TYPICAL APPLICATIONS

- CD/DVD Servo
- Motor Control Systems
- General Applications

FUNCTIONAL BLOCK DIAGRAM



Ver 1.7 (March 2003)

No responsibility is assumed by SEC for its use nor for any infringements of patents or other rights of third parties that may result from its use. The content of this datasheet is subject to change without any notice.

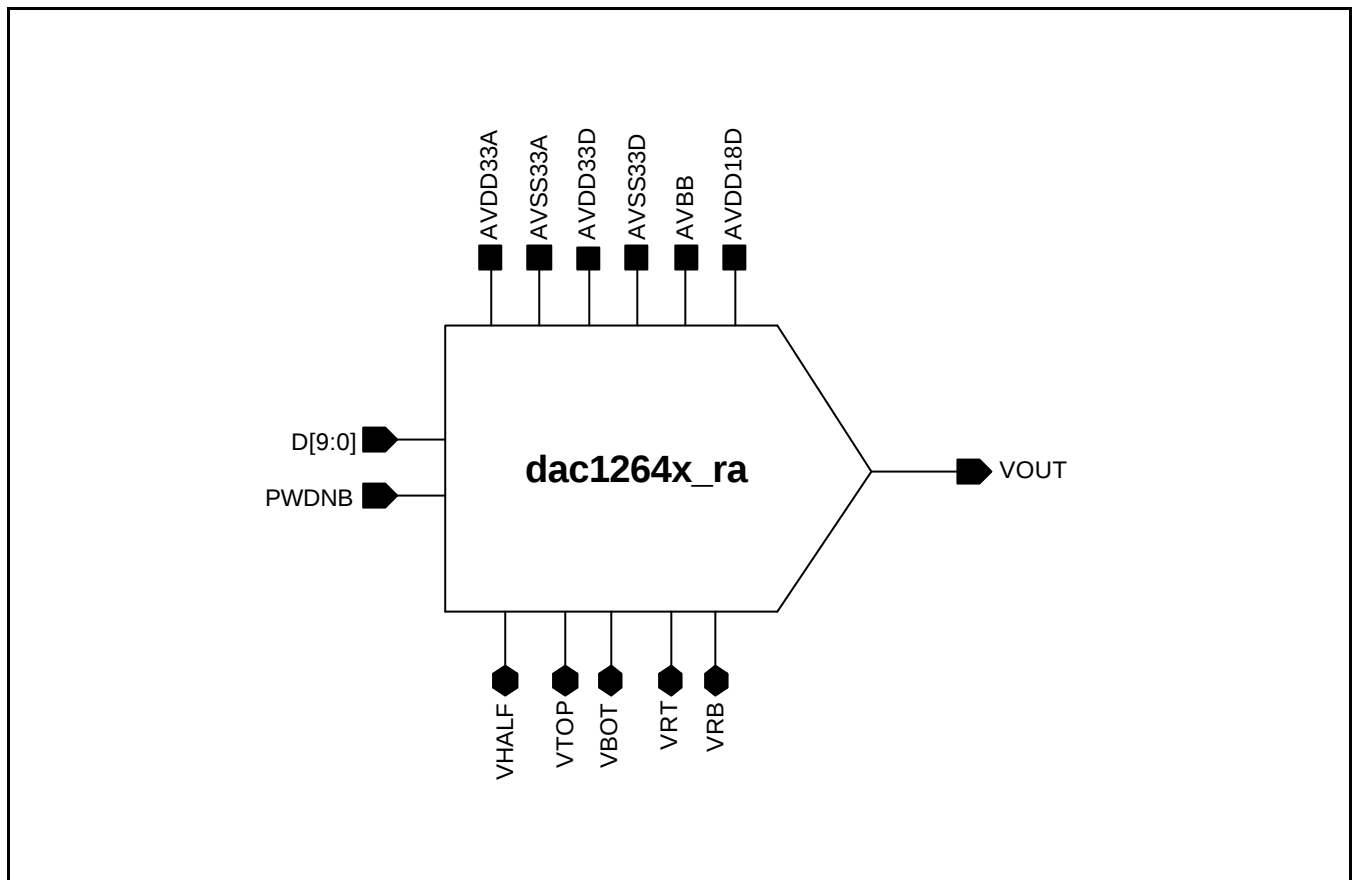
CORE PIN DESCRIPTION

Pin Name	I/O Type	I/O Pad	Pin Description
D[9:0]	DI	picc_abb	Digital Input Data (10bit : 1.8V) D[9] : MSB , D[0] : LSB
PWDNB	DI	picc_abb	Power Down (Active Low : 1.8V)
VHALF	AB	phia_abb	External Voltage Reference (1.65V)
VTOP	AB	phia_abb	Voltage Reference Top (3.3V)
VBOT	AB	phia_abb	Voltage Reference Bottom (0.0V)
VRT	AB	phia_abb	Internal Voltage Reference Top (2.65V)
VRB	AB	phia_abb	Internal Voltage Reference Bottom (0.65V)
VOUT	AO	phoa_abb	Analog Voltage Output
AVDD33D	AP	vdd3t_abb	Analog Power (+3.3V)
AVSS33D	AG	vss3t_abb	Analog Ground (0.0V)
AVDD33A	DP	vdd3t_abb	Digital Power (+3.3V)
AVSS33A	DG	vss3t_abb	Digital Ground (0.0V)
AVBB	AG	vbb3t_abb	Analog Sub Bias (0.0V)
AVDD18D	DP	vdd1t_abb	Digital Power (+1.8V)

I/O Type Abbr.

- AI: Analog Input
- DI: Digital Input
- AO: Analog Output
- DO: Digital Output
- AB: Analog Bi-direction
- DB: Digital Bi-direction
- AP: Analog Power
- AG: Analog Ground
- DP: Digital Power
- DG: Digital Ground

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	VDD (AVDD33A,AVDD33D)	4.5	V
Analog Output Voltage	VOUT	AVSS33A to AVDD33A	V
Digital Input Voltage	D[9:0]	AVSS33D to AVDD18D	V
Reference Voltage	VRT VRB	AVDD33A AVSS33A	V
Operating Temperature Range	Topr	0 to 70	°C

NOTES:

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS (AVSS33A or AVSS33D or AVBB) unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	AVDD33A - AVSS33A AVDD33D - AVSS33D	3.15	3.3	3.45	V
	AVDD18D - AVSS33D	1.65	1.8	1.95	V
Supply Voltage Difference	AVDD33A - AVDD33D	-0.1	0.0	0.1	V
Reference Voltage	VRT	–	2.65	3.3	V
	VRB	0.0	0.65	–	V
Digital Input 'Low' Voltage	VIL	–	–	0.3×VDD	V
Digital Input 'High' Voltage	VIH	0.7×VDD	–	–	V
Operating Temperature	Topr	0	–	70	°C

NOTES:

1. It is strongly recommended that to avoid power latch-up all the supply pins(AVDD33A,AVDD33D) be driven from the same source.
2. VDD → AVDD18D

DC ELECTRICAL CHARACTERISTICS

(Converter Specifications: AVDD33D=AVDD33A=3.3V, AVSS33D=AVSS33A=AVBB=0V, AVDD18D=1.8V, PWDNB=High, Top=25°C, VRT=2.65V, VRB=0.65V unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Resolution	Bit	–	10	–	Bits	–
Differential Linearity Error	DLE	-1.0	±0.2	+1.0	LSB	–
Integral Linearity Error	ILE	-2.5	±1.6	+2.5	LSB	–
Zero Scale Error ⁽¹⁾	V _{ZSE}	-15	10	+15	mV	V _{TOP} =3.3V, VRB=0.0V (VRT and VRB are floated.)
Full Scale Voltage Error ⁽²⁾	V _{FSE}	-15	10	+15	mV	
Maximum Output Voltage	V _{O_MAX}	2.633	2.648	2.663	V	V _{O_MAX} = V _{OUT} (D[9:0]=High)
LSB Size	V _{LSB}	1.93	1.953	1.97	mV	V _{LSB} = (V _{O_MAX} - V _{OUT} (D[9:0]=Low)) / 1023

NOTES:

- V_{ZSE} = V_{OUT}(D[9:0] = Low) - VRB
- V_{FSE} = V_{OUT}(D[9:0] = High) - {(VRT-VRB) × 1023/1024 + VRB}

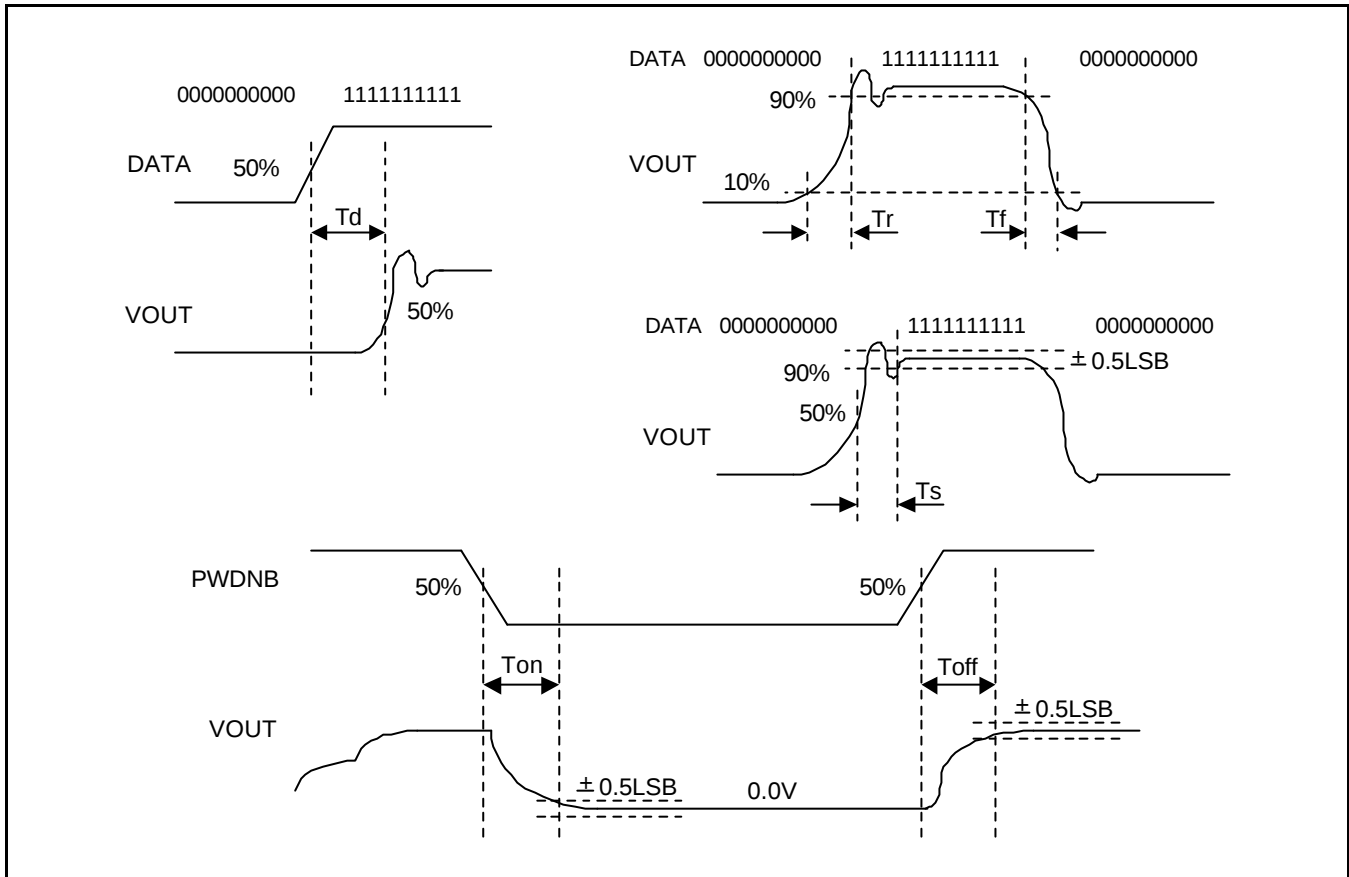
AC ELECTRICAL CHARACTERISTICS

(Converter Specifications : AVDD33D=AVDD33A=3.3V, AVSS33D=AVSS33A=AVBB=0V, AVDD18D=1.8V, load cap=25pF load resistance=5kΩ, Top=25°C, VRT=2.65V, VRB=0.65V unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Supply Current (Average Current)	I _{VDD1}	2	3	4	mA	I _{VDD1} = I _{AVDD33A} + I _{AVDD33D} Data Input: All Low or All High
Supply Current (Power Down Mode)	I _{VDD2}	–	–	10	µA	I _{VDD2} = I _{AVDD33A} + I _{AVDD33D} Data Rate = 2MHz PWDNB=LOW
Reference Current	I _{VRT}	–	0.75	–	mA	
Analog Output Delay	T _d	35	50	80	ns	Data Rate = 2MHz Data : All LOW → All HIGH
Analog Output Rise Time	T _r	40	60	100	ns	Data Rate = 2MHz Data : All LOW → All HIGH
Analog Output Fall Time	T _f	65	103	176	ns	Data Rate = 2MHz Data : All HIGH → All LOW
Analog Output Settling Time	T _s	360	400	420	ns	Data Rate = 2MHz Data : All LOW ® All HIGH
Power Down On Time	T _{on}	–	30	–	ns	PWDNB : HIGH → LOW
Power Down Off Time	T _{off}	–	300	–	ns	PWDNB : LOW → HIGH
Glitch Energy	GLE	-0.1		0.1	nsV	Data Rate = 2MHz Data : 0111111111 → 1111111111
Signal-to-Noise and	SNDR	-48	-56	-58	dB	Data Rate = 2MHz

Distortion Ratio						Output Frequency (fout) = 50kHz
------------------	--	--	--	--	--	---------------------------------

TIMING DIAGRAM



NOTES:

1. Output delay measured from the 50% point of the rising edge of input data to the full scale transition.
2. Settling time measured from the 50% point of full scale transition to the output remaining within $\pm 1/2$ LSB.
3. Output rise/fall time measured between the 10% and 90% points of full scale transition.

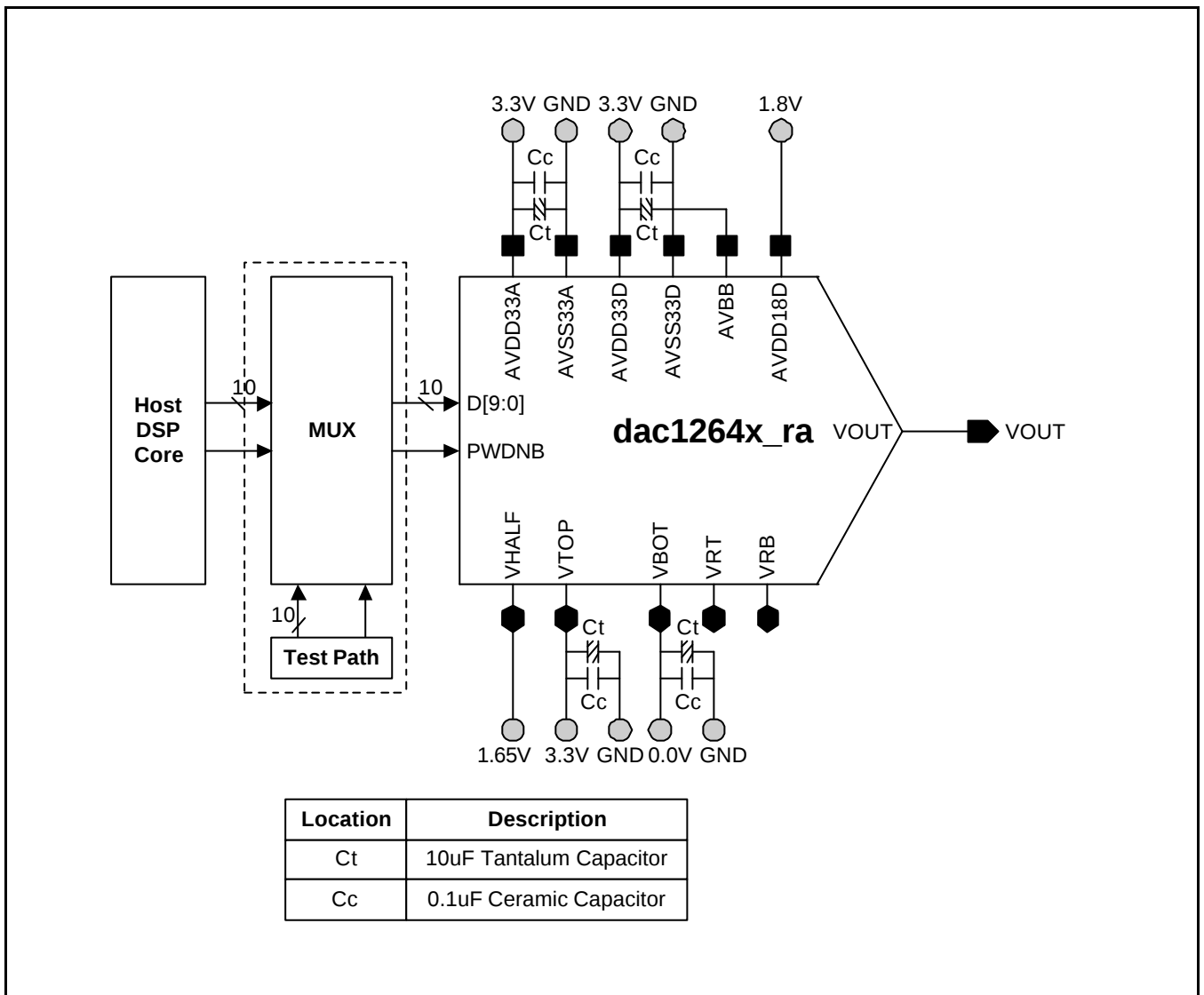
FUNCTIONAL DESCRIPTION

1. The dac1264x_ra has a 10bit R-string block, two decoders, and an OP amp.
2. The digital outputs of two decoders decide the voltage level of R-string block.

$$V_{R\text{string}} = \frac{V_{RT}-V_{RB}}{2^{10}} \sum_{n=0}^9 (2^n \times D[n]) + V_{RB}$$

3. The voltages of VRT and VRB are internally generated by resistor strings.
($V_{TOP} = 3.3\text{V}$, $V_{BOT} = 0.0\text{V}$ then $V_{RT} = 2.65\text{V}$, $V_{RB} = 0.65\text{V}$)
For more accurate operations, you had better connect VRT and VRB with voltage sources instead of connecting VTOP and VBOT with voltage sources. ($V_{RT} = 2.65\text{V}$, $V_{RB} = 0.65\text{V}$)
4. The VOUT pin is dependent of digital input values.
5. Power Down Mode reduces only analog currents ($I_{AVDD33A}$) and reference current (I_{VRT}) is always dissipated.

CORE EVALUATION GUIDE



TESTABILITY

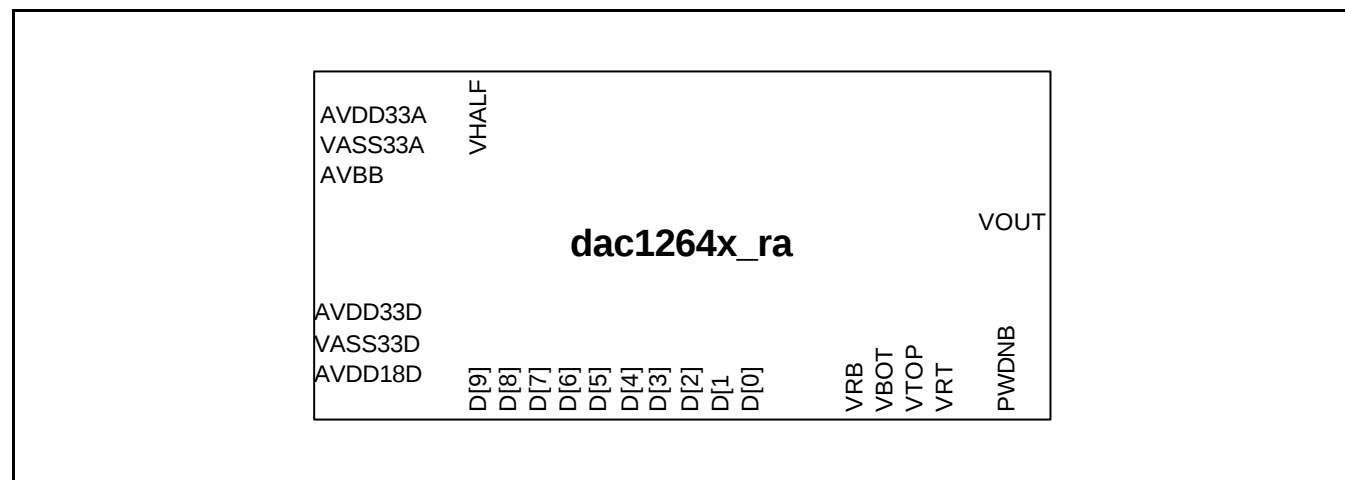
Whether you use MUX or the internal logic for testability, it is required to be able to select values of digital inputs (D[9:0]).

See above figure. Only if it is, you can check the main function. (Linearity)

For more accurate operations, you had better connect VRT and VRB with voltage sources instead of connecting VTOP and VBOT with voltage sources.

(VRT = 2.65V , VRB = 0.65V)

PHANTOM CELL INFORMATION



Pin Name	Property	Pin Usage	Pin Layout Guide
D[9:0]	DI	Internal/External	1. Digital Input Signal lines must have same length to reduce propagation delay.
PWDNB	DI	Internal/External	
VRT	AB	Internal/External	1. Voltage reference lines (VRT/VRB and VTOP/VBOT) must be wide metal to reduce voltage drop of metal lines. 2. If you use VRT and VRB, VTOP and VBOT may be disconnected and vice versa. 3. VOUT signal should not be crossed by any signals and should not run next to digital signals to minimize capacitive coupling between the two signals.
VRB	AB	Internal/External	
VTOP	AB	External	
VBOT	AB	External	
VOUT	AO	Internal/External	1. It is recommended that you use thick analog power metal. When connected to PAD, the path should be kept as short as possible. 2. Digital power and analog power are separately used.
AVDD33A	AP	External	
AVSS33A	AG	External	
AVDD33D	DP	External	
AVSS33D	DG	External	
AVBB	AG	External	
AVDD18D	DP	External	

NOTES:

- When the core block is connected to other blocks, it must be double guard-ring using N-well and P+ active to remove the substrate and coupling noise. In that case, the power metal should be connected to PAD directly.
- The Bulk power is used to reduce the influence of substrate noise.

FEEDBACK REQUEST

We appreciate your interest in our products. If you have further questions, please specify in the attached form. Thank you very much.

DC / AC Electrical Characteristic					
Characteristics	Min	Typ	Max	Unit	Remarks
Supply Voltage				V	
Power dissipation				mW	
Resolution				Bits	
Analog Output Voltage				V	
Operating Temperature				°C	
Output Load Capacitor				pF	
Output Load Resistor				kΩ	
Integral Non-Linearity Error				LSB	
Differential Non-Linearity Error				LSB	
Maximum Conversion Rate				MHz	

Voltage Output DAC					
Characteristics	Min	Typ	Max	Unit	Remarks
Reference Voltage TOP BOTTOM				V	
Analog Output Voltage Range				V	
Digital Input Format	Binary Code or 2's Complement Code				

Current Output DAC					
Characteristics	Min	Typ	Max	Unit	Remarks
Analog Output Maximum Current				mA	
Analog Output Maximum Signal Frequency				kHz	
Reference Voltage				V	
External Resistor for Current Setting(RSET)				kΩ	
Pipeline Delay				sec	

- Do you want to Power down mode?
- Do you want to Internal Reference Voltage(BGR)?
- Which do you want to serial input data type or parallel input data type?
- Do you need 3.3V and 5V power supply in your system?

HISTORY CARD

Version	Date	Modified Items	Comments
Ver 1.0	00.09	Preliminary Version	
Ver 1.1	01.03.15	Page 1 : block diagram is modified (AVSS33A → AVSS33D)	
Ver 1.2	01.03.28	Version Updated page 8 : °C → kΩ (Output Load Resistor)	
Ver 1.3	01.04.12	Version Updated page 8 : Interl → Internal	
Ver 1.4	01.10.05	Version Updated 1.8V pin for digital input is added. (block diagram, symbol, spec..etc) Core layout guide is added.	
Ver 1.5	01.11.02	Version Updated page 7 : Layout guide is modified.	
Ver 1.6	02.05.13	Version Updated page 3 : Absolute Maximum Rating is modified. page 4 : Test result is added. page 5 : Functional description is modified. page 6 : Diagram is modified. page 8 : Diagram is modified. page 9 : Question is modified.	
Ver1.7	03.03.06	Version Updated Page 1 : Application is modified. Page 4 : 111111111 → 1000000000 Page 8 : Diagram is modified.	