DR8052EX

8-bit RISC Extended Microcontroller

ver 2.00

OVERVIEW

DR8052EX soft core is binary-compatible with the industry standard 8052 8-bit microcontroller and can achieve a performance of up to **50 million** instructions per second in today's integrated circuit technologies. DR8052EX has RISC architecture that is 6.7 time faster compare to original implementation.

KEY FEATURES

- Software compatible with industry standard 8052
- RISC architecture
- 6.7 times faster than the original implementation
- 4-clk periods multiplication
- 5-clk periods division
- Up to 16M bytes of external standard Data Memory
- Up to 256 bytes of internal dual port Data Memory
- Up to 64K bytes of Program Memory
- User programmable RAMWE and RAMRD pulses between 1 to 8 clock periods
- De-multiplexed Address/Data Bus to allow easy connection to memory
- Over 16 times data transfer faster than the original implementation
- Three 16-bit timer/counters
- Eight Additional interrupts
- Two full-duplex serial ports
- I2C bus controller
- Two data pointers (DPTR1 & DPTR2)
- Support for External SFRs
- Fully synthesizable, static synchronous design with no internal tri-states
- 670 MHz virtual clock frequency compare to original implementation (over 100 MHz in a typical 0.25u technological process)

DELIVERABLES

- VHDL, Verilog source code
- VITAL simulation model
- HDL test bench
- Synthesis scripts
- Technical documentation
- Technical support

DESIGN FEATURES

✓ DATA MEMORY:

The DR8052EX can address Internal Data Memory of up to 256 bytes, and up to 16M bytes of external Data RAM via the function interconnect signals. The Internal Data Memory can be implemented as Single-Port synchronous or asynchronous RAM.

✓ EXTERNAL SPECIAL FUNCTION REGISTERS:

Up to 99 External Special Function Registers (ESFRs) may be added to the DR8052EX design. ESFRs are memory mapped into Direct Memory between addresses 80 hex and FF hex in the same manner as core SFRs and may occupy any address that is not occupied by a core SFR.

✓ STRETCH MEMORY CYCLE REGISTER:

Allows applications software to adjust to different external RAM speeds (XRAMWR and XRAMRD pulse between 1 – 8 clock cycles).

✓ EXTERNAL RAM:

Allows applications software to access up to 16 MB of external data memory. Extra DPP(*Data Page Pointer*) register is used for segments swapping.

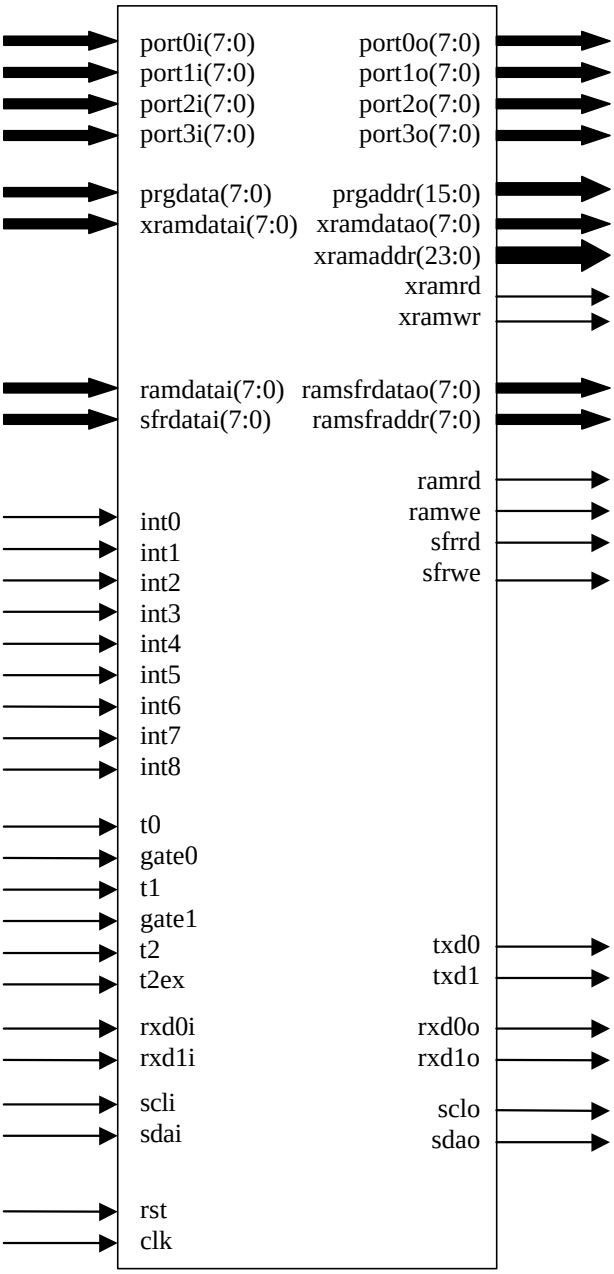
✓ ADDITIONAL INTERRUPTS :

Four additional low level sensitive interrupts (INT2-INT5), and three additional falling edge sensitive interrupts (INT6-INT8).

PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
port0i[7:0]	input	Port 0 input
port1i[7:0]	input	Port 1 input
port2i[7:0]	input	Port 2 input
port3i[7:0]	input	Port 3 input
prgdata[7:0]	input	Data bus from program memory
xramdatai[7:0]	input	Data bus from ext. data memory
ramdati[7:0]	input	Data bus from int. data memory
sfrdatai[7:0]	input	Data bus from user SFR's
int0	input	External interrupt 0
int1	input	External interrupt 1
int2	input	External interrupt 2
int3	input	External interrupt 3
int4	input	External interrupt 4
int5	input	External interrupt 5
int6	input	External interrupt 6
int7	input	External interrupt 7
int8	input	External interrupt 8
t0	input	Timer 0 input
t1	input	Timer 1 input
t2	input	Timer 2 input
gate0	input	Timer 0 gate input
gate1	input	Timer 1 gate input
t2ex	input	Timer 2 trigger input
rxd0i	input	Serial 0 receiver input
rxd1i	input	Serial 1 receiver input
scli	input	I2C bus clock line input
sdai	input	I2C bus data line input
port0o[7:0]	output	Port 0 output
port1o[7:0]	output	Port 1 output
port2o[7:0]	output	Port 2 output
port3o[7:0]	output	Port 3 output
prgaddr[15:0]	output	Program memory address bus
xramaddr[23:0]	output	External data memory address bus
xramdatao[7:0]	output	Data bus for external data memory
xramwr	output	External data memory write
xramrd	output	External data memory read
ramsfraddr[7:0]	output	RAM and SFR's address bus
ramsfrdatao[7:0]	output	Data bus for internal data memory
ramwe	output	Internal data memory write enable
ramrd	output	Internal data memory read
sfrwe	output	User SFR's write enable
sfrrd	output	User SFR's read
rxd0o	output	Serial 0 receiver output
rxd1o	output	Serial 1 receiver output
txd0	output	Serial 0 transmitter output
txd1	output	Serial 1 transmitter output
sclo	output	I2C bus clock line output
sdao	output	I2C bus data line output

SYMBOL



PERFORMANCE

The following table gives a survey about the DR8052EX performance in ALTERA® devices after Place & Route (all key features have been included):

a) FLEX™ 10K100E-1

Area	-	2832 LC + 1EAB
System clock f_{max}	-	49 MHz

b) APEX™ 10K100E-1

Area	-	2930 LC
System clock f_{max}	-	48 MHz

c) ACEX™ 1K100-1

Area	-	2892 LC + 1EAB
System clock f_{max}	-	47 MHz

MODIFICATIONS

For any modification or special request contact to DCD.

Headquarter:

Wroclawska 94

41-902 Bytom

POLAND

e-mail: info@dcd.com.pl

tel. : +48 32 282 82 66

fax : +48 32 282 74 37

Field Office:

Texas Research Park

14815 Omicron Dr. suite 100

San Antonio, TX 78245

USA

e-mail: info-us@dcd.com.pl

tel. : +1 210 667 0185

fax : +1 210 667 0635

Distributor:

MTC-Micro Tech Consulting GmbH

AM Weidegrund 10

D-82194 Gröbenzell

Germany

e-mail : MTCinfo@mtc.de

tel. : +49 8142 5961-0

fax : +49 8142 5961-44