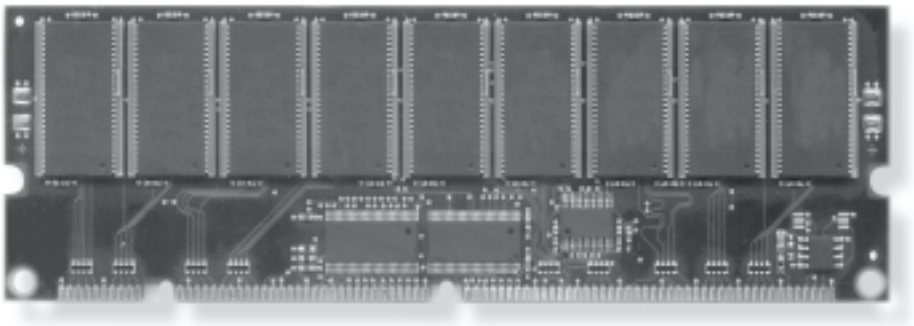
DTM60180

256MB-32M x 72, 168-Pin Registered PC133 SDRAM DIMMS



Identification

DTM60180:32Mx72

Performance range

133MHz (7.5ns @ CL=2)

Features

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- MRS cycle with address key programs Latency (Access from column address) Burst length (1, 2, 4 & 8 page) Data scramble (Sequential & Interleave)
- Serial presence detect with EEPROM
- 168-pin PC133 DIMM double-sided assembly 5.250" wide by 1.70" high

Description

The Dataram DTM60180 is registered 32Mx72 Synchronous Dynamic RAM high density memory modules.The DTM60180 consists of eighteen monolithic 32Mx4bit SDRAMS in TSOP-II 400Mil packages. Three 18-bit Drive ICs for input control, one PLL for clock, and one 2K EEPROM for Serial Presence Detect are also installed on a 168-pin glass-epoxy substrate. Sychronous design allows for precise cycle control with the use of a system clock. The DTM60180 isDual in-line Memory Modules intended for mounting into168-pin connector sockets. Each module is addressed by 12 row lines, 10 column ines, 2 bank addresses and is organized as two physical bank.

Pin configurations

Front side						Back side					
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	Vdd	87	DQ33	115	RAS	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	*Vref	90	Vdd	118	A3	146	*Vref
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	Vdd	101	DQ45	129	*CS3	157	Vdd
18	Vdd	46	DQM2	74	DQ28	102	Vdd	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vdd	77	DQ31	105	CB4	133	Vdd	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	Vdd	54	Vss	82	**SDA	110	Vdd	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd

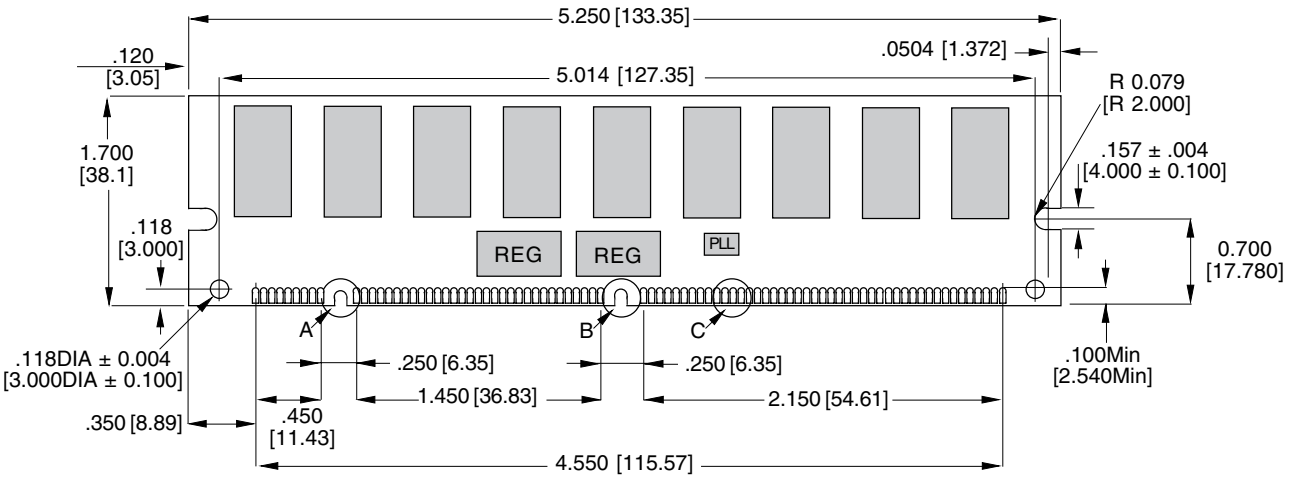
Pin names

Pin name	Function
A0-A11	Address input (Multiplexed)
BA0-BA1	Select bank
DQ0-DQ63	Data input/output
CB0-CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0-CS3	Chip select input
RAS	Row address strobe
CAS	Colume address strobe
WE	Write enable
DQM0-DQM7	DQM
Vdd	Power supply (3.3V)
Vss	Ground
Vref	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

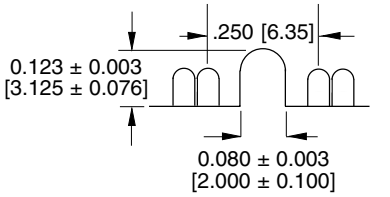
* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.

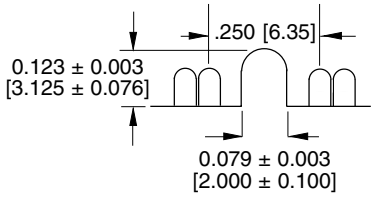
Front view



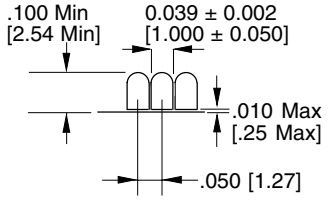
Detail A



Detail B

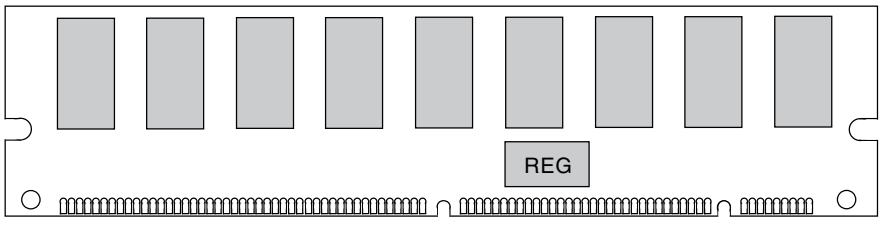


Detail C

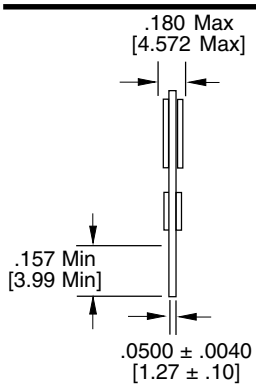


Units: Inches (Millimeters)

Back view



Side view



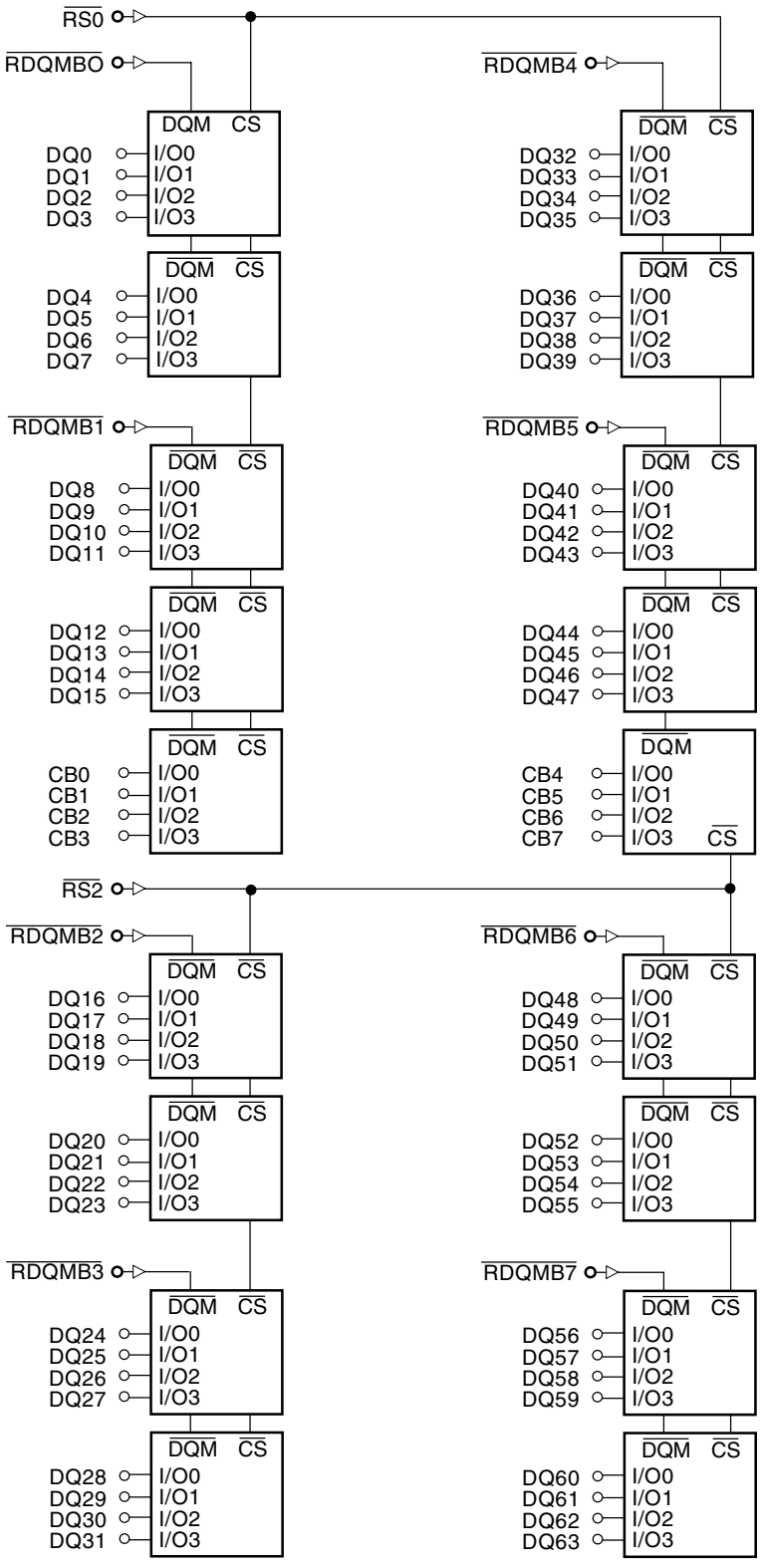
Notes

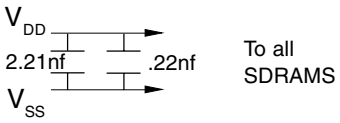
Tolerances on all dimensions except where otherwise indicated are ±.005 [.13].

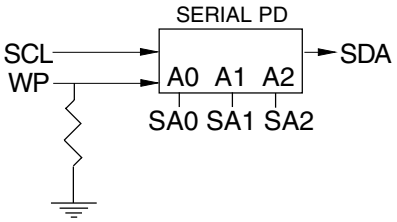
The used device is 32Mx4 SDRAM, TSOP

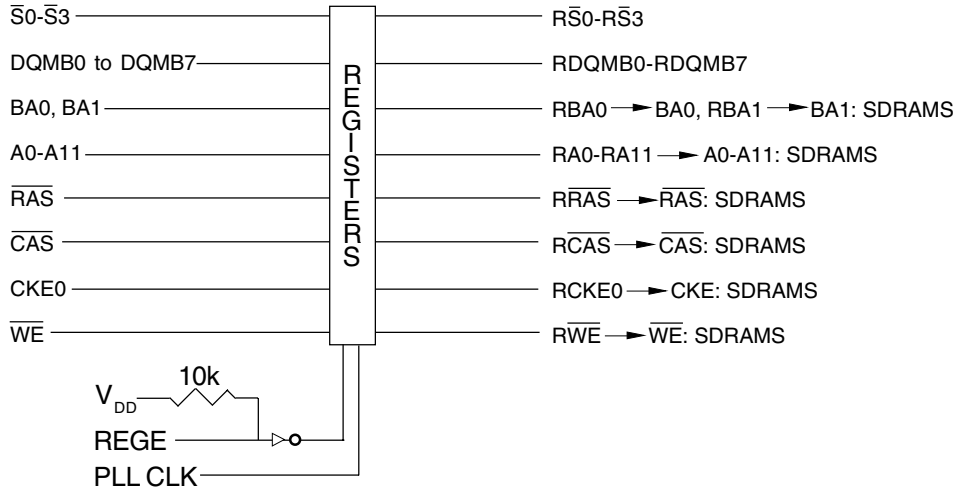
All dimensions are expressed: inches [millimeters].

DIAGRAM OF THE DTM60180




V_{DD}
2.21nf
.22nf
V_{SS}
To all
SDRAMS


SERIAL PD
SCL
WP
A0 A1 A2
SDA
SA0 SA1 SA2


S0-S3
DQMB0 to DQMB7
BA0, BA1
A0-A11
RAS
CAS
CKE0
WE
REGISTERS
RS0-RS3
RDQMB0-RDQMB7
RBA0 → BA0, RBA1 → BA1: SDRAMS
RA0-RA11 → A0-A11: SDRAMS
RRAS → RAS: SDRAMS
RCAS → CAS: SDRAMS
RCKE0 → CKE: SDRAMS
RWE → WE: SDRAMS
10k
V_{DD}
REGE
PLL CLK

Absolute maximum ratings

	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 to +4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD} V_{DDQ}	-1.0 to +4.6	V
Storage temperature	T_{stg}	-55 to +150	°C
Power dissipation	P_D	20	W
Short-circuit output current	I_{OS}	50	mA

Note:
Permanent damage to the device may occur if absolute maximum ratings are exceeded. Operation should be restricted to the conditions detailed in the operational sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC operating conditions and characteristics

(Voltage referenced to V_{SS}= 0V; T_A = 0 to 70°C)

	Symbol	Minimum	Typical	Maximum	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	$V_{DDQ+0.3}$	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	$I_{OH=-2mA}$
Output low voltage	V_{OL}	-	-	0.4	V	$I_{OL=2mA}$
Input leakage current (Inputs)	I_{IL}	-4	-	4	uA	3
Input leakage current (I/O pins)	I_{IL}	-3	-	3	uA	3,4

Notes:
(1) V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
(2) V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
(3) Any input $OV \le V_{IN} \le V_{DDQ}$
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
(4) Dout is disabled, $OV \le V_{OUT} \le V_{DDQ}$

Capacitance (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz)

		ORGANIZATION	
	Symbol	x72MAX	Unit
Input capacitance (A0-A11)	C_{IN1}	19	pF
Input capacitance (RAS, CAS, WE)	C_{IN2}	19	pF
Input capacitance (CKE0)	C_{IN3}	19	pF
Input capacitance (CLK0)	C_{IN4}	28	pF
Input capacitance (CS0-CS3)	C_{IN5}	15	pF
Input capacitance (DQM0-DQM7)	C_{IN6}	14	pF
Input capacitance (BA0-BA1)	C_{IN7}	19	pF
Input/Output capacitance (DQ0-DQ63)	C_{OUT}	20	pF
Input/Output capacitance (CB0-CB7)	C_{OUT1}	20	pF

DC characteristics (Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

	Symbol	Test Condition	ORGANIZATION x72	Unit	Note
Operating current (One bank active)	I_{DD1}	Burst length=1 $t_{RC} \geq t_{RC}$(min) I_{OL}=0 mA	2,660	mA	1
Precharge standby current in power-down mode	$I_{DD2}P$	CKE ≤ V_{IL} (max), t_{CC}=15ns	356	mA	3
	$I_{DD2}PS$	CKE & CLK ≤ V_{IL} (max), t_{CC}=15ns∞	117	mA	3
Precharge standby current in non power-down mode	$I_{DD2}N$	CKE ≥ V_{IH} (min), $\overline{CS}$ ≥ V_{IH} (min), t_{CC}=15ns Input signals are changed one time during 30ns	760	mA	3
	$I_{DD2}NS$	CKE ≥ V_{IH} (min), CLK ≥ V_{IL} (max), t_{CC}=∞ Input signals are stable	270	mA	3
Active standby current in power-down mode	$I_{DD3}P$	CKE ≤ V_{IL} (max), t_{CC}=15ns	446	mA	3
Active standby current in non power-down mode	$I_{DD3}N$	CKE ≥ V_{IH} (min), $\overline{CS}$ ≥ V_{IH} (min), t_{CC}=15ns Input signals are changed one tme during 30ns	1,120	mA	3
Operating current (Burst mode)	I_{DD4}	I_{OL}=0mA Page Burst 2 Banks activated t_{CCD}=2CLK	3,200	mA	1
Refresh current	I_{DD5}	t_{RC}=t_{RC}(min)	5,060	mA	2
Self refresh current	I_{DD6}	CKE ≤ 0.2V	276	mA	3

Notes: 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1 PLL & 3 Drive ICs.

AC operating test conditions (V_{DD}=3.3V ± 0.3V, T_A= 0 to 70°C)

	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf=1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 1	

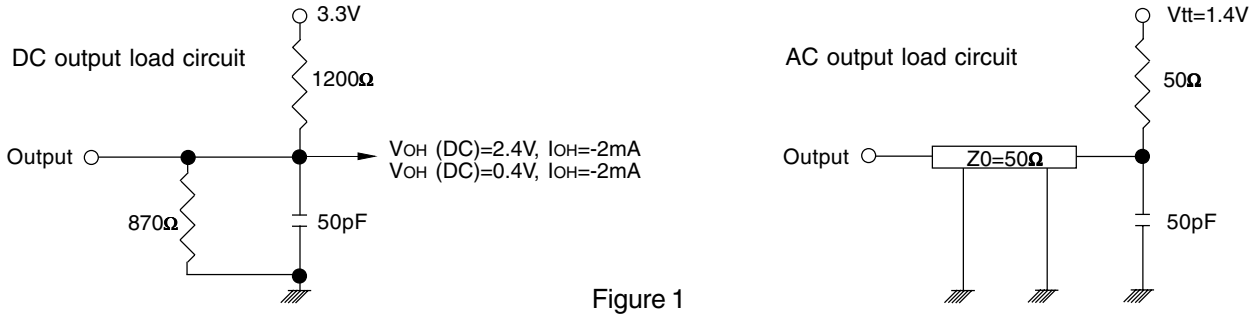


Figure 1

Operating AC parameter (AC operating conditions unless otherwise noted)

	Symbol	Time	Unit	Note
Row active to row active delay	t_{RRD}(min)	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD}(min)	20	ns	1
Row precharge time	t_{RP}(min)	20	ns	1
Row active time	t_{RAS}(min)	45	ns	1
	t_{RAS}(max)	100	us	
Row cycle time	t_{RC}(min)	67.5	ns	1
Last data in to row precharge	t_{RDL}(min)	1	CLK	2
Col. address to col. addess delay	t_{CCD}(min)	1	CLK	3

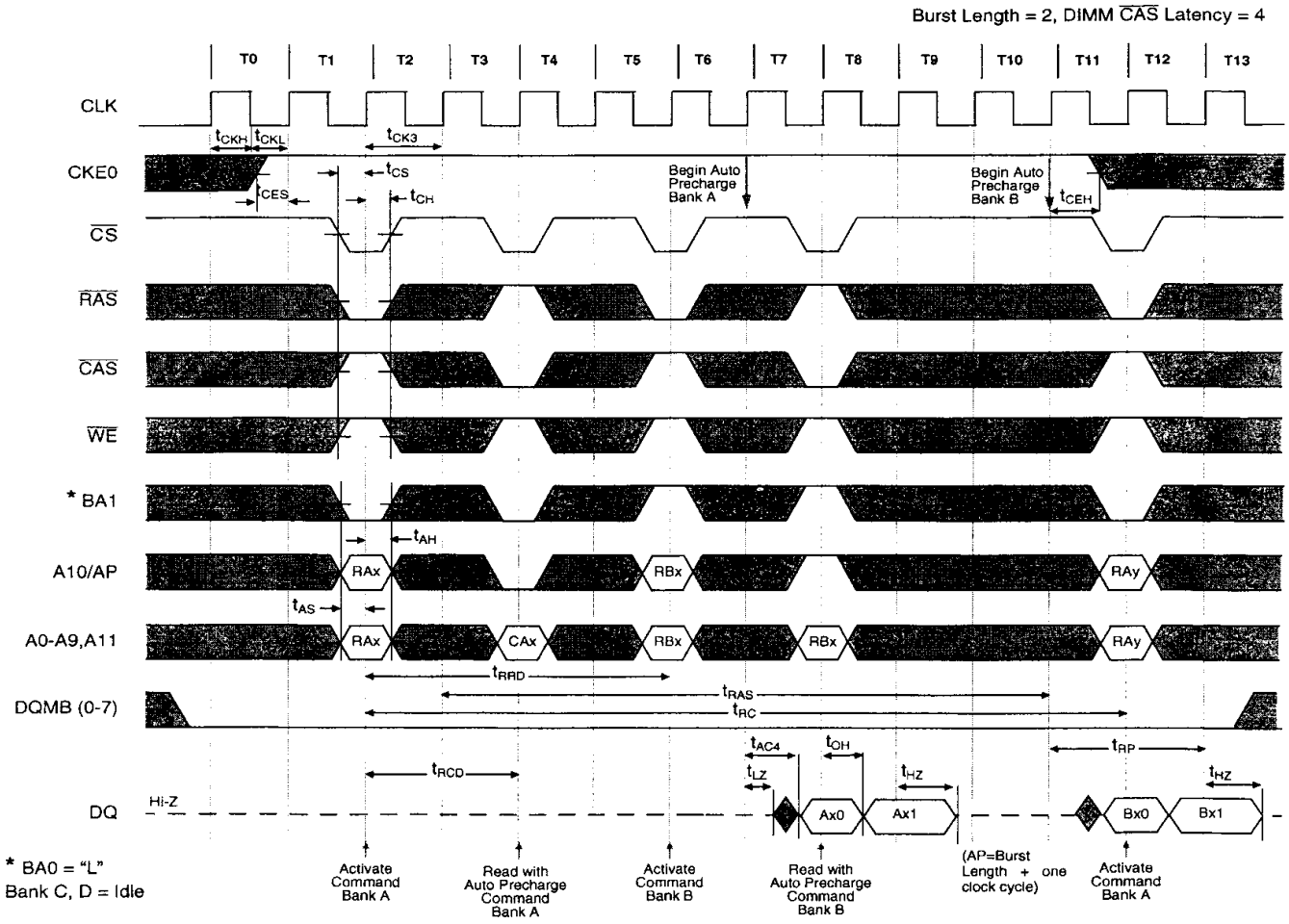
Notes: 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write in Reg. DIMM (1 CLK earlier than Unbuff. DIMM)
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC characteristics (AC operating conditions unless otherwise noted)

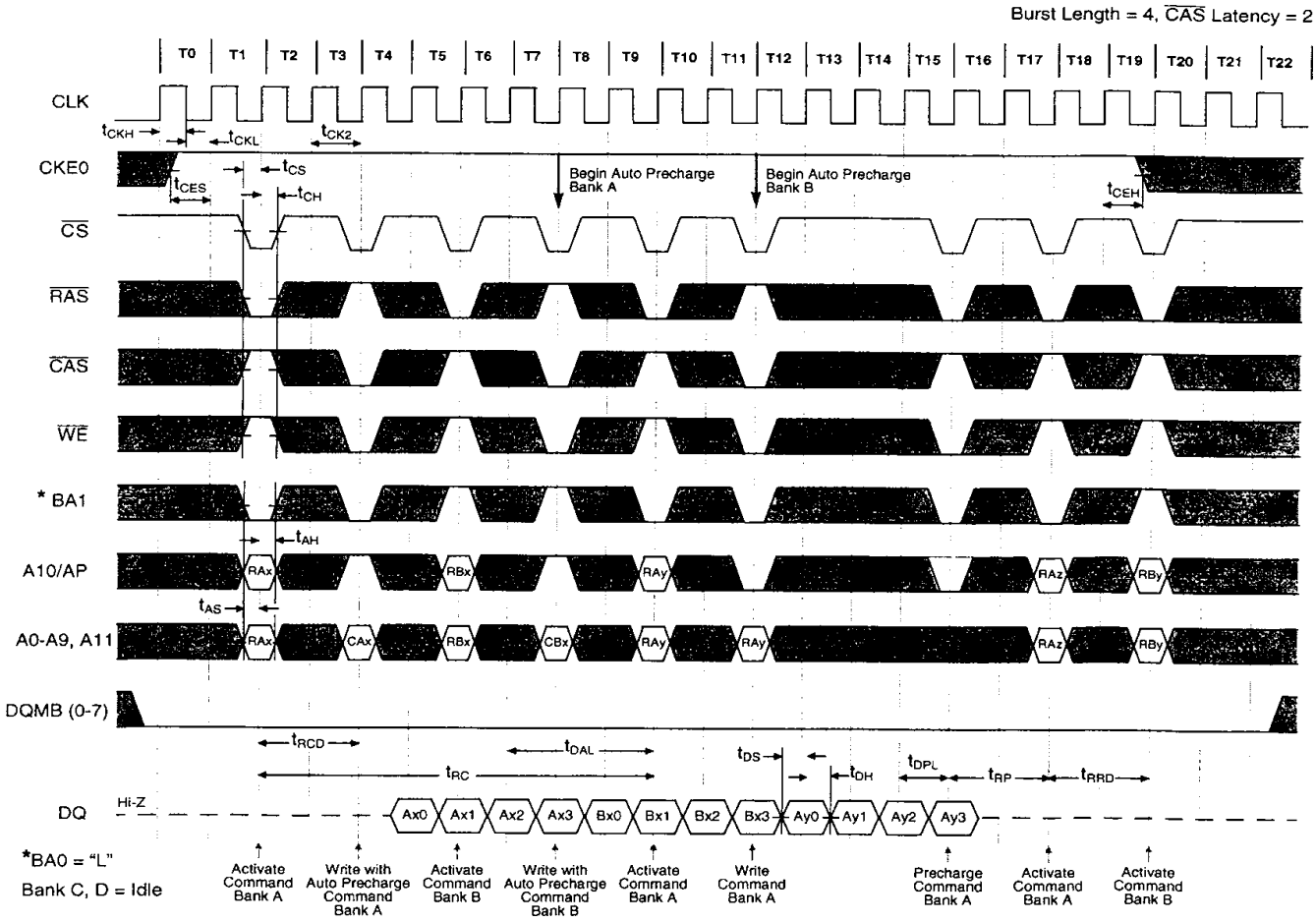
	CAS	Symbol	Minimum	Maximum	Unit	Note
CLK cycle time	CAS latency=2	tCK	7.5	1000	ns	1
CLK to valid output delay	CAS latency=2	tAC		5.65	ns	1,2
Output data hold time	CAS latency=2	t_{OH}	2.45		ns	1,2
CLK high pulse width		tCKH	2.5		ns	3
CLK low pulse width		tCKL	2.5		ns	3
Input setup time		tDS	1.75		ns	3
Input hold time		tDH	1.05		ns	3
CLK to output in Low-Z		tLZ	.6		ns	2
CLK to output in Hi-Z	CAS latency=2	tHZ	3.6	6	ns	1

Notes: 1. Parameters depend on programmed CAS latency. DIMM CAS Latency=Device CL+1 for Register Mode.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer that 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1] ns should be added to the parameter.

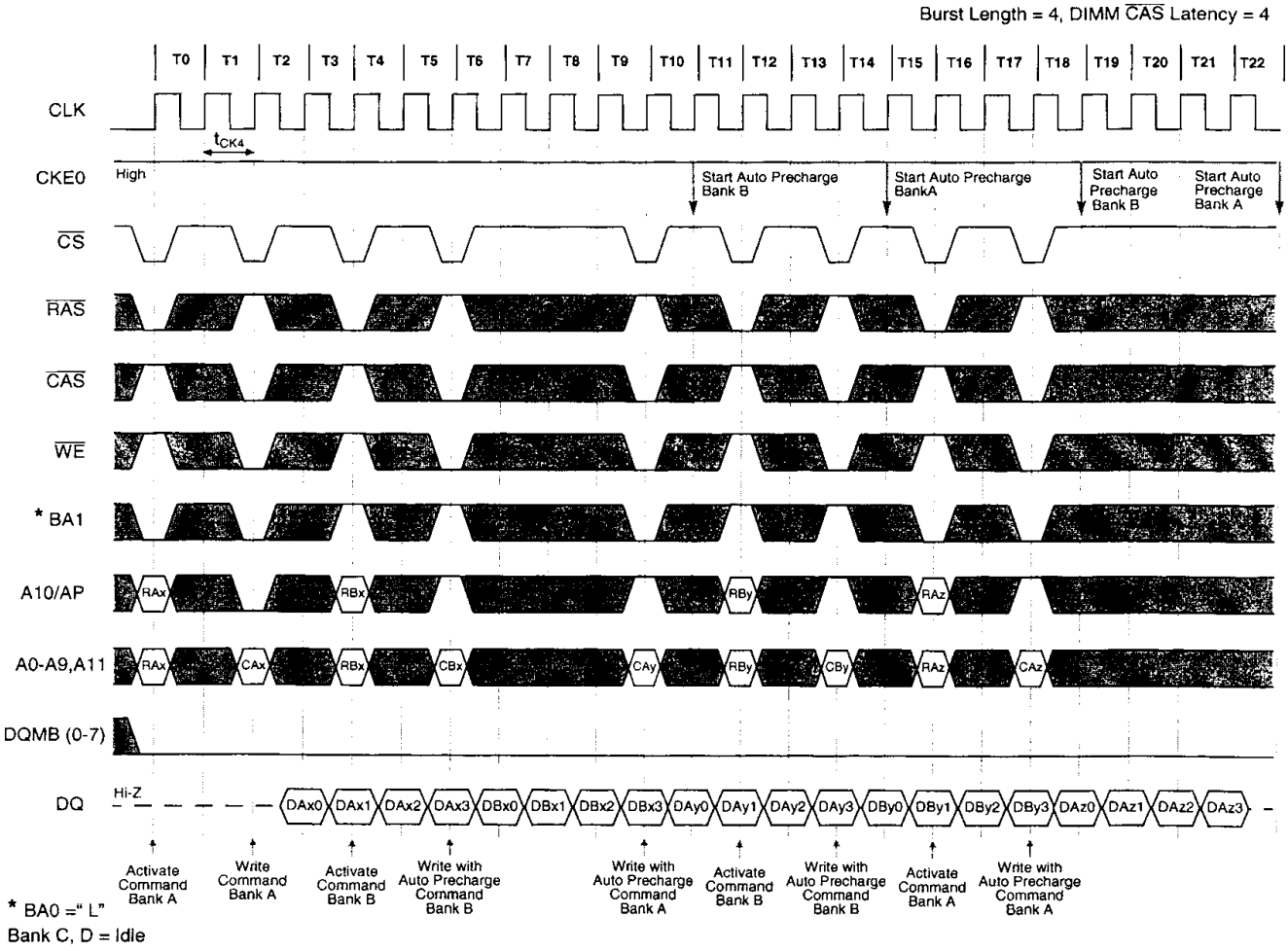
AC Parameters for Read Timing



AC Parameters for Write Timing

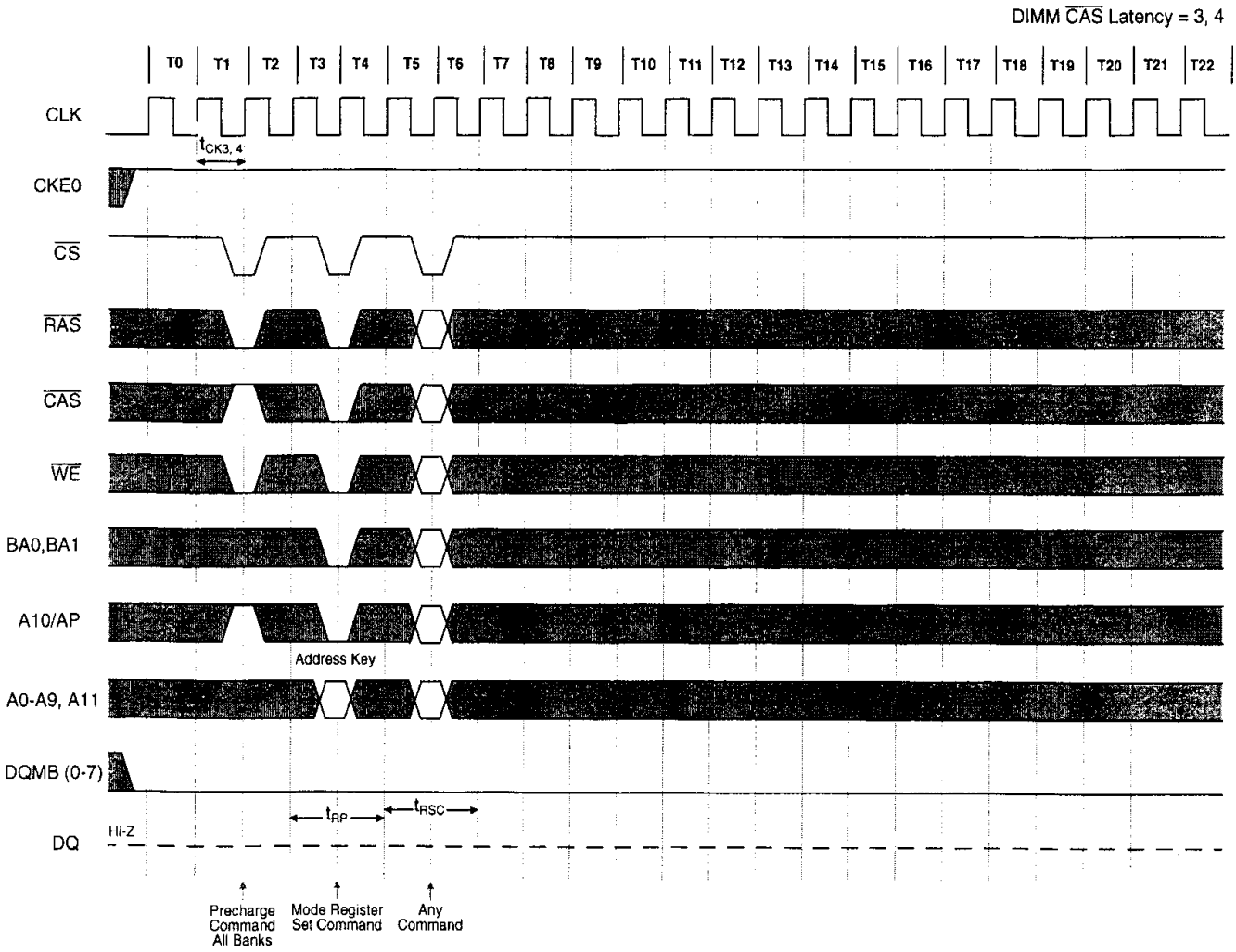


Auto Precharge After Write Burst

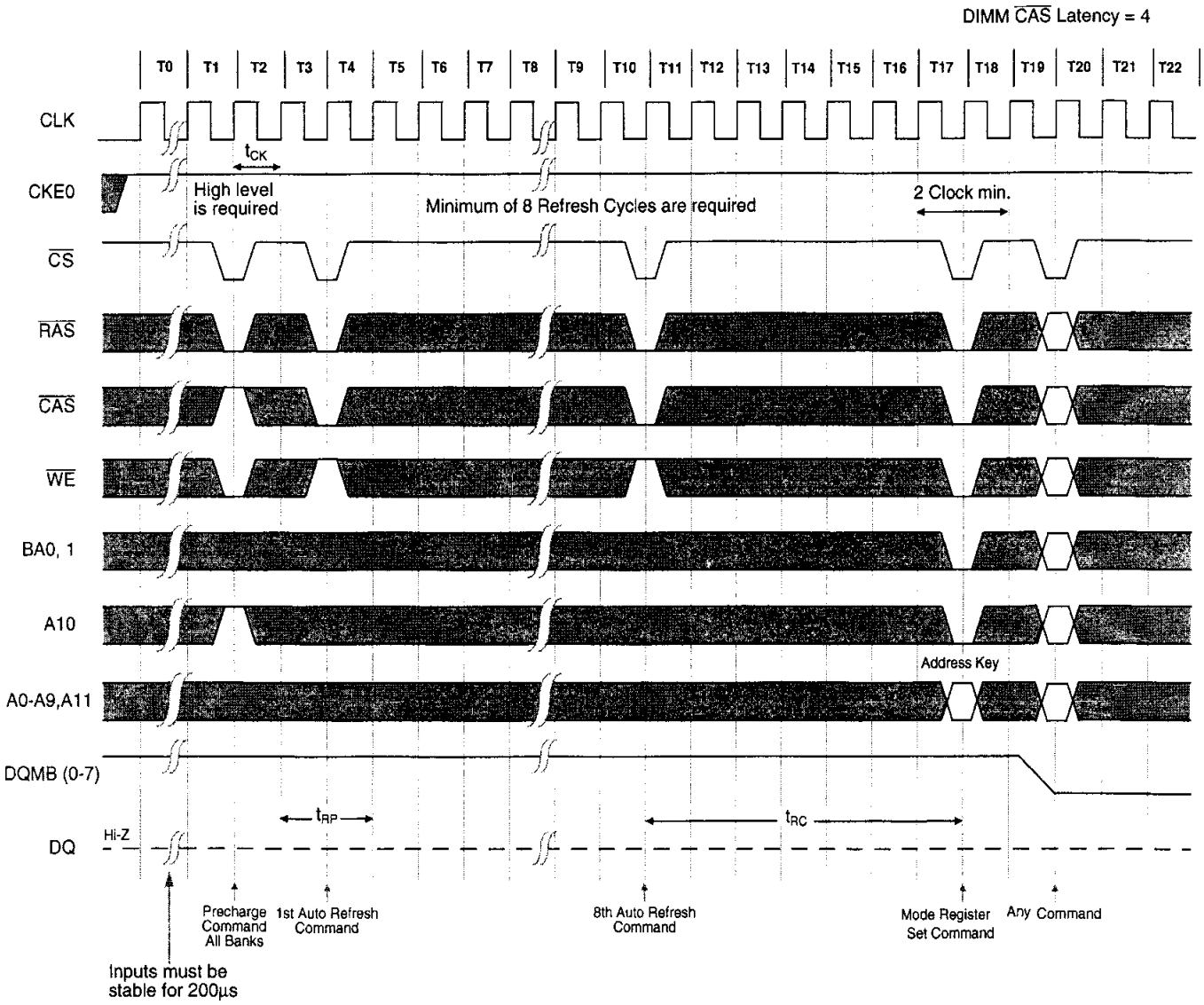


* BA0 =" L"
Bank C, D = Idle

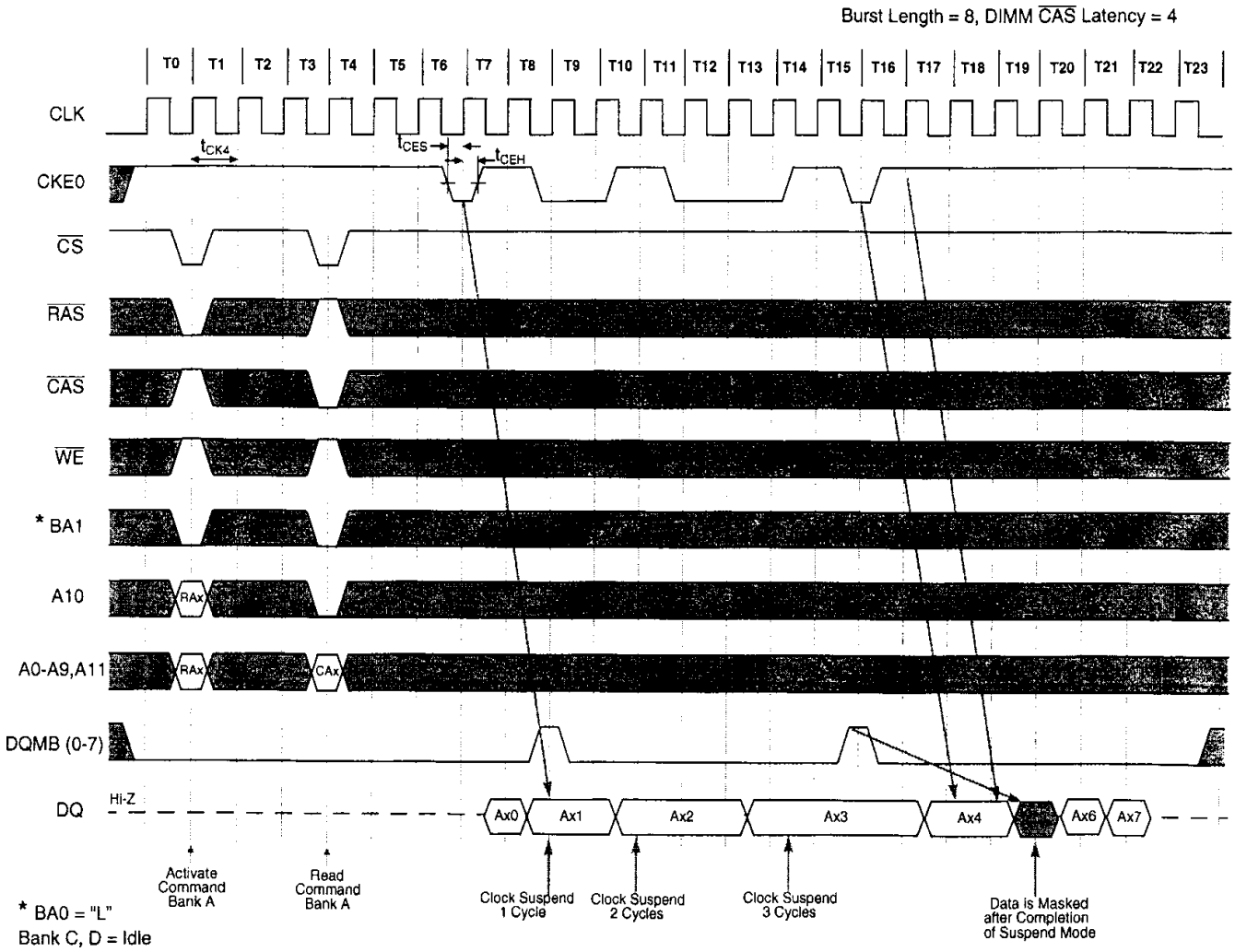
Mode Register Set



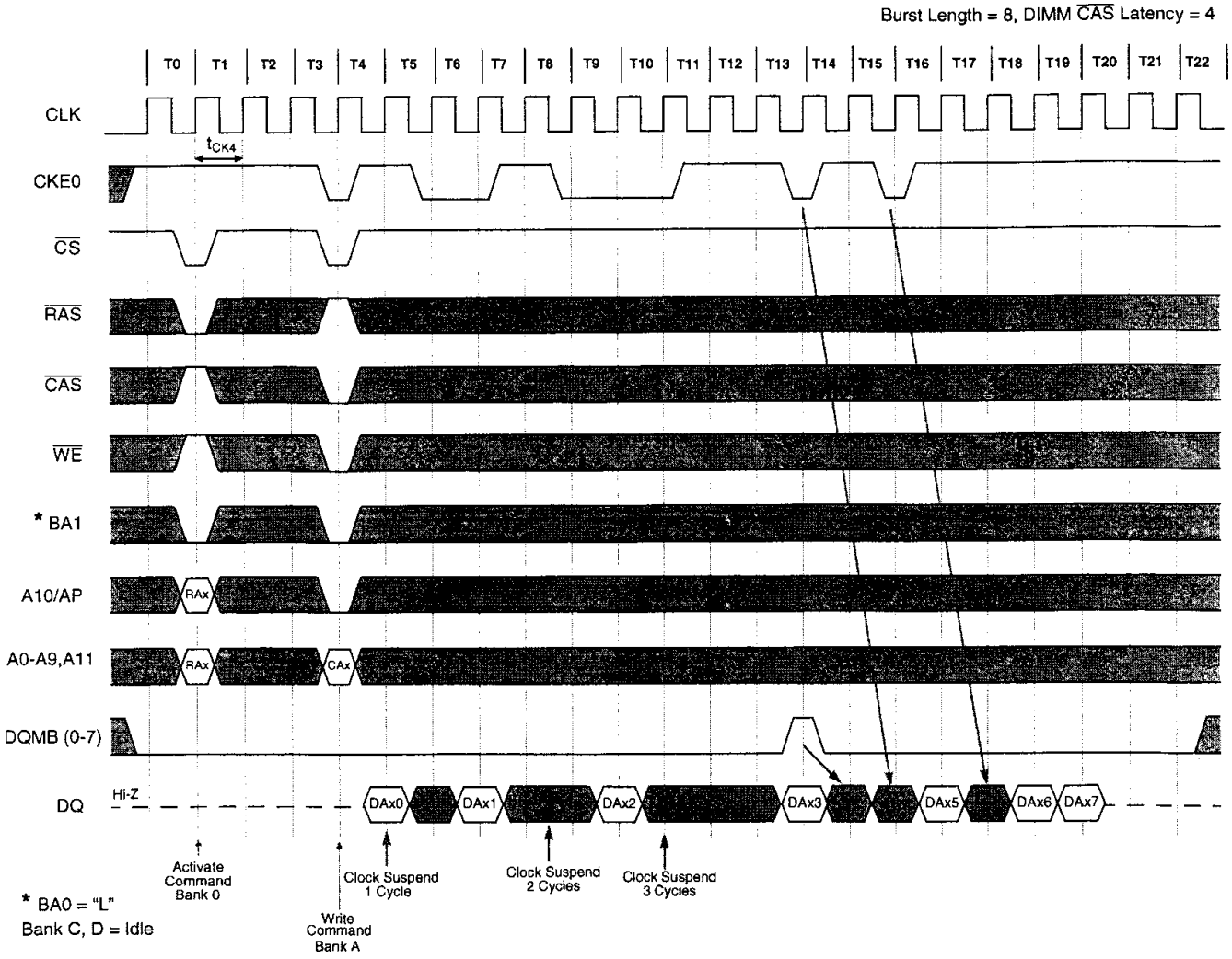
Power on Sequence and Auto Refresh (CBR)



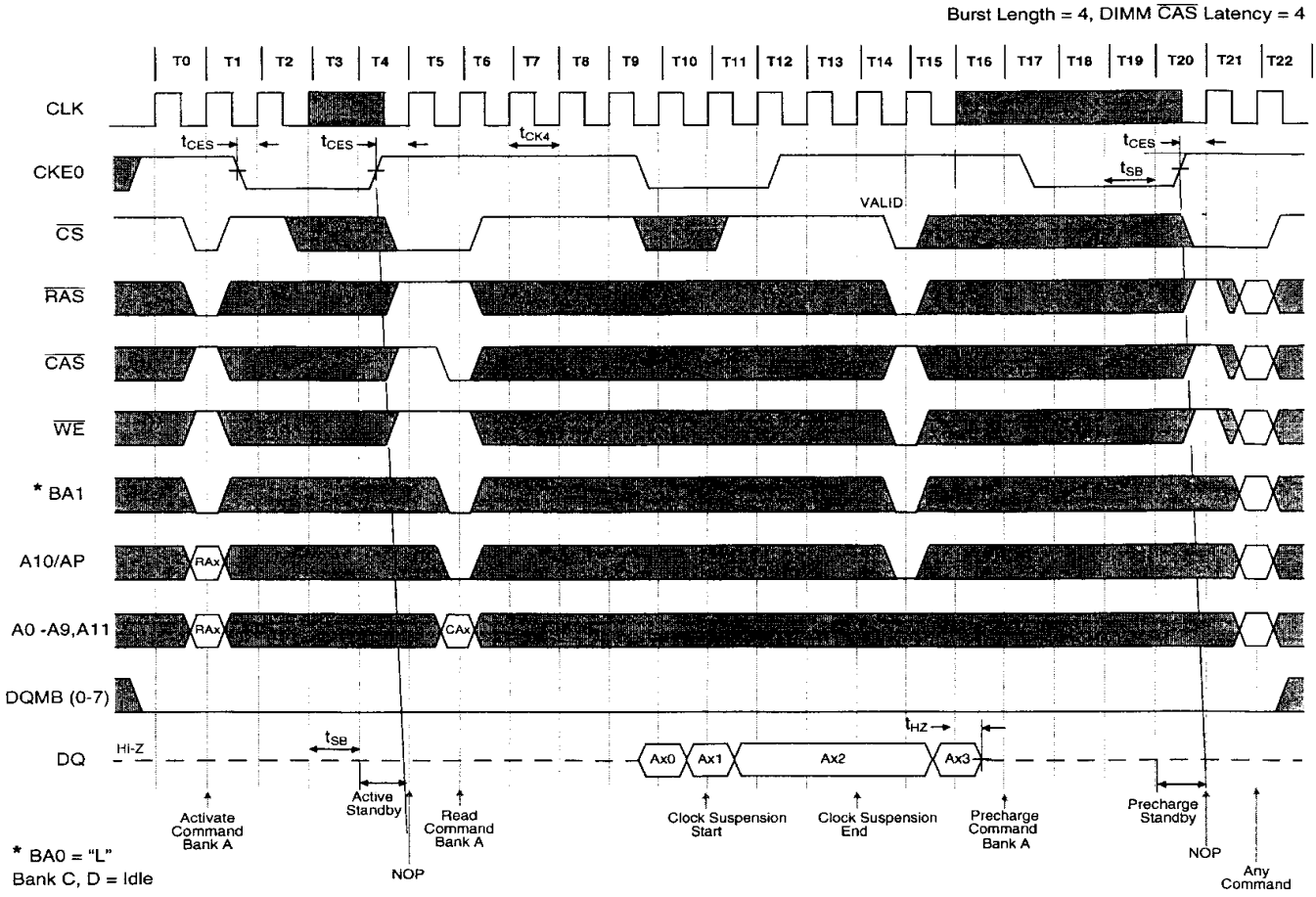
Clock Suspension / DQMB During Burst Read



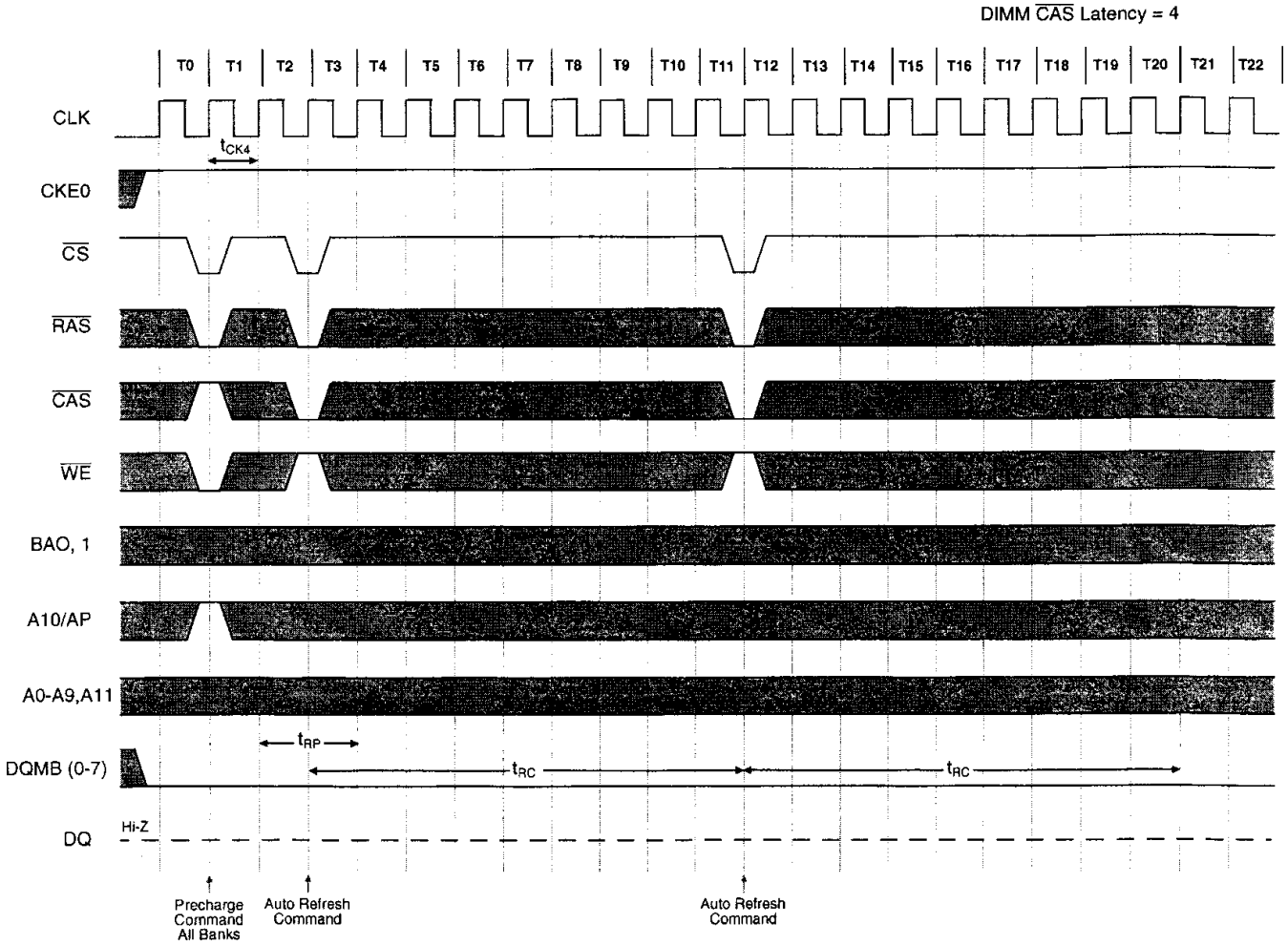
Clock Suspension / DQMB During Burst Write



Power Down Mode and Clock Suspend

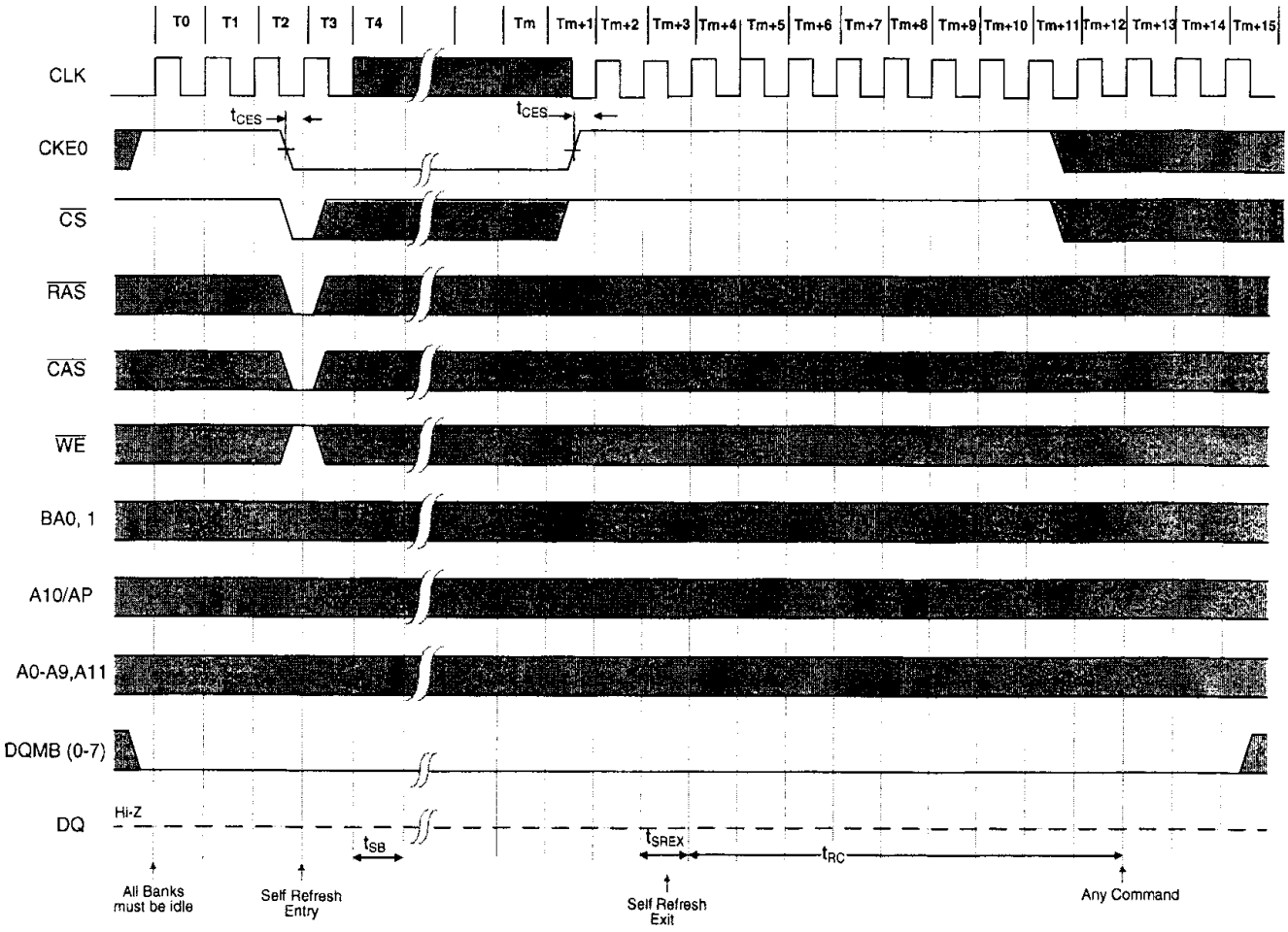


Auto Refresh (CBR)

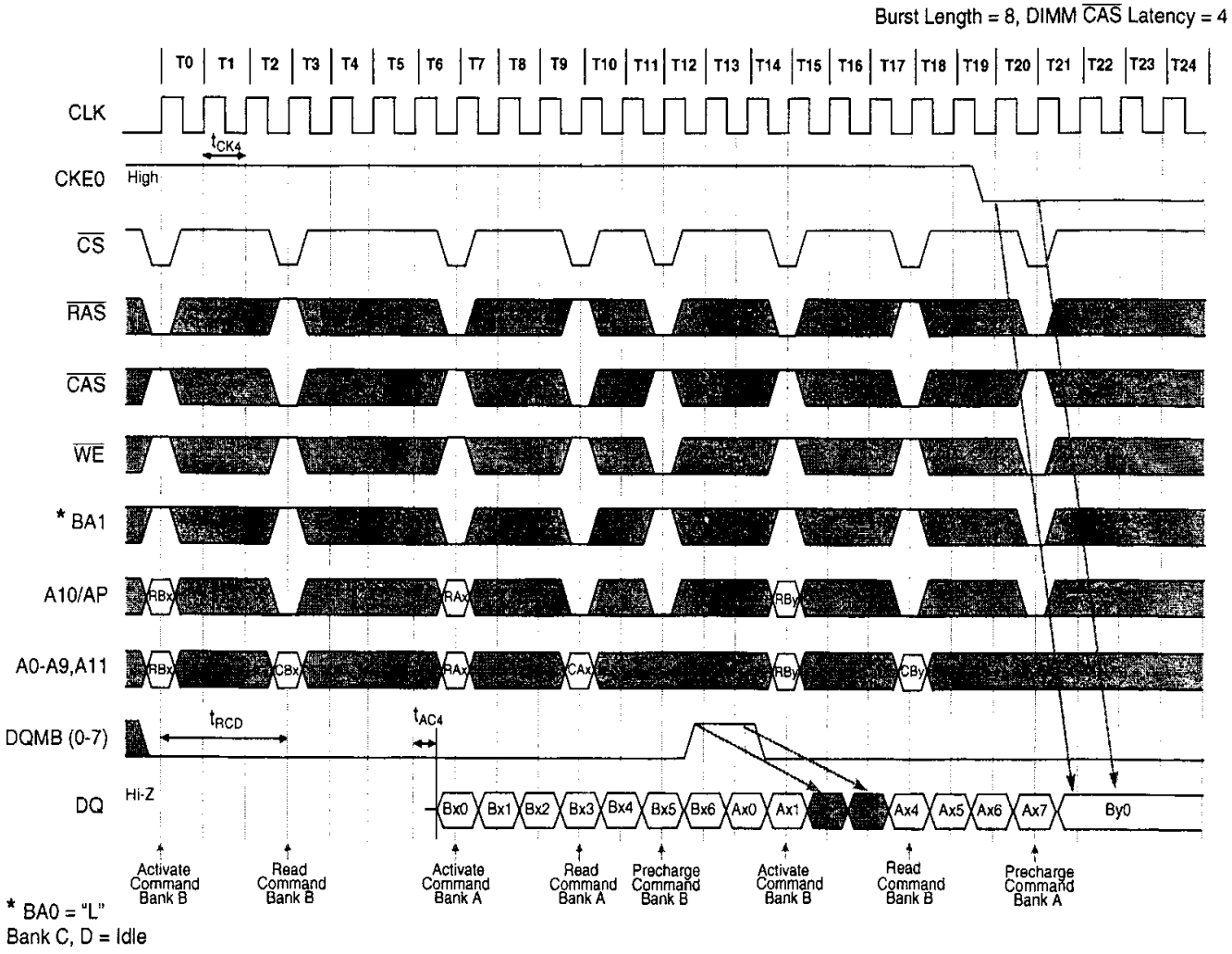


Self Refresh (Entry and Exit)

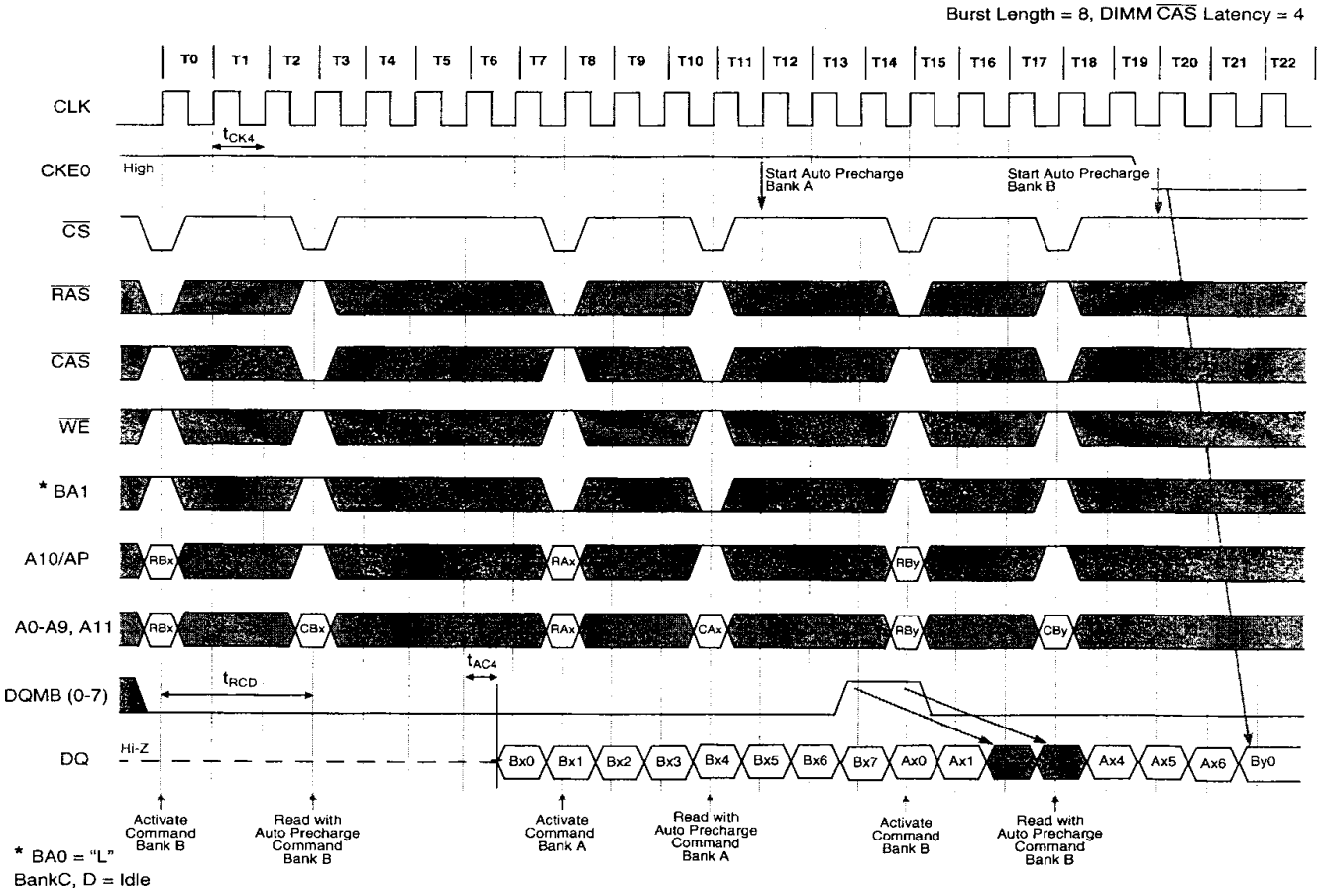
Note: The CK0 signal must be reestablished prior to DKE0 returning high.



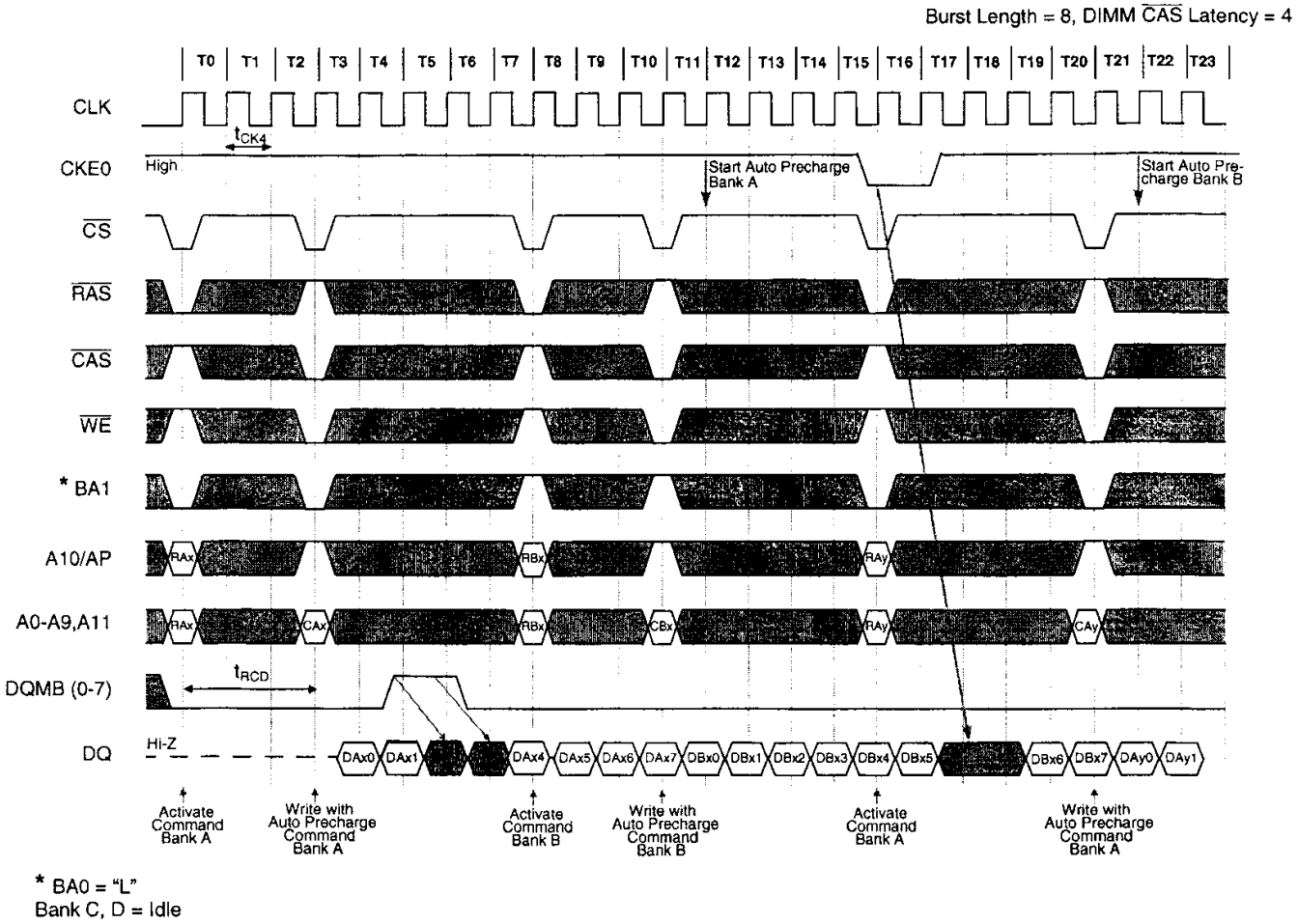
Random Row Read (Interleaving Banks) with Precharge



Random Row Read (Interleaving Banks) with Auto-Precharge

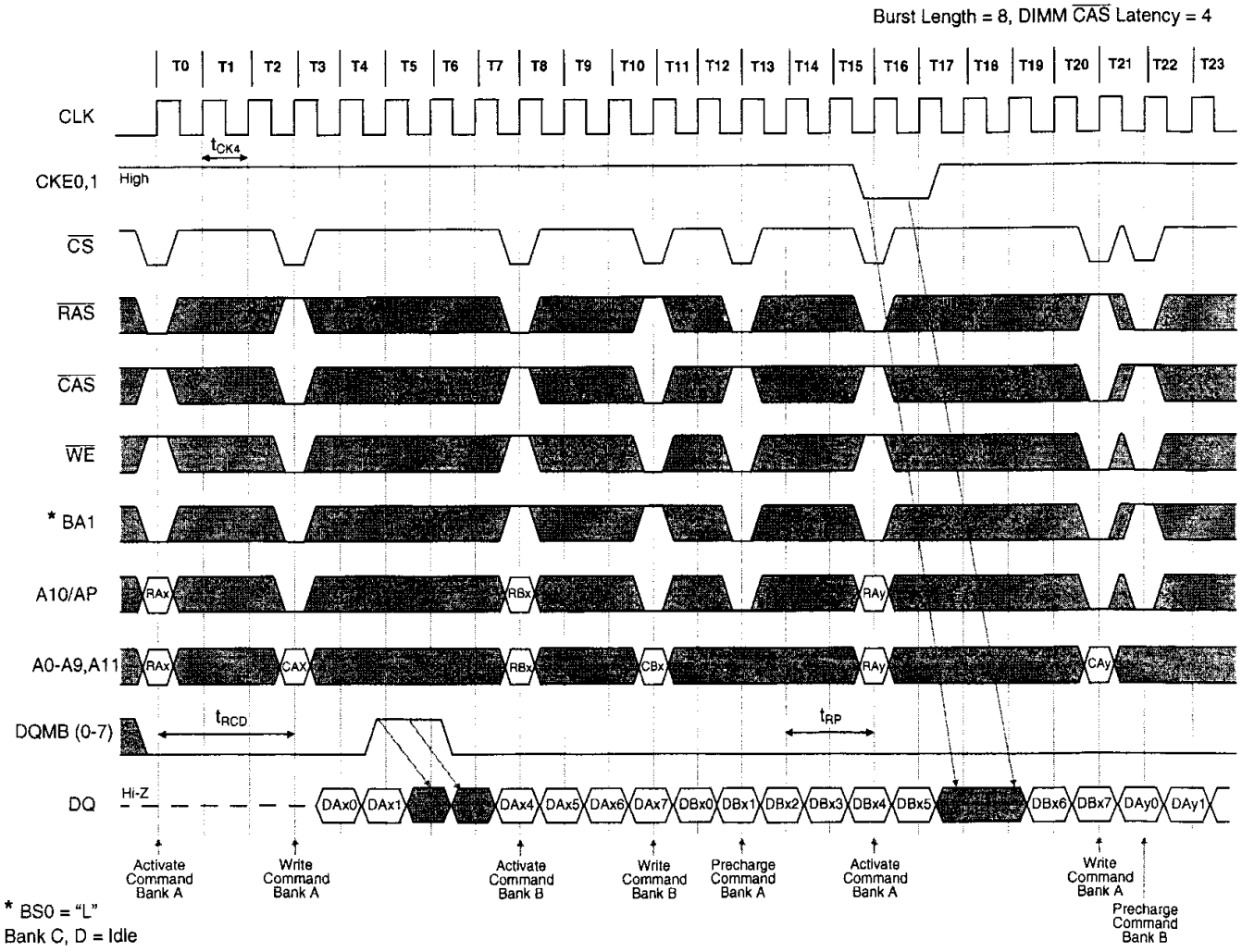


Random Row Write (Interleaving Banks) with Auto-Precharge

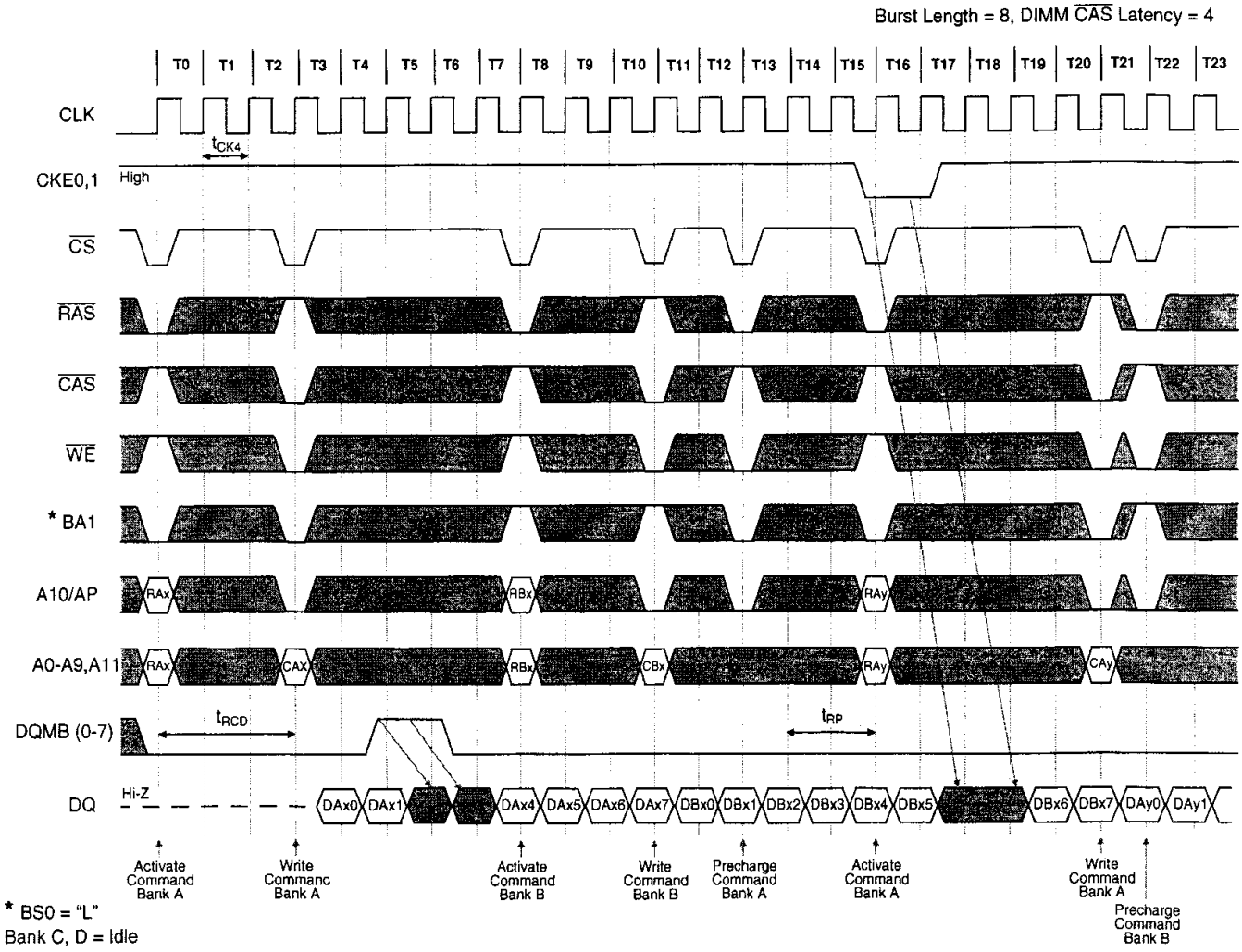


* BA0 = "L"
Bank C, D = Idle

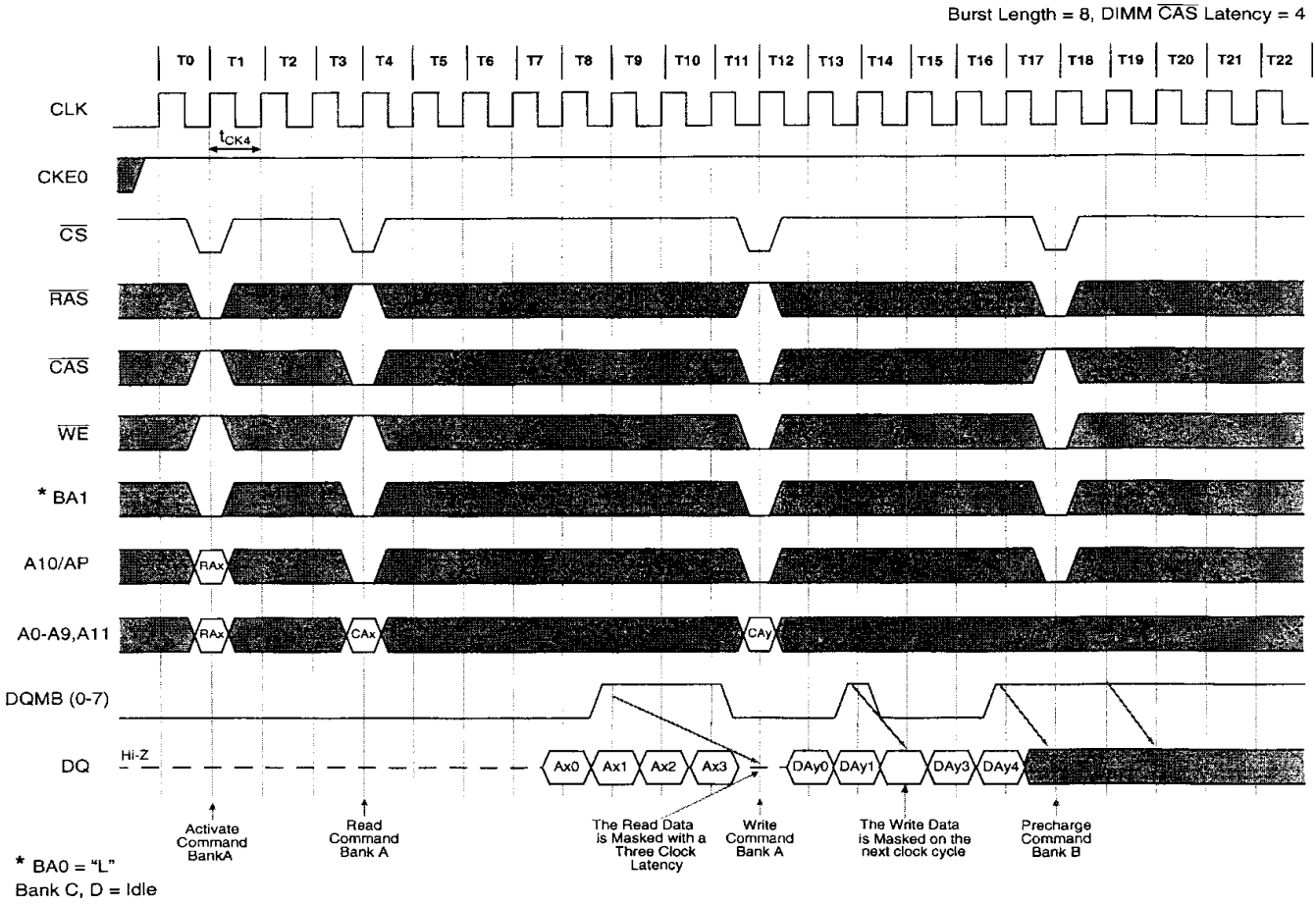
Random Row Write (Interleaving Banks) with Precharge



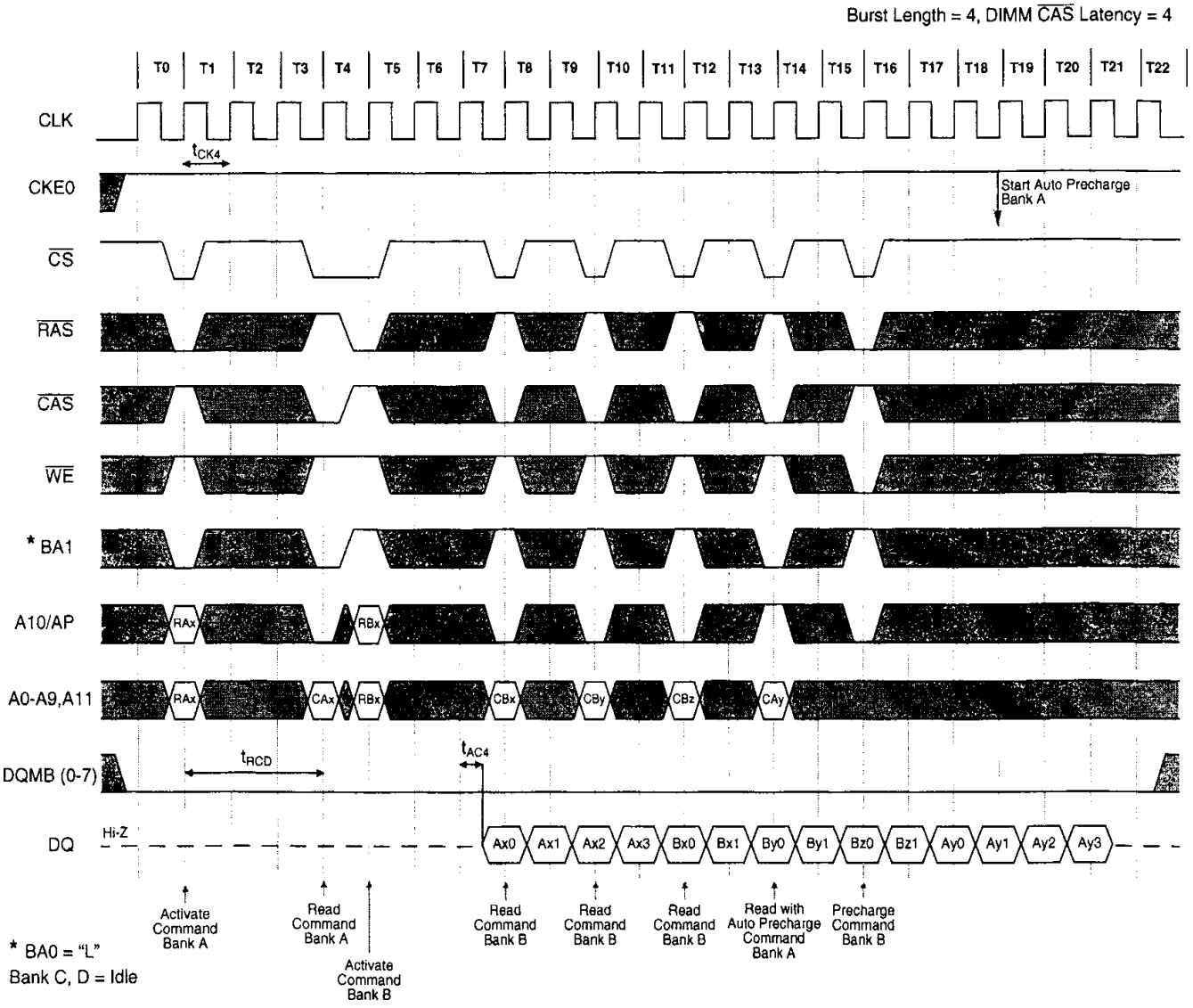
Random Row Write (Interleaving Banks) with Precharge



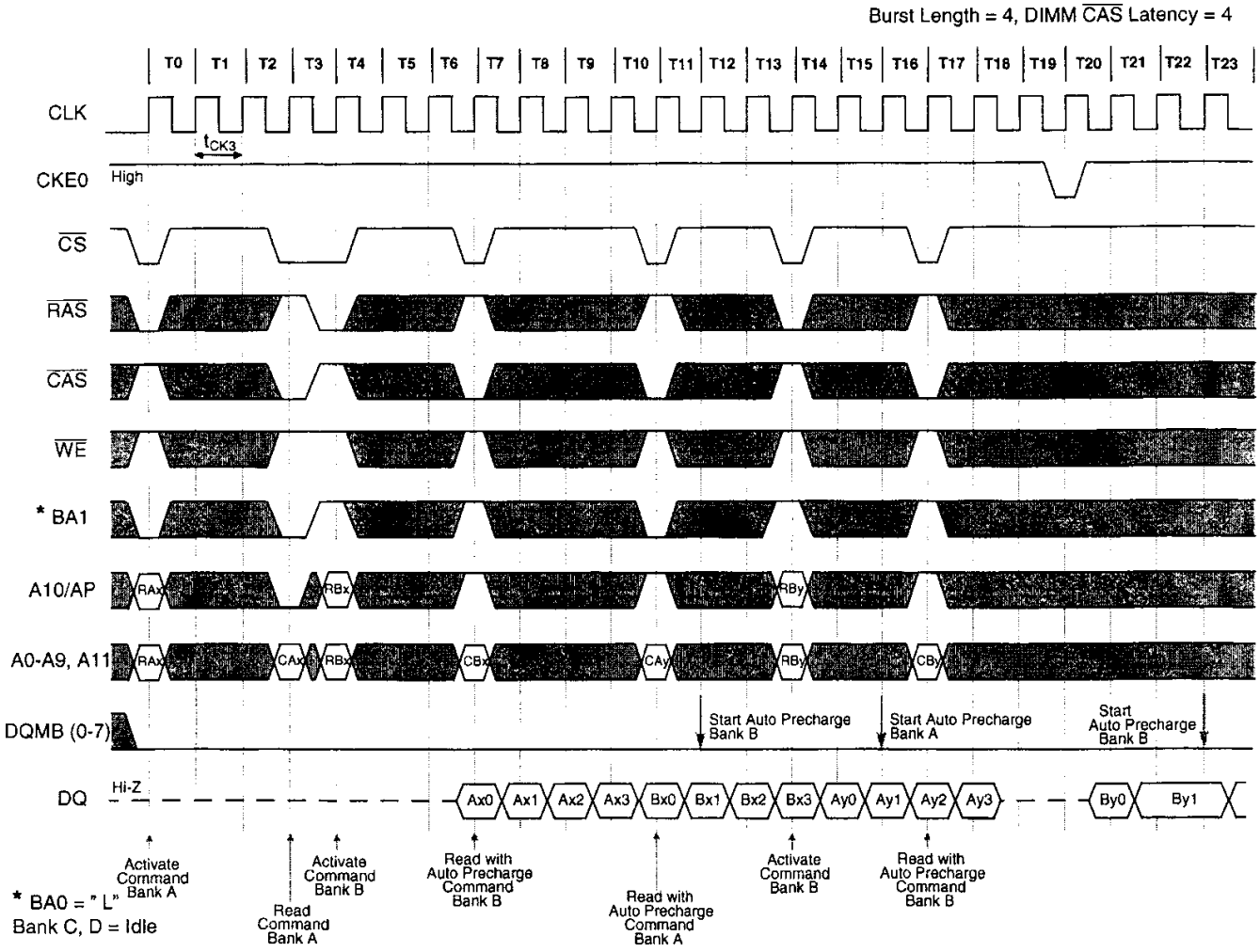
Read / Write Cycle



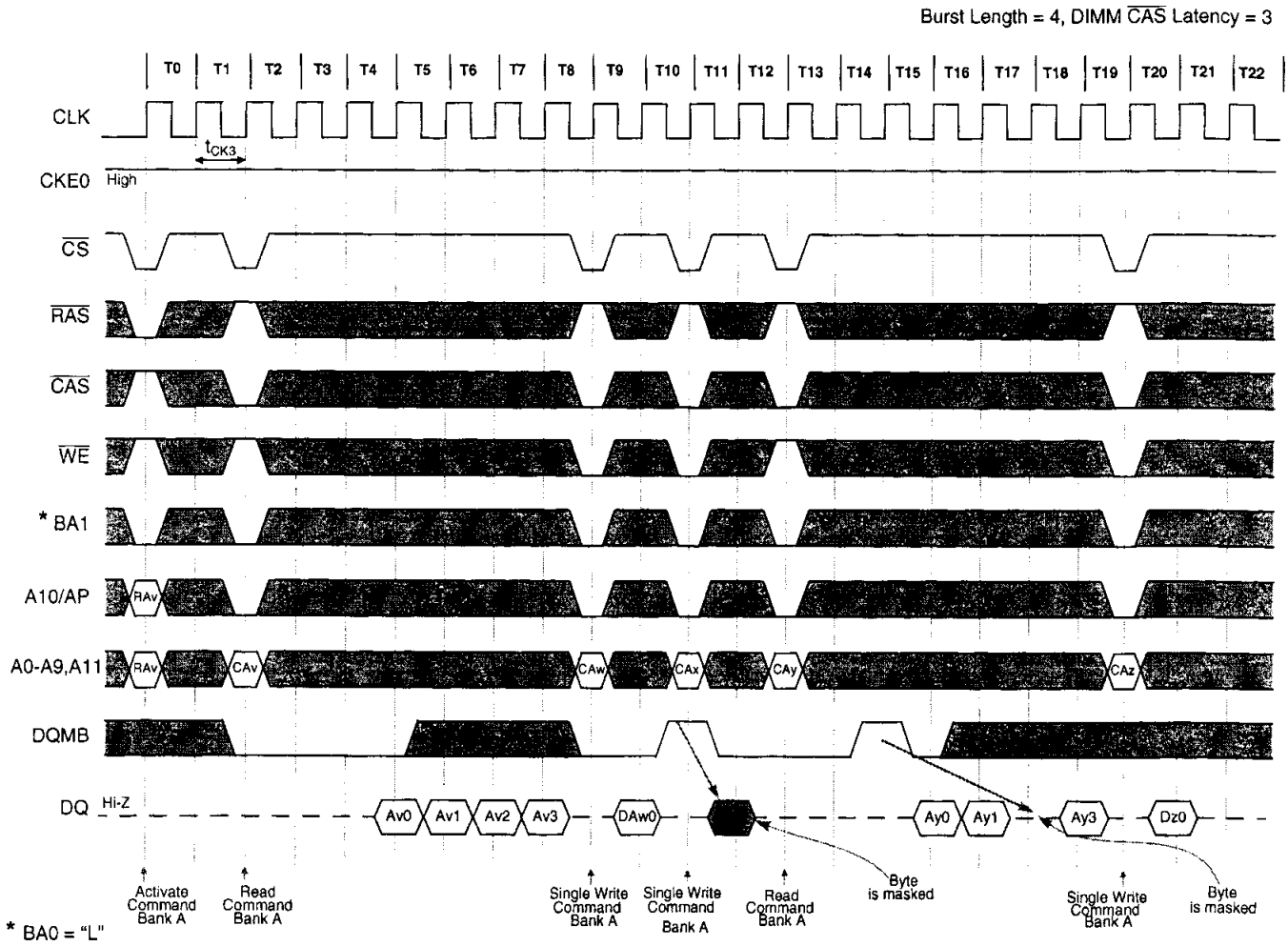
Interleaved Column Read Cycle



Auto Precharge After Read Burst



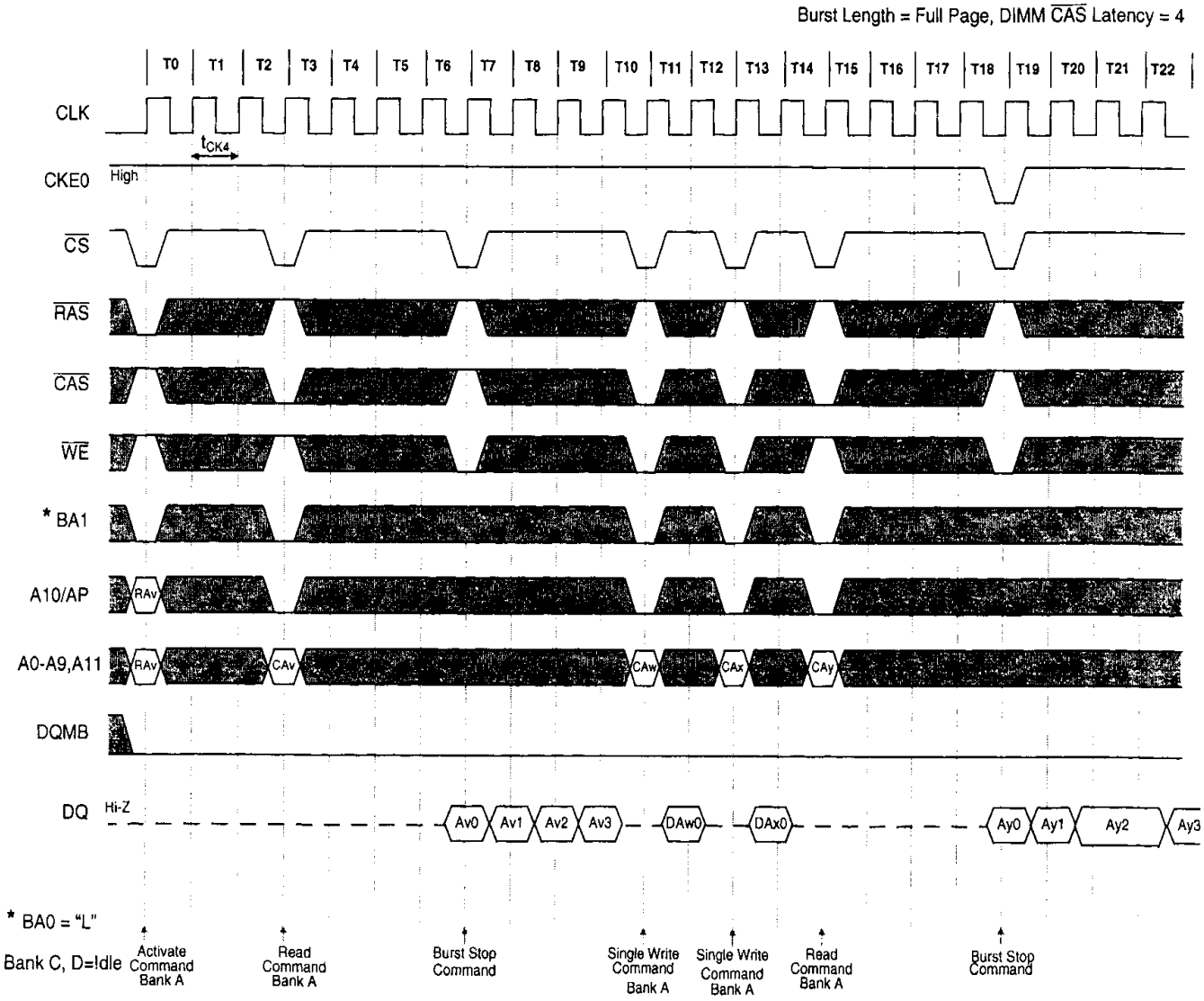
Burst Read and Single Write Operation‡



* BA0 = "L"
Bank C, D = Idle

‡ Note that the Single Write Operation is possible through programming of the Mode Register.

Full Page Burst Read and Single Write Operation‡



‡ Note that Single Write Operation is possible through programming of the Mode Register.