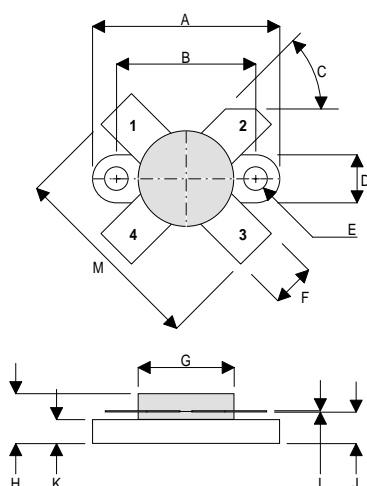


## MECHANICAL DATA



## DM

PIN 1	SOURCE	PIN 2	DRAIN
PIN 3	SOURCE	PIN 4	GATE

DIM	mm	Tol.	Inches	Tol.
A	24.76	0.13	0.975	0.005
B	18.42	0.13	0.725	0.005
C	45°	5°	45°	5°
D	6.35	0.13	0.25	0.005
E	3.17 Dia.	0.13	0.125 Dia.	0.005
F	5.71	0.13	0.225	0.005
G	12.7 Dia.	0.13	0.500 Dia.	0.005
H	6.60	REF	0.260	REF
I	0.13	0.02	0.005	0.001
J	4.32	0.13	0.170	0.005
K	3.17	0.13	0.125	0.005
M	26.16	0.25	1.03	0.010

# GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET 150W – 50V – 175MHz SINGLE ENDED

## FEATURES

- SIMPLIFIED AMPLIFIER DESIGN
- SUITABLE FOR BROAD BAND APPLICATIONS
- LOW  $C_{rss}$
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN – 10 dB MINIMUM

## APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS  
from 1 MHz to 175 MHz

ABSOLUTE MAXIMUM RATINGS ( $T_{case} = 25^{\circ}C$  unless otherwise stated)

$P_D$	Power Dissipation	220W
$BV_{DSS}$	Drain – Source Breakdown Voltage	125V
$BV_{GSS}$	Gate – Source Breakdown Voltage	$\pm 20V$
$I_{D(sat)}$	Drain Current	18A
$T_{stg}$	Storage Temperature	$-65$ to $150^{\circ}C$
$T_j$	Maximum Operating Junction Temperature	$200^{\circ}C$

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## ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25°C unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub> Drain–Source Breakdown Voltage	V <sub>GS</sub> = 0 I <sub>D</sub> = 100mA	125			V
I <sub>DSS</sub> Zero Gate Voltage Drain Current	V <sub>DS</sub> = 50V V <sub>GS</sub> = 0			6	mA
I <sub>GSS</sub> Gate Leakage Current	V <sub>GS</sub> = 20V V <sub>DS</sub> = 0			1	μA
V <sub>GS(th)</sub> Gate Threshold Voltage*	I <sub>D</sub> = 10mA V <sub>DS</sub> = V <sub>GS</sub>	1		7	V
g <sub>fs</sub> Forward Transconductance*	V <sub>DS</sub> = 10V I <sub>D</sub> = 3A	4.8			S
G <sub>PS</sub> Common Source Power Gain	P <sub>O</sub> = 150W	10			dB
η Drain Efficiency	V <sub>DS</sub> = 50V I <sub>DQ</sub> = 0.6A	50			%
VSWR Load Mismatch Tolerance	f = 175MHz	20:1			—
C <sub>iss</sub> Input Capacitance	V <sub>DS</sub> = 50V V <sub>GS</sub> = -5V f = 1MHz			360	pF
C <sub>oss</sub> Output Capacitance	V <sub>DS</sub> = 50V V <sub>GS</sub> = 0 f = 1MHz			150	pF
C <sub>rss</sub> Reverse Transfer Capacitance	V <sub>DS</sub> = 50V V <sub>GS</sub> = 0 f = 1MHz			9	pF

\* Pulse Test: Pulse Duration = 300 μs , Duty Cycle ≤ 2%

## HAZARDOUS MATERIAL WARNING

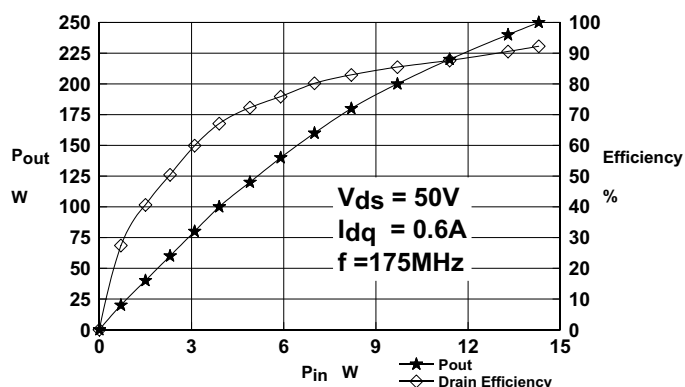
The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area.

**THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.**

## THERMAL DATA

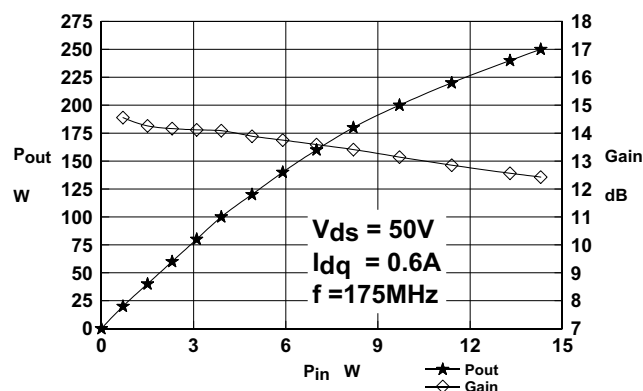
R <sub>THj-case</sub>	Thermal Resistance Junction – Case	Max. 0.8°C / W
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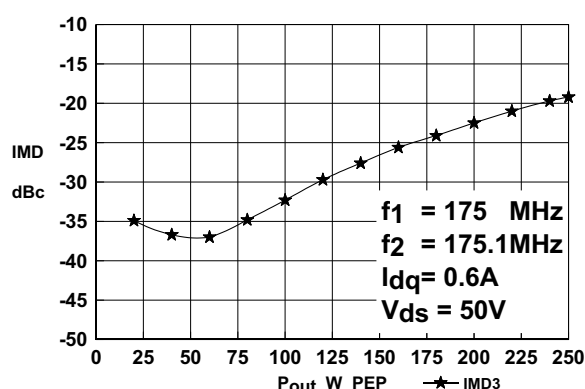
**Figure 1**

Power Output & Efficiency vs. Power Input



**Figure 2**

Power Output and Gain vs. Power Input



**Figure 3**

IMD<sub>3</sub> vs Power Output

## OPTIMUM SOURCE AND LOAD IMPEDANCE

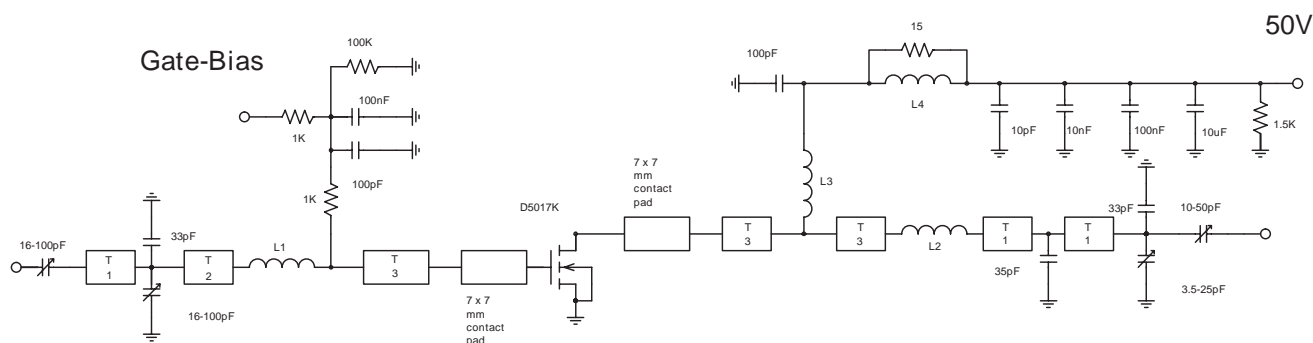
Frequency MHz	$Z_S$ $\Omega$	$Z_L$ $\Omega$
175	$2.6 + j1.8$	$4 + j1.2$

## Typical S Parameters

! Vds=50V Idq=0.6A  
# MHZ S MA R 50

!Freq !Mhz	S11 mag ang	S21 mag ang	S12 mag ang	S22 mag ang
60	0.918 -167.2	5.927 98.5	0.01 29.1	0.713 -157.5
70	0.916 -168.2	5.073 91.8	0.01 29.2	0.713 -156.7
80	0.918 -168.7	4.541 86.3	0.009 29.3	0.719 -156.6
90	0.917 -170.3	3.985 79.7	0.009 31.5	0.732 -157.2
100	0.919 -170.8	3.634 75.6	0.009 35.2	0.742 -157.8
110	0.927 -171.8	3.224 69.3	0.008 40	0.762 -158.5
120	0.926 -172.6	2.933 65.4	0.008 45.2	0.771 -159.1
130	0.932 -173.3	2.612 61	0.008 51.9	0.79 -160.1
140	0.934 -173.7	2.384 57.1	0.009 57.5	0.799 -160.9
150	0.936 -174.8	2.136 52.9	0.009 63.2	0.815 -162
160	0.941 -175.3	1.968 49.7	0.01 67.3	0.827 -162.4
170	0.939 -176.2	1.766 46.3	0.011 72.2	0.837 -163.9
180	0.943 -177	1.594 43.5	0.011 76.4	0.849 -164.9
190	0.946 -177.5	1.482 42.2	0.012 80.5	0.857 -165.9
200	0.954 -177.8	1.347 39.6	0.013 82.4	0.871 -166.1
210	0.952 -178.8	1.253 39	0.014 85.4	0.881 -168
220	0.957 -179.3	1.169 37.8	0.016 86.8	0.889 -168.8
230	0.958 -179.4	1.102 36	0.017 87.8	0.891 -169.6
240	0.961 179.9	1.019 33	0.018 87.9	0.9 -170.6
250	0.965 179.2	0.957 31	0.019 88	0.899 -171.5
260	0.966 178.9	0.882 29.3	0.02 88.9	0.91 -172.4
270	0.962 178.2	0.84 28.2	0.021 89.9	0.913 -173
280	0.965 177.8	0.786 27.1	0.023 90.1	0.922 -173.3
290	0.969 177.5	0.733 26.7	0.024 91.1	0.927 -175.3
300	0.97 176.6	0.703 26.6	0.026 90.8	0.93 -175.2
310	0.97 176.6	0.669 25.3	0.027 90.2	0.934 -176.2
320	0.971 175.8	0.638 22.5	0.028 88.2	0.938 -177.1
330	0.972 175.7	0.598 20	0.029 86.7	0.939 -177.7
340	0.974 175	0.559 19.2	0.029 86.7	0.944 -178.4
350	0.976 175.1	0.516 17.8	0.03 87.5	0.944 -179.6
360	0.977 173.7	0.486 17.3	0.031 88.3	0.95 -180
370	0.976 173.3	0.455 17.8	0.032 89.6	0.952 179.3
380	0.975 173.4	0.437 18.2	0.034 89.8	0.952 178.4
390	0.977 172.8	0.413 18.8	0.035 89.5	0.958 177.5
400	0.976 172.2	0.402 20.5	0.037 90.4	0.959 177.7
410	0.979 172.2	0.396 19.4	0.039 89.6	0.962 176.3
420	0.978 171.6	0.377 17.6	0.04 88	0.962 176.3
430	0.977 171.3	0.362 16	0.04 86.3	0.965 175.4
440	0.982 170.7	0.341 14.9	0.041 86	0.966 174.5
450	0.979 170.4	0.327 15.1	0.041 86.4	0.966 174.4
460	0.978 170.5	0.31 15	0.042 86.5	0.97 174
470	0.98 169.9	0.3 15.9	0.043 87.3	0.967 173.2
480	0.982 169.6	0.289 16.3	0.045 87.4	0.972 172.6
490	0.979 169	0.28 16.5	0.046 87.7	0.968 171.7
500	0.98 168.8	0.271 16.6	0.047 87.4	0.969 171.7

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## D5017UK 175MHz Test Fixture

**Substrate 1.6mm PTFE/glass,  $\epsilon_r = 2.5$**

**All microstrip lines  $W = 5\text{mm}$**

**T1 7.5mm**

**T2 12.5 mm**

**T3 6mm**

**L1 Hairpin loop 18 swg 10mm high, 6.5mm gap**

**L2 Hairpin loop 5mm wide ribbon, 7mm high, 3.5 mm gap**

**L3 9 turns 19swg enamelled copper wire, 6mm id.**

**L4 12 turns 19swg enamelled copper wire on Fair-Rite FT82 ferrite core**

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