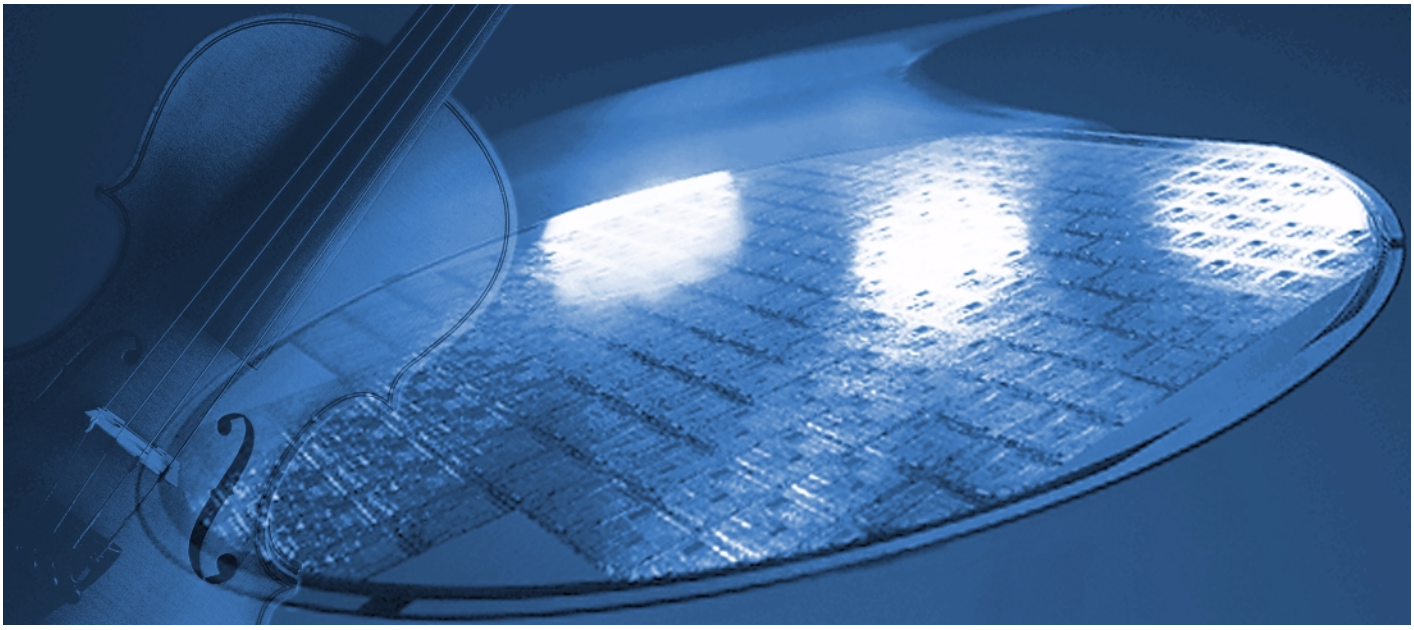
MICRONAS

DAC 3560C

Feb/2002



DAC 3560C
Stereo Audio DAC with Power Amplifiers and Power Management

The DAC 3560C is a single-chip, high-precision, dual digital-to-analog converter designed for audio applications. The IC employes a conversion technique based on oversampling with noise-shaping. With the implementation of Micronas' unique multibit sigma-delta approach, high linearity, less sensitivity to clock jitter, and an enhanced S/N ratio have been achieved. The DAC 3560C is controlled via SPI or I^2C bus.

Digital audio input data is received via a versatile I^2S interface. The IC provides three integrated power audio outputs: a 25-mW stereo headphone, a 100-mW mono earpiece, and a 410-mW mono loudspeaker output. Mixing of additional analog audio sources to the D/A-converted signal is also supported.

For applications with a noise-critical power supply environment, the DAC 3560C is equipped with a low-dropout regulator (LDO).

The IC is designed for all kinds of applications in the audio and multimedia field, such as mobile phones, PDA's, and MP3 / CD / DVD Players.

Features

- Three integrated power audio outputs
  - 25-mW stereo headphone outputs
  - 100-mW mono earpiece output
  - 410-mW mono loudspeaker output
- Integrated LDO
- 100 dB PSRR
- 95-dB SNR multi-bit Sigma-Delta DAC
- Continous sample rates from 8 kHz to 192 kHz
- Analog stereo and mono line inputs with programmable gain
- Pop-free power on and off of audio outputs
- Capacitor-free audio driver connection
- I^2C/SPI compatible serial control ports
- I^2S audio interface
- Programmable power management
- –30 dB to 6 dB analog volume, mute
- 3.0 V (2.2 V) to 5.5 V supply voltage
- 1.8 V to 5.5 V digital I/O voltage
- Standby mode

Applications

- PDAs
- Portable phones
- Hand-held terminals
- Portable players

Package

- 40-Pin Plastic Quad Flat No leads package (PQFN40)

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System Architecture

The DAC 3560C provides three audio driver outputs capable to drive 2×25 mW, 100 mW and 410 mW into 32 Ω, 32 Ω and 8 Ω loads. Either digital or analog audio can be delivered to the DAC 3560C. Digital audio data is sent via a I²S-compatible interface to a multi-bit sigma-delta DAC in which all internal oversampling clocks are derived from the I²S clock input by means of the internal PLL. Analog audio sources can be mixed to the digital data by means of one mono and two stereo line inputs. All line inputs have programmable gains.

The I²C/SPI-compatible control interface provides full control over the DAC 3560C thus allowing configuration of various sample rates, gain/volume settings of the analog inputs/outputs, as well as the possibility to power on/off signal chains in order to optimize power consumption. The audio drivers' outputs can be ramped up or down from or to their quiescent level to suppress audible pops during power-on or power-off.

For applications with a noisy power supply, the DAC 3560C contains a low-dropout regulator which can be used to improve the PSRR of the headset/earpiece driver to >100 dB at supply voltages as low as 3 V. If the PSRR is a non-critical parameter, then the DAC 3560C can be used without the LDO, allowing a lowered supply limit of 2.7 V. A version with a lowered supply limit of 2.2 V is planned.

Furthermore, the digital I/O-Interfaces have a separate supply pin which provides an I/O-supply voltage as low as 1.8 V thus allowing direct DSP and µC connection.

As an additional feature, the DAC 3560C provides a common output for the single-ended stereo headset driver outputs enabling a capacitor-free headset connection.

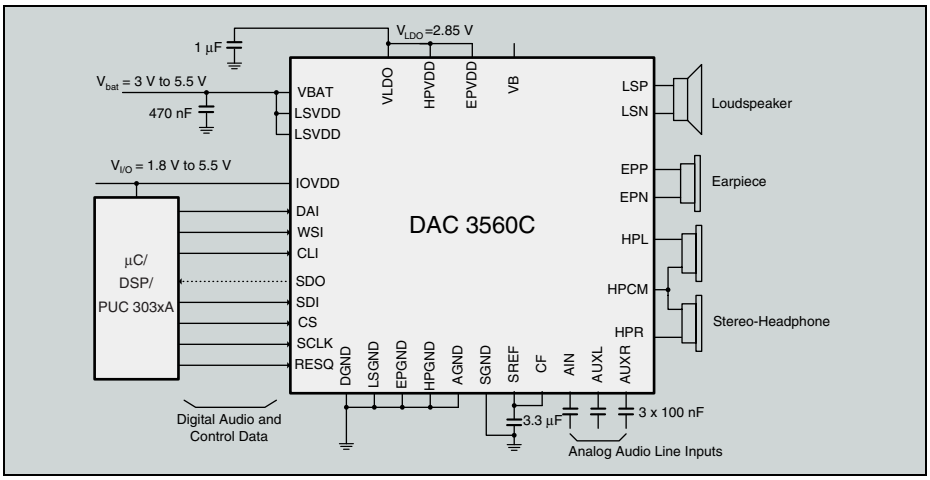

Fig. 1: Typical application circuit

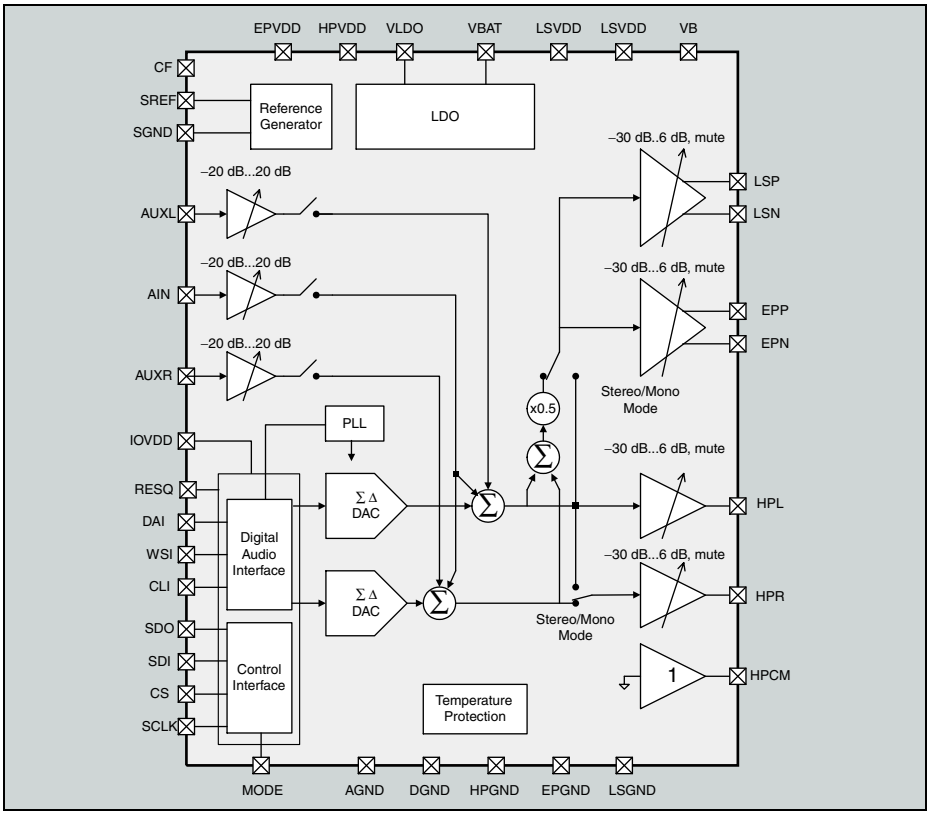

Fig. 2: Block diagram of the DAC 3560C

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