

Precision Quad SPDT Analog Switch

FEATURES

- $\pm 22\text{-V}$ Supply Voltage Range
- TTL and CMOS Compatible Logic
- Low On-Resistance ($25\ \Omega$)
- On-Resistance Matched Between Channels ($<2\ \Omega$)
- Flat On-Resistance Over Analog Signal Range ($\Delta <3\ \Omega$)
- Low Charge Injection ($1\ \text{pC}$)
- Low Leakage ($0.2\ \text{nA}$)
- Fast Switching ($175\ \text{ns}$)
- Single-Supply Operation ($5\ \text{V}$ to $40\ \text{V}$)
- ESD tolerance $>2\ \text{kV}$ per 3015.x
- Low Power ($<1\ \mu\text{A}$) – DG333A/333AL

BENEFITS

- Rail-to-Rail Analog Signal Range
- Simple Logic Interface
- High Precision and Accuracy
- Minimal Transients
- Low Distortion
- Reduced Power Consumption
- Improved Reliability
- Break-Before-Make Switching Action

APPLICATIONS

- Audio Switching
- Test Equipment
- Portable Instrumentation
- Communication Systems
- PBX, PABX
- Computer Peripherals
- Mass Storage Systems
- Switched-Capacitor Networks
- Battery-Powered Systems

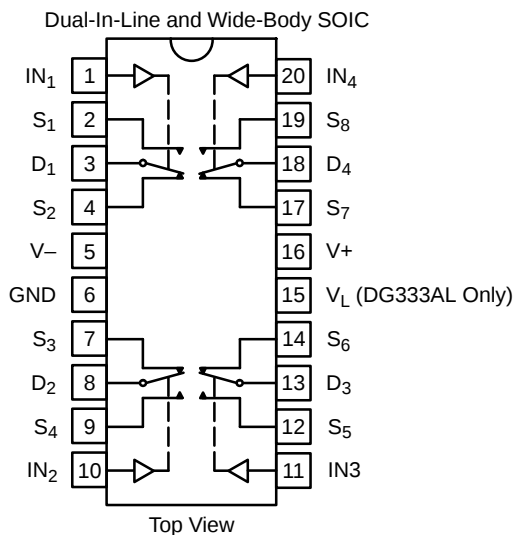
DESCRIPTION

The DG333A/333AL consist of four independently controlled single-pole double-throw analog switches. These monolithic switch is designed to control analog signals with a high degree of accuracy. The DG333A/333AL minimize measurement errors by offering low on-resistance ($25\text{-}\Omega$ typ), low leakage (20-pA typ) and low charge injection performance. The DG333AL features micro-power operation ($<1\text{-}\mu\text{W}$ typ). This is ideal for battery operated systems. Pin 15 is not connected on the DG333A.

An improved charge injection compensation design minimizes switching transients. These switches can handle up to $\pm 22\text{-V}$ signals and have an improved continuous current of $30\ \text{mA}$.

The DG333A/333AL is fabricated in Vishay Siliconix's proprietary HVSG-2 CMOS process, resulting in higher speed and lower power consumption. An epitaxial layer prevents latchup. Each switch conducts equally well in both directions when on. When off, they block voltages up to the power-supply levels.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE

Logic	SW1, 4, 5, 8 Normally Open	SW2, 3, 6, 7 Normally Closed
0	Off	On
1	On	Off

Logic "0" $\leq 0.8\ \text{V}$
Logic "1" $\geq 2.4\ \text{V}$

ORDERING INFORMATION

Temp Range	Package	Part Number
-40 to 85°C	20-Pin Plastic DIP	DG333ADJ
		DG333ALDJ
	20-Pin Wide-Body SOIC	DG333ADW
		DG333ALDW

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V–

V+ 44 V

GND 30 V

V+ to GND 30 V

Digital Inputs^a V_S, V_D (V–) –2 V to (V+) +2 V
or 30 mA, whichever occurs first

Current, Any Terminal 30 mA

Peak Current, S or D

(Pulsed at 1 ms, 10% duty cycle max) 100 mA

Storage Temperature –65 to 125°C

Power Dissipation (Package)^b

20-Pin Plastic DIP^c 890 mW

20-Pin Wide SOIC^d 800 mW

Notes:

a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC Board.

c. Derate 12 mW/°C above 75°C

d. Derate 10 mW/°C above 75°C

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

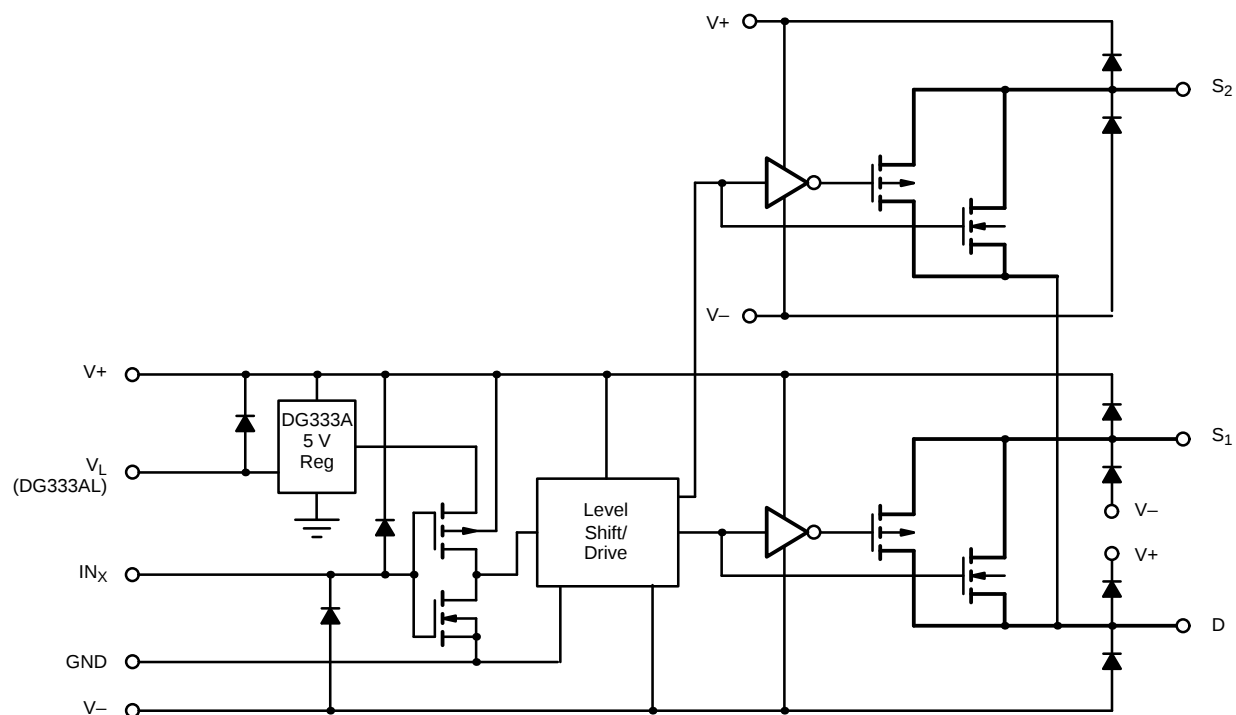


FIGURE 1.



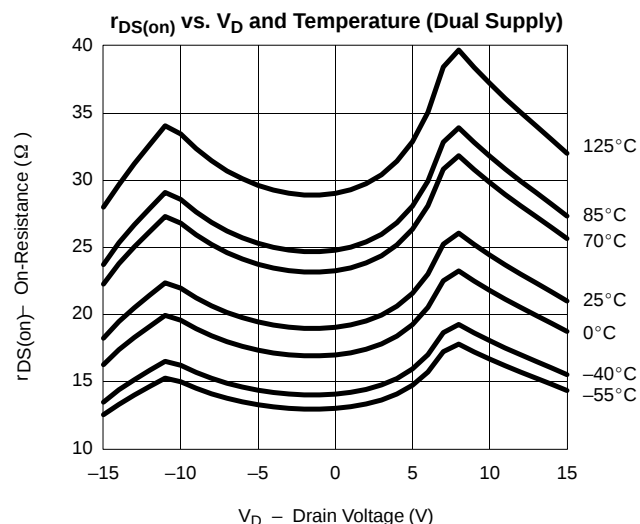
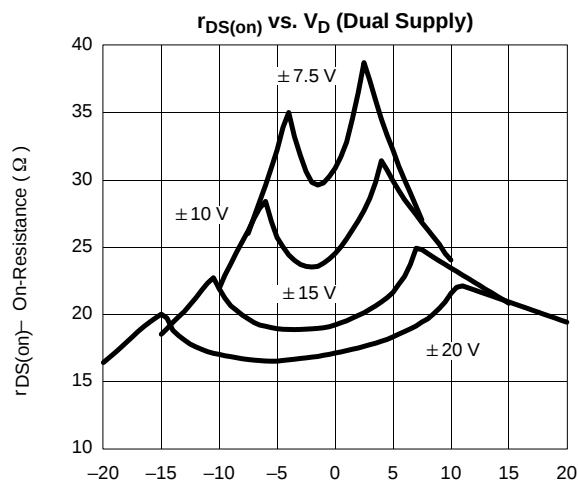
SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V VIN = 2.4 V, 0.8 V ^e	Limits D Suffix −40 to 85°C				Unit
			Temp ^a	Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	VANALOG		Full	V−		V+	V
Channel On-Resistance	rDS(on)	IS = −10 mA, VD = ±10 V	Room Full		25	45 90	Ω
On-Resistance Flatness		IS = −10 mA, VD = ±5 V V+ = 16.5 V, V− = −16.5 V	Room Full			3 5	
rDS(on) Match Between Channels ^f	ΔrDS(on)	IS = −10 mA, VD = ±10 V	Room Full			2 4	
Source Off Leakage Current	IS(off)	VD = ±15.5 V, VS = ∓15.5 V V+ = 16.5V, V− = −16.5 V	Room Hot	−0.25 −20		0.25 20	nA
Channel On Leakage Current	ID(on)	VD = ±15.5 V, VS(open) = ∓15.5 V V+ = 16.5V, V− = −16.5 V	Room Hot	−0.75 −60		0.75 60	
Digital Control							
Input Voltage High	VINH		Full	2.4			V
Input Voltage Low	VINL		Full			0.8	
Input Current	IINH or IINL	VINH or VINL	Full	−1		1	μA
Dynamic Characteristics							
Turn-On Time	tON	See Switching Time Test Circuit Figure 2	Room			175	ns
Turn-Off Time	tOFF		Room			145	
Break-Before-Make Time Delay	tD	See Figure 3	Room	5			
Charge Injection ^d	Q	CL = 10 nF, Vgen = 0 V, Rgen = 0 Ω	Room			10	pC
Off Isolation	OIRR	RL = 75 Ω, CL = 5 pF VD = 2.3 VRMS, f = 1 MHz	Room		72		dB
Channel-to-Channel Crosstalk	XTALK		Room		80		
Off Capacitance	COFF	f = 1 MHz, VS = 0 V	Room		8		pF
Channel On Capacitance	CON		Room		12		
Power Supplies							
Positive Supply Current	I+	DG333A: VIN = 0 or 5 V	Room			200	μA
Negative Supply Current	I−		Room	−1			
Positive Supply Current	I+	DG333AL: VIN = 0 or 5 V, VL = 5 V	Room			1	
Logic Supply Current	IL		Room			1	
Negative Supply Current	I−		Room	−1			
Supply Voltage Range	V+/V−		Full	±4		±22	V

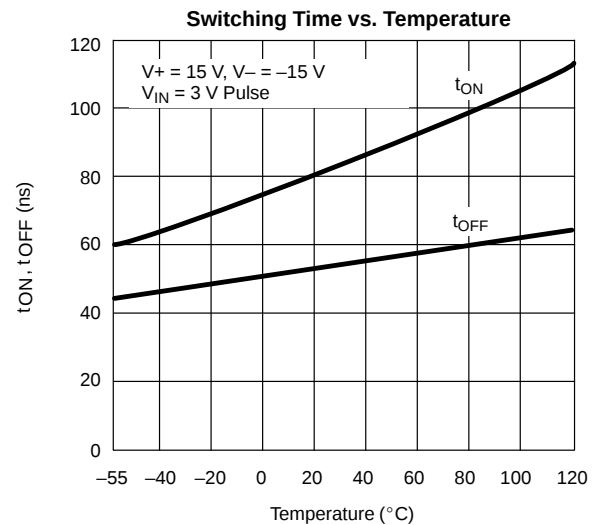
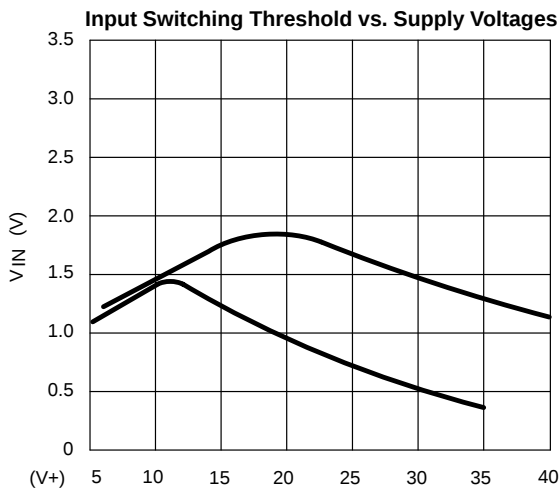
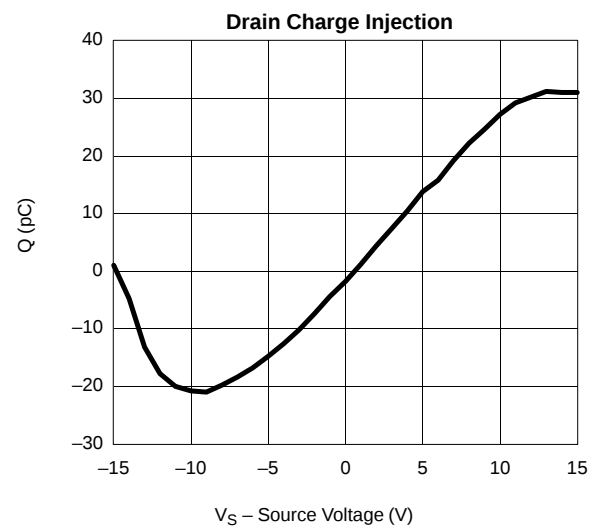
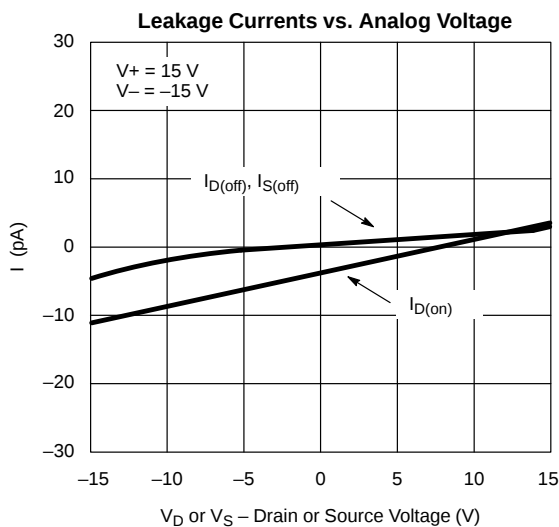
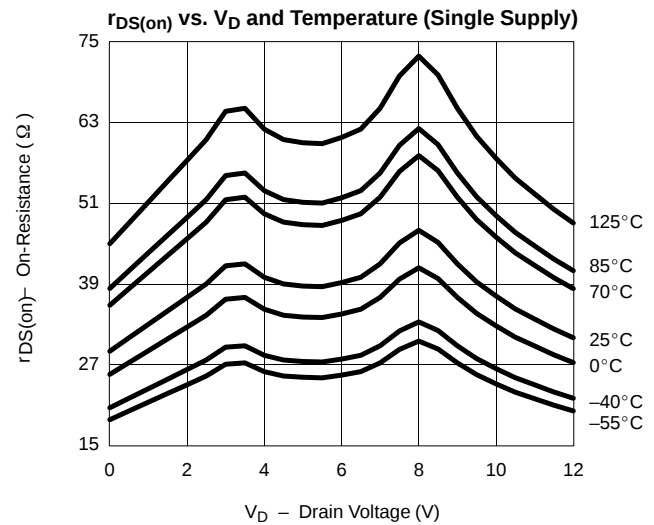
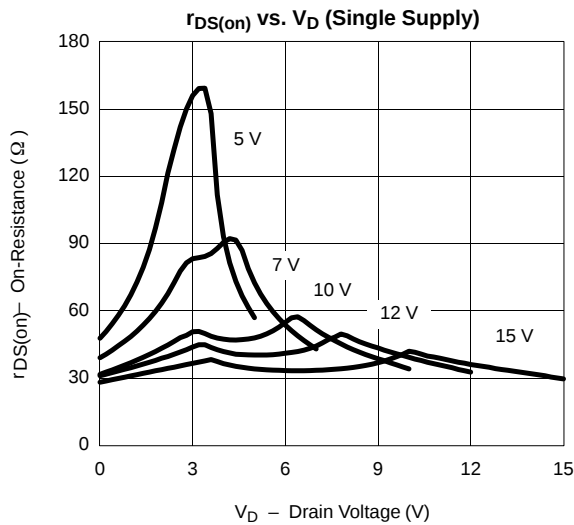
SPECIFICATIONS (UNIPOLAR SUPPLIES)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = −0 V TA = 25°C	Limits D Suffix −40 to 85°C				Unit
			Temp ^a	Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	VANALOG		Full	V−		V+	V
Channel On-Resistance	rDS(on)	IS = −10 mA, VD = 10, 1 V	Room		35	75	Ω
Source Off Leakage Current	IS(off)	VD = 11 V, VS(open) = 1 V	Room			0.25	nA
Channel On Leakage Current	ID(on)	VD = 11 V, VS(open) = 0 V VD = 1 V, VS(open) = V+	Room			0.75	
Dynamic Characteristics							
Turn-On Time	tON	See Switching Times Test Circuit Figure 2	Room		90		ns
Turn-Off Time	tOFF		Room		45		
Break-Before-Make Time Delay	tD	See Figure 3	Room	5	10		
Power Supplies							
Positive Supply Current	I+	DG333A: VIN = 0 or 5 V	Room			200	μA
			Room			1	
Positive Supply Current	I+	DG333AL: VIN = 0 or 5 V, VL = 5 V	Room			1	
Logic Supply Current	IL		Room			1	
Positive Supply Range	V+		Room	5		40	V

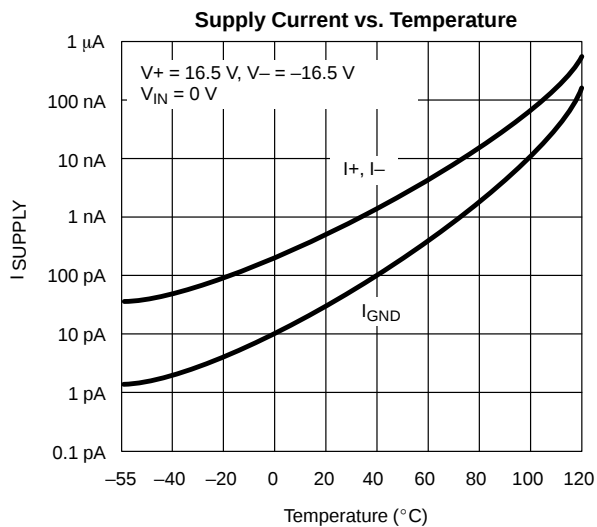
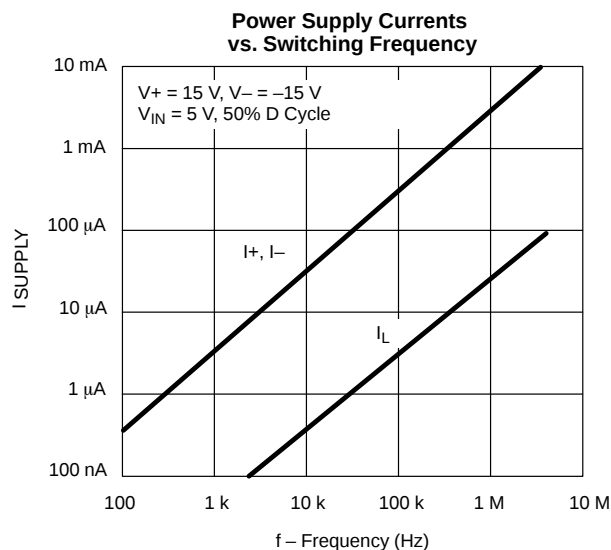
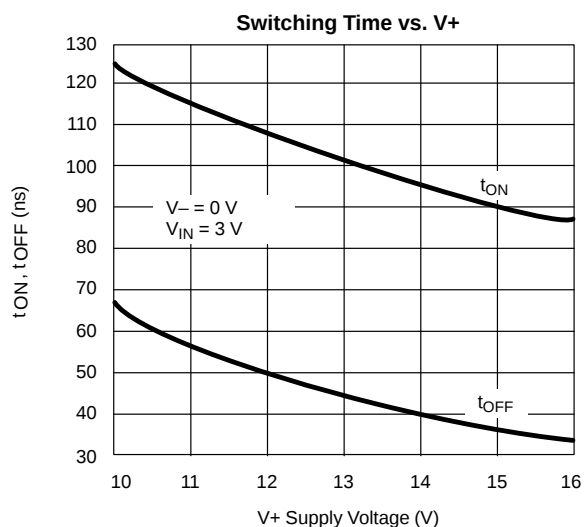
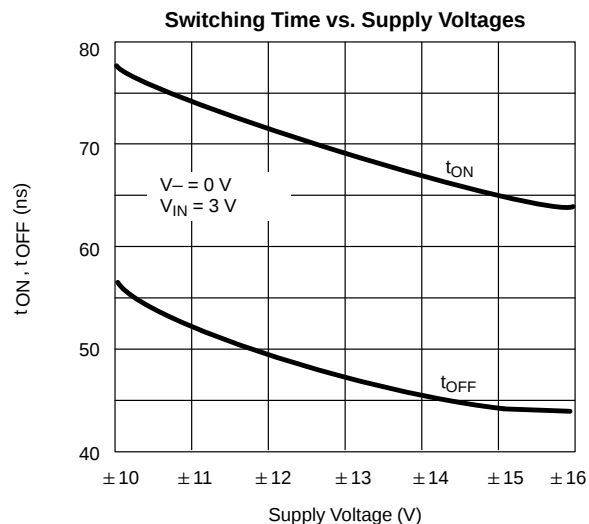
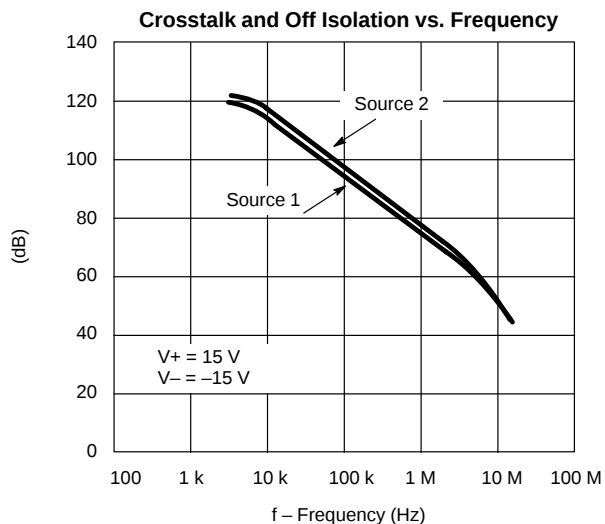
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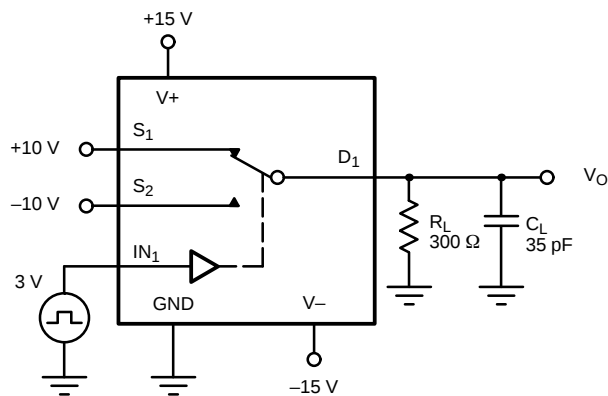
- Room = 25°C , Full = as determined by the operating temperature suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.
- On-resistance match and flatness are guaranteed only for bipolar supply operation.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

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TEST CIRCUITS


Repeat Test for IN₂, IN₃ and IN₄

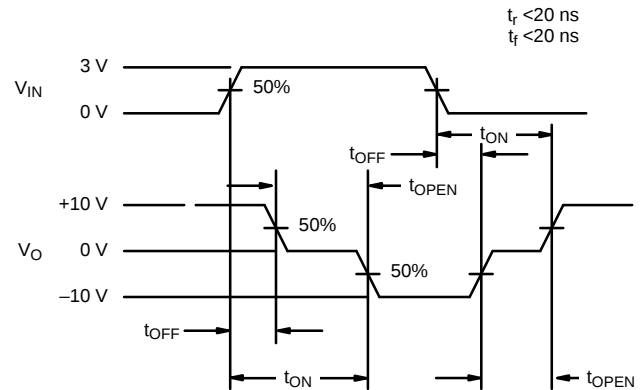
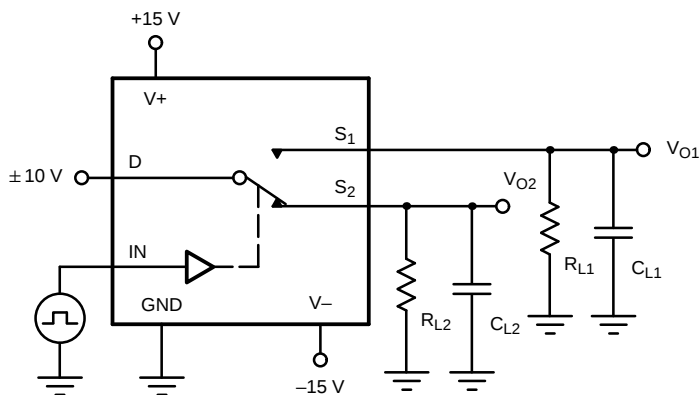


FIGURE 2. Switching Times



$R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$
 C_L (includes fixture and stray capacitance)

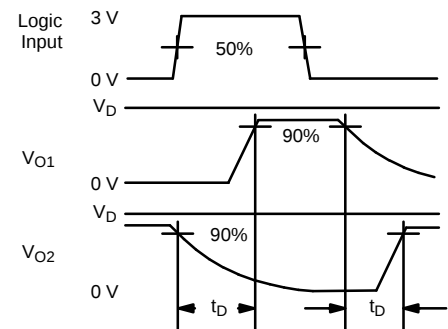


FIGURE 3. Break-Before-Make

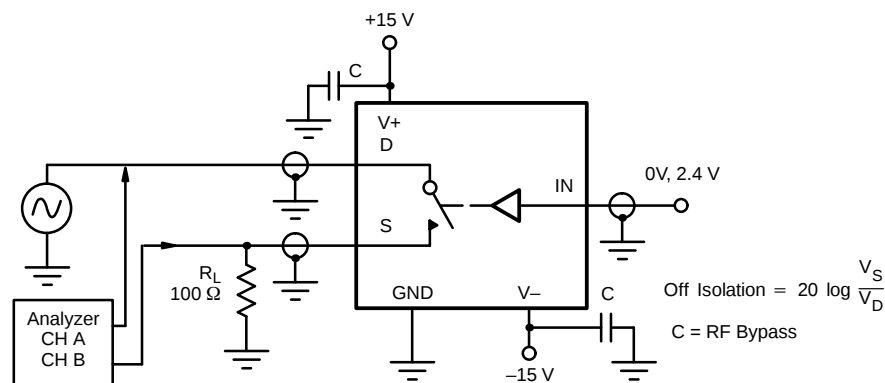


FIGURE 4. Off Isolation

TEST CIRCUITS

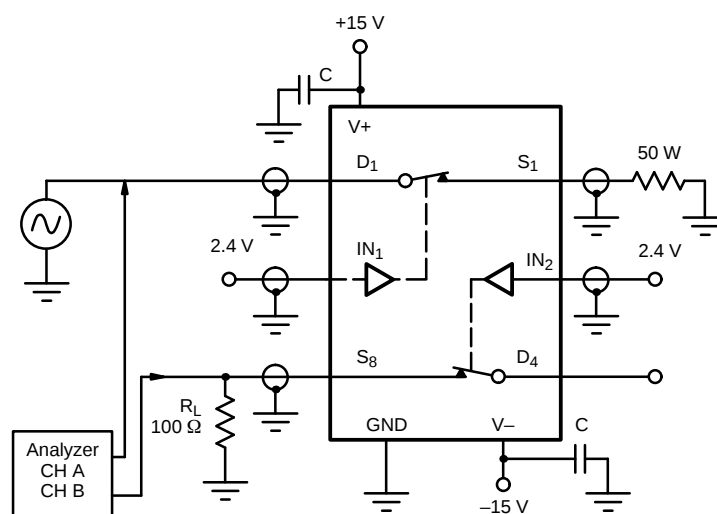


FIGURE 5. Crosstalk

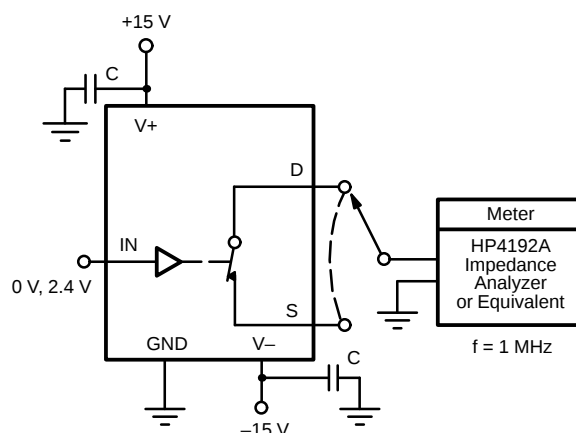


FIGURE 6. Capacitances

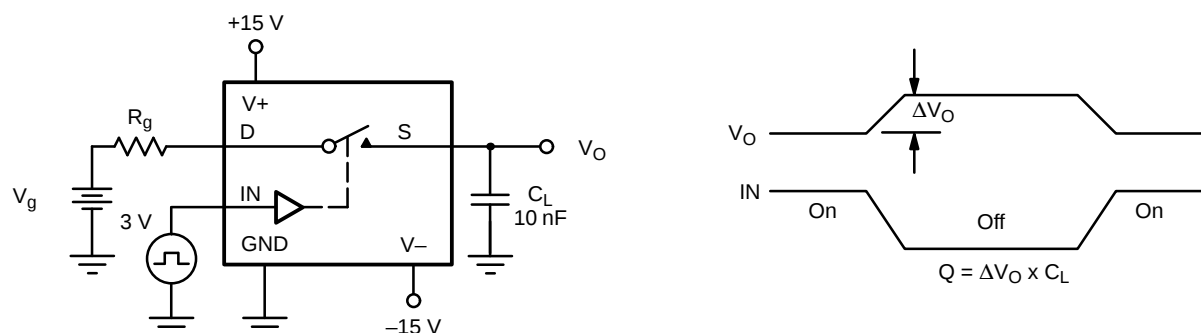


FIGURE 7. Charge Injection

Band-Pass Switched Capacitor Filter

clock rates and consequently higher filter operating frequencies. Figure 8 shows two capacitors being switched. The DG333A/333AL is capable of switching four capacitors.

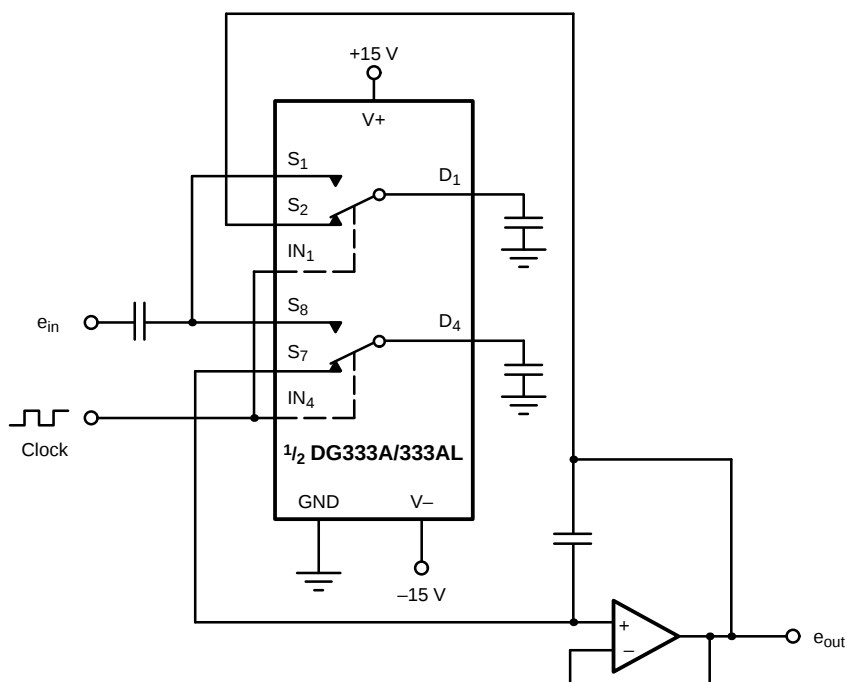


FIGURE 8. Band-Pass Switched Capacitor Filter