DG243

General Purpose Monolithic Dual SPDT CMOS Analog Switch

Features

- PLUS-40 Process
- Make-Before-Break Operation
- Full Rail-to-Rail Analog Signal Range
- True TTL Compatibility
- Low $r_{DS(on)}$: 30 Ω

Benefits

- Low Power
- Reduced Switching Noise
- Reduced Need for Buffers

Applications

- Programmable Gain Amplifiers
- Analog Multiplexing
- Servo Control Systems
- Programmable Filters
- Audio Switching

Description

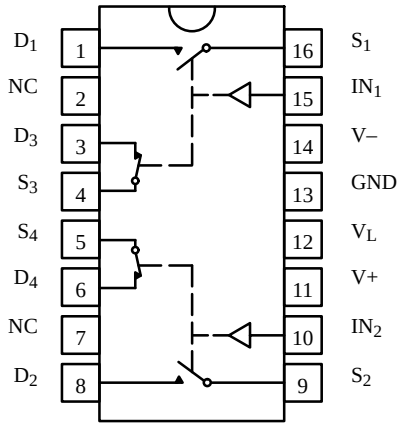
The DG243 is a monolithic dual SPDT analog switch designed for general switching applications in communication, instrumentation, and process control systems. Featuring make-before-break action, the DG243 is used in closed loop systems to switch gain or bandwidth networks without opening the loop.

The DG243 is designed on the Siliconix PLUS-40 CMOS process to combine low power dissipation with a high breakdown voltage rating of 44 V. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off.

Functional Block Diagram and Pin Configuration

Dual-In-Line



Top View

Truth Table

Logic	SW_1, SW_2	SW_3, SW_4
0	OFF	ON
1	ON	OFF

Logic “0” ≤ 0.8 V
Logic “1” ≥ 2.0 V

Ordering Information

Temp Range	Package	Part Number
0°C to 70°C	16-Pin Plastic DIP	DG243CJ

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70042.

Absolute Maximum Ratings

V+ to V– . . . . . 44 V
GND to V– . . . . . 25 V
V_L . . . . . (GND – 0.3 V) to 44 V
Digital Inputs[a] V_S, V_D . . . . . (V–) –2 V to (V+ plus 2 V) or 30 mA, whichever occurs first
Current (Any Terminal) Continuous . . . . . 30 mA
Current, S or D (Pulsed 1 ms 10% duty) . . . . . 100 mA
Storage Temperature . . . . . –65 to 125°C

Power Dissipation (Package)b
16-Pin Plastic DIP[c] . . . . . 450 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V V_L = 5 V, V_{IN} = 2.0 V, 0.8 V[e]	Temp[a]	C Suffix 0 to 70°C Min[c]	 Typ[b]	 Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	–15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = –10 mA, V_D = ± 10 V	Room Full		30	50 75	Ω
Switch Off Leakage Current	$I_{S(off)}$	V_D = ± 14 V, V_S = ∓ 14 V	Room Full	–1 –100	± 0.3	1 100	nA
	$I_{D(off)}$		Room Full	–1 –100	± 0.3	1 100	
Channel On Leakage Current	$I_{D(on)}$	V_D = V_S = ± 14 V	Room Full	–2 –200	± 0.5	2 200	
Digital Control							
Input Current with V_{IN} Low	I_{IL}	V_{IN}= 0.8 V	Full	–1	–0.005	1	µA
Input Current with V_{IN} High	I_{IH}	V_{IN}= 2.0 V	Full	–1	–0.01	1	
Dynamic Characteristics							
Turn-On Time	t_{ON}	R_L = 1 kΩ , C_L = 35 pF, See Figure 2	Room		250	700	ns
Turn-Off Time	t_{OFF}		Room		390	1200	
Charge Injection	Q	C_L = 1000 pF, V_{GEN} = 0 V R_{GEN} = 0 Ω	Room		60		pC
Off Isolation Reject Ratio	OIRR	R_L = 75 Ω , f = 1 MHz	Room		75		dB
Crosstalk (Channel-to-Channel)	X_{TALK}		Room		89		
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 0 V	Room		15		pF
Drain-Off Capacitance	$C_{D(off)}$		Room		17		
Channel-On Capacitance	$C_{D + S (on)}$		Room		45		
Power Supplies							
Positive Supply Current	I+	All Channels On or Off	Room		180	300	µA
Negative Supply Current	I–		Room	–300	–150		
Logic Supply Current	I_L		Room		100	300	
Ground Current	I_{GND}		Room	–300	–140		

Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

Schematic Diagram (Typical Channel)

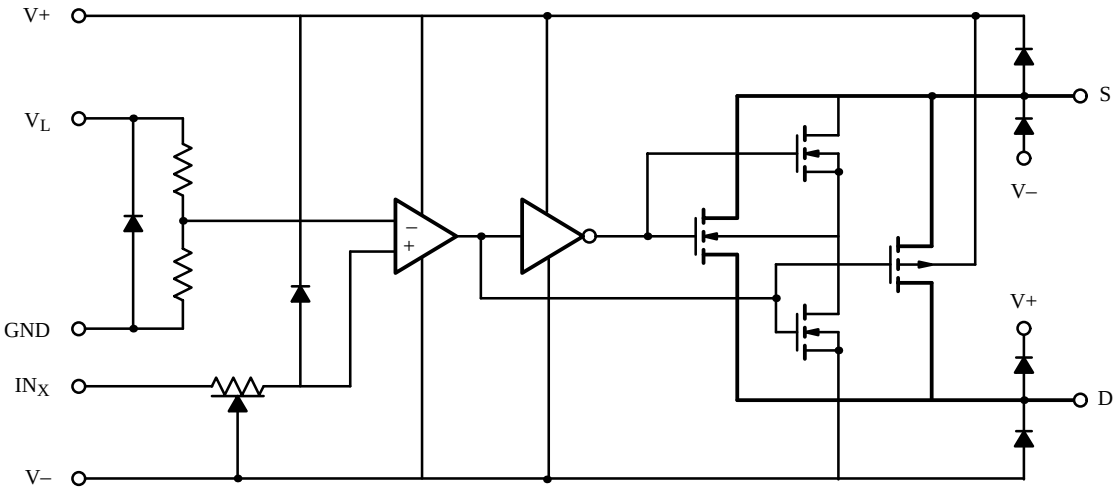
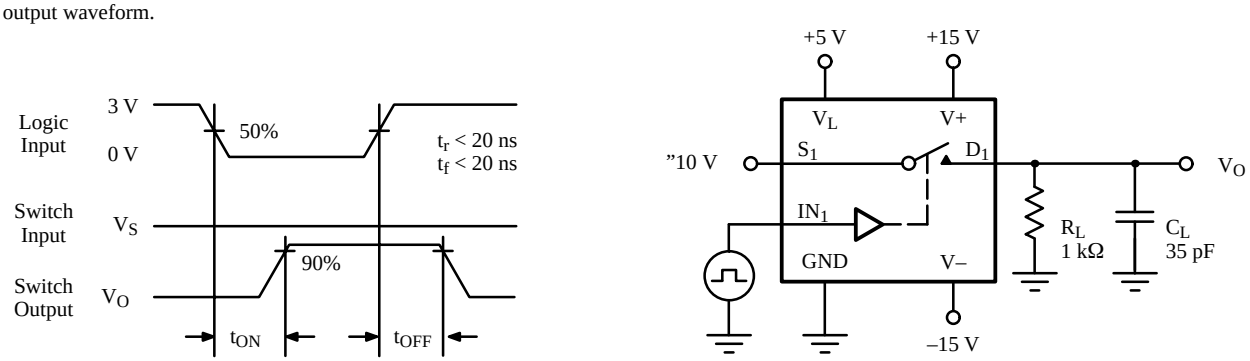


Figure 1.

Test Circuits

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Figure 2. Switching Time

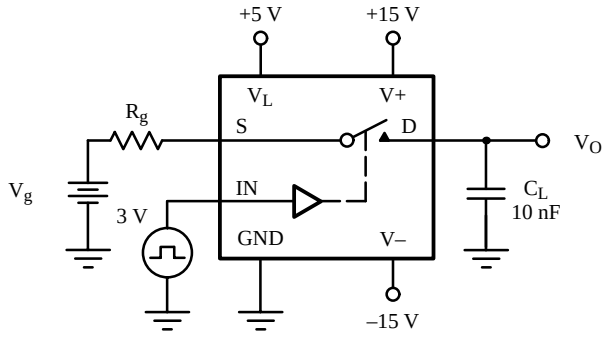


Figure 3. Charge Injection

Applications

The make-before-break operation of the DG243 provides simple transient suppression in these two important applications.

Figure 3 shows a minimum amount of glitching during changes of gain states. The relatively low impedance of the gain setting resistors (10 kΩ , 1 kΩ , and 100 Ω) shunt the injected charge-to-ground minimizing transient effects occurring at the inverting input of the op amp. Consequently, these transients are not amplified to V_{OUT}.

Figure 4 takes advantage of the make-before-break operation of the DG243 by shorting transition current to real ground instead of virtual ground. The best results are obtained by selecting an op amp with the proper offset voltage specification.

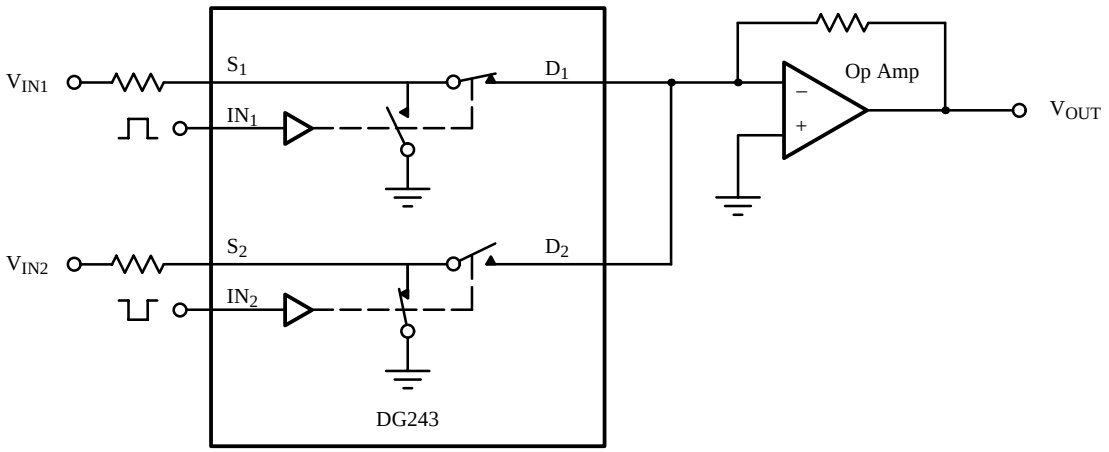


Figure 4. Minimizing Glitches in Audio Switching

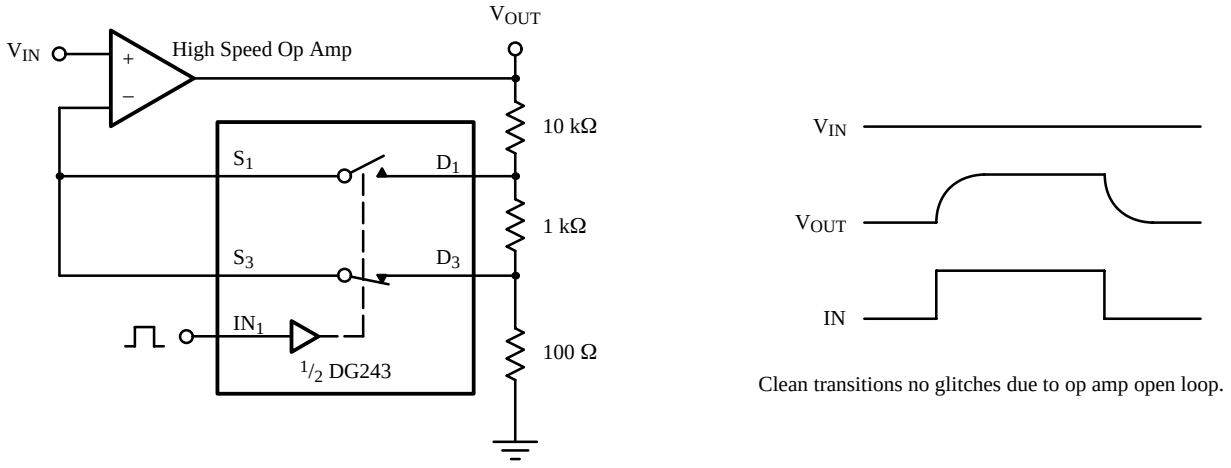


Figure 5. Make-Before-Break Improves Transient Response in Programmable Gain Amplifiers