DEVICE
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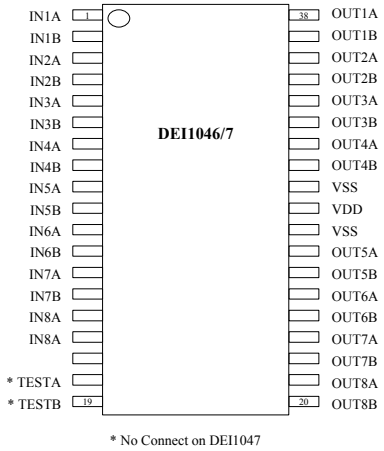
DEI1046, DEI1047
OCTAL ARINC 429 LINE RECEIVER

FEATURES

- Eight channel ARINC 429 to TTL/CMOS logic line receivers
- Operates from single +5V ± 10% or 3.3V ± 10% power supply
- ARINC inputs internally protected to lightning requirements of DO-160D Level A3
- Operates in high noise environment
  - Input Common Voltage Range: ± 20V
  - 2V minimum Input hysteresis
- Optional logic level TEST inputs on DEI1046.
- 38 lead TSSOP package, 4.4mm body.

PINOUT



* No Connect on DEI1047

Table 1 PIN DESCRIPTION

PIN	NAME	DESCRIPTION
15,13,11, 9,7,5,3,1	**IN[8:1]A**	**429 INPUTS.** ARINC 429 format serial digital data "A" inputs.
16,14,12, 10,8,6,4,2	**IN[8:1]B**	**429 INPUTS.** ARINC 429 format serial digital data "B" inputs.
18	**TESTA**	**LOGIC INPUT.** Test input A on DEI1046. No Connect on DEI1047.
19	**TESTB**	**LOGIC INPUT.** Test input B on DEI1046. No Connect on DEI1047.
21,23,25,27, 32,34,36,38	**OUT[8:1]A**	**LOGIC OUTPUTS.** CMOS/TTL format serial digital data "A" outputs.
20,22,24,26, 31,33,35,37	**OUT[8:1]B**	**LOGIC OUTPUTS.** CMOS/TTL format serial digital data "B" outputs.
29	**VDD**	**POWER INPUT.** 5 VDC OR 3.3VDC.
28, 30	**VSS**	**POWER INPUT.** Ground.

FUNCTIONAL DESCRIPTION

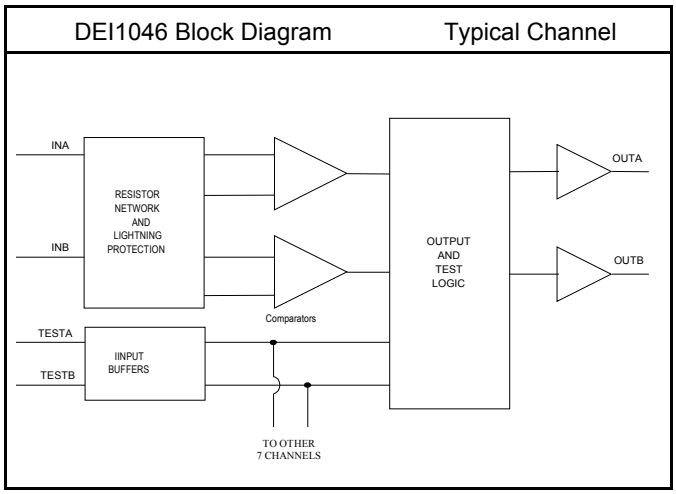
The DEI1046/7 is a BICMOS device which contains eight differential line receivers. Each receiver channel translates incoming ARINC 429 data bus signals (tri-level RZ bipolar differential modulation) to a pair of TTL/CMOS logic outputs. Each channel operates independently and meets the requirements of the ARINC 429 Digital Information Transfer Standard. Refer to Figure 1 " DEI1046/7 Block Diagram and Truth Table". Note: Test inputs are not implemented on the DEI1047. They are internally connected to logic 0.

The device is designed to operate in a high noise environment. Inputs are accepted over a +/- 20V common mode voltage range and the receivers provide over 2 Volts of hysteresis. Circuit speed is optimized to reject high frequency transients.

All ARINC input pins are designed with internal protection from damage due to transients meeting the lightning induced transient requirements of DO-160D Level A3.

The DEI1046 device provides logic level TEST inputs for built in system test. They force the outputs of all eight receivers to the specified ZERO, ONE or NULL state. The ARINC inputs are ignored when the device is in test mode.

The DEI1047 does not support the built in system test function. A metal mask option removes all test input logic to maximize channel isolation.



DEI1046 Truth Table					
INPUTS			OUTPUTS		
TEST INPUTS (TTL/CMOS)		ARINC INPUTS	TTL/CMOS		
TEST A	TEST B	$A_{IN} - B_{IN}$ V	OUT A	OUT B	Logic
0	0	Logic +1	1	0	ONE
0	0	Logic -1	0	1	ZERO
0	0	NULL	0	0	NULL
0	1	X	0	1	ZERO
1	0	X	1	0	ONE
1	1	X	0	0	NULL

Note: Test inputs are not implemented on DEI1047. They are internally connected to logic 0.

Figure 1 DEI1046/7 Block Diagram and Truth Table

ELECTRICAL DESCRIPTION

Table 1 Absolute Maximum Rating

PARAMETER	MIN	MAX	UNITS
Supply Voltage (with respect to V_{SS})	-0.3	7.0	V
Operating Frequency		155	KHz
Operating Temperature	-55	+85	°C
Storage Temperature	-65	+150	°C
Input Voltage, continuous (ARINC Inputs)	-40	+40	V
Input Voltage (Test Inputs)	V_{SS} – 0.3	V_{DD}+0.3	V

PARAMETER	MIN	MAX	UNITS
Power Dissipation @ 85 °C		800	mW
Junction Temperature: Tjmax, (limited by molding compound Tg)		145	°C
Lead Soldering Temperature (10 sec duration)		280	°C
Lightning Protection (ARINC 429 Channel Inputs and TESTA/TESTB Inputs) Waveform 3* Waveform 4 and 5* *Per DO160D level 3A. See Figures 4-6.	 -600 -300	 +600 +300	 V V
ESD per JEDEC A114-A Human Body Model		2000	V
Caution: Stresses above these limits can cause permanent damage.			

Table 2 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	Vdd	+5V ± 10% +3.3V ± 10%
Logic Input Levels	$V_{TESTA,B}$	0 to Vdd

Table 3 Electrical Characteristics

Conditions: Temperature: -55°C to +85°C; V_{DD} = +5V ± 10% or 3.3V ± 10%						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN**	**NOM**	**MAX**	**UNITS**
ARINC INPUTS						
$V_A - V_B$ = Logic +1	OUTA = 1	V_{+1}	6.5	10	13	V
$V_A - V_B$ = Logic -1	OUTB = 1	V_{-1}	-6.5	-10	-13	V
$V_A - V_B$ = Logic Null	OUTA = 0 OUTB = 0	V_{NULL}	-2.5	0	2.5	V
Input Hysteresis		V_{HY}	2.0		4.0	V
$V_A - V_B$ = Null to +1 transition	OUTA = 0→1	V_{T+1+}	5.5		6.5	V
$V_A - V_B$ = +1 to Null transition	OUTA = 1→0	V_{T+1-}	2.5		3.5	V
$V_A - V_B$ = Null to -1 transition	OUTB = 0→1	V_{T-1+}	-6.5		-5.5	V
$V_A - V_B$ = -1 to Null transition	OUTB = 1→0	V_{T-1-}	-3.5		-2.5	V
Input Common Mode Voltage Range	Logic +1, Null, Logic -1	V_{CM}	-20		+20	V
Input Resistance IN_A to IN_B	V_{DD} open, Shorted to V_{SS} or +5V	R_{IN}	12k			Ω
Input Resistance IN_A or IN_B to V_{SS}	V_{DD} open, Shorted to V_{SS} or +5V	R_S	12k			Ω
Input Capacitance IN_A to IN_B	V_{DD} open, Shorted to V_{SS} or +5V	C_{IN}			50	pF

Conditions: Temperature: -55°C to +85°C; V_{DD} = +5V ± 10% or 3.3V ± 10%						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN**	**NOM**	**MAX**	**UNITS**
Input Capacitance IN_A or IN_B to V_{SS}	V_{DD} open, Shorted to V_{SS} or +5V	C_S			50	pF
TEST INPUTS						
Logic 0 Voltage		V_{IL}			0.8	V
Logic 1 Voltage		V_{IH}	2.0			V
Logic 0 Current	V_{IL} = 0.8	I_{IL}			1	µA
Logic 1 Current	V_{IH} = 2.0	I_{IH}			20	µA
LOGIC OUTPUTS						
OUT A or OUT B	I_{OH} = 5mA (5V Vdd) I_{OH} = 1.5mA (3.3V Vdd) TTL Compatible	V_{OH}	2.4			V
OUT A or OUT B	I_{OL} = 5mA (5V Vdd) I_{OL} = 1.5mA (3.3V Vdd) TTL Compatible	V_{OL}			0.4	V
OUT A or OUT B	I_{OH} = 100µA CMOS Compatible	V_{OH}	V_{DD} – 50mV			V
OUT A or OUT B	I_{OL} = 100µA CMOS Compatible	V_{OH}			V_{SS} + 50mV	V
SUPPLY CURRENT						
V_{DD} Current	Data Rate = 0MHz, A/BIN =open, A/BOUT=open, Vdd = 5.5V or 3.63V	I_{DD}		20		mA

Table 4 Switching Characteristics

PARAMETER	**TEST CONDITION**	**SYMBOL**	**MAX**	**MAX**	**UNITS**
			Vdd 3.3V	Vdd 5V	
INA/B to OUT A/B Prop Delay	TESTA = TESTB = 0 C_L = 50pF	t_{LH}	300	200	nsec
INA/B to OUT A/B Prop Delay	TESTA = TESTB = 0 C_L = 50pF	T_{HL}	300	200	nsec
OUT A/B rise time	10% to 90%, C_L = 50pF	t_r	50	25	nsec
OUT A/B fall time	10% to 90%, C_L = 50pF	t_f	50	25	nsec
TESTA/B to OUTA/B Prop delay	C_L = 50pF	t_{TOH}	100	60	nsec
TESTA/B to OUTA/B Prop delay	C_L = 50pF	t_{TOL}	100	60	nsec

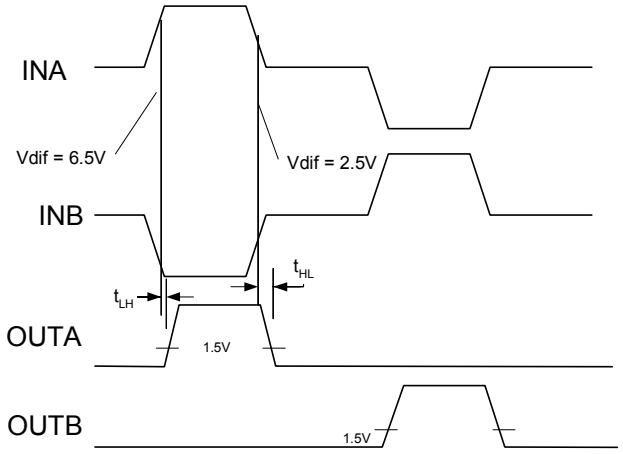


Figure 2 ARINC 429 Input to Logic Output Switching Waveform

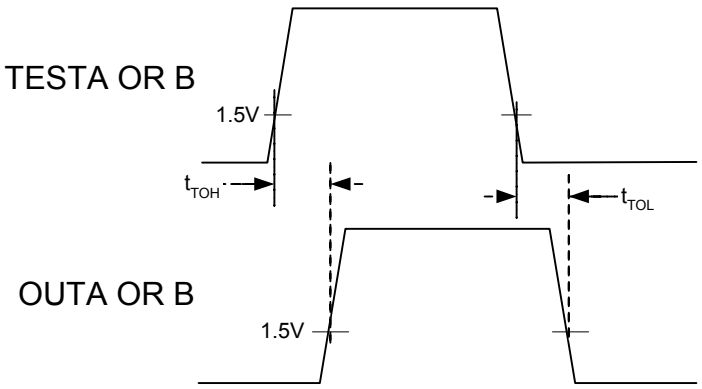


Figure 3 TEST Input to Logic Output Switching Waveform

LIGHTNING TRANSIENT NOTES:

1. Voc = Peak Open Circuit Voltage available at the calibration point.
2. Isc = Peak Short Circuit Current available at the calibration point.
3. Amplitude tolerances: +10%, -0%.
4. The ratio of Voc to Isc is the generator source impedance to be used for generating the waveforms.

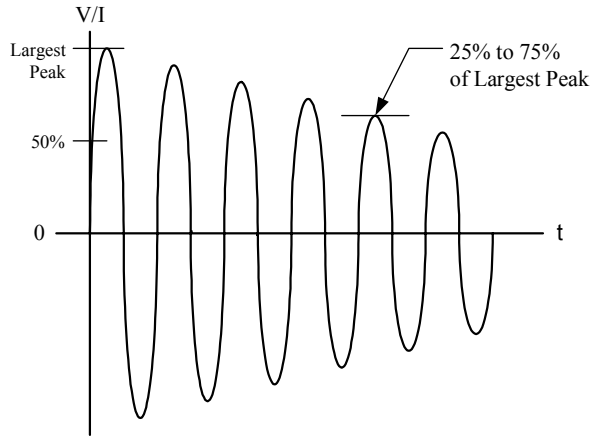


Figure 4 DO160D Lightning Induced Transient Voltage Waveform #3.
Voc = 600V, Isc = 24A, Frequency =1MHz +-20%

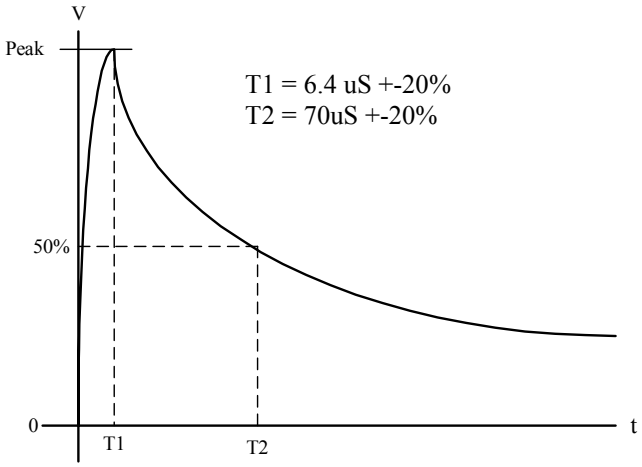


Figure 5 DO160D Lightning Induced Transient Voltage Waveform #4.
Voc = 300V, Isc = 60A

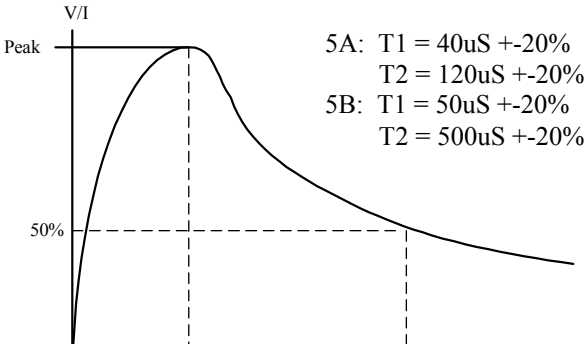


Figure 6 DO160D Lightning Induced Transient Voltage Waveform #5.
Voc = 300V, Isc = 300A

PACKAGE DESCRIPTION

38 Lead TSSOP

Table 5 38 Lead TSSOP Characteristics

SYMBOL	DESCRIPTION	VALUE	UNITS
$Theta_{jc}$	Junction to Case	15	°C/W
$Theta_{ja}$	Junction to Ambient. 4 layer board with 2 internal power planes.	75	°C/W
MSL	JEDEC Moisture Sensitivity Level	2	-

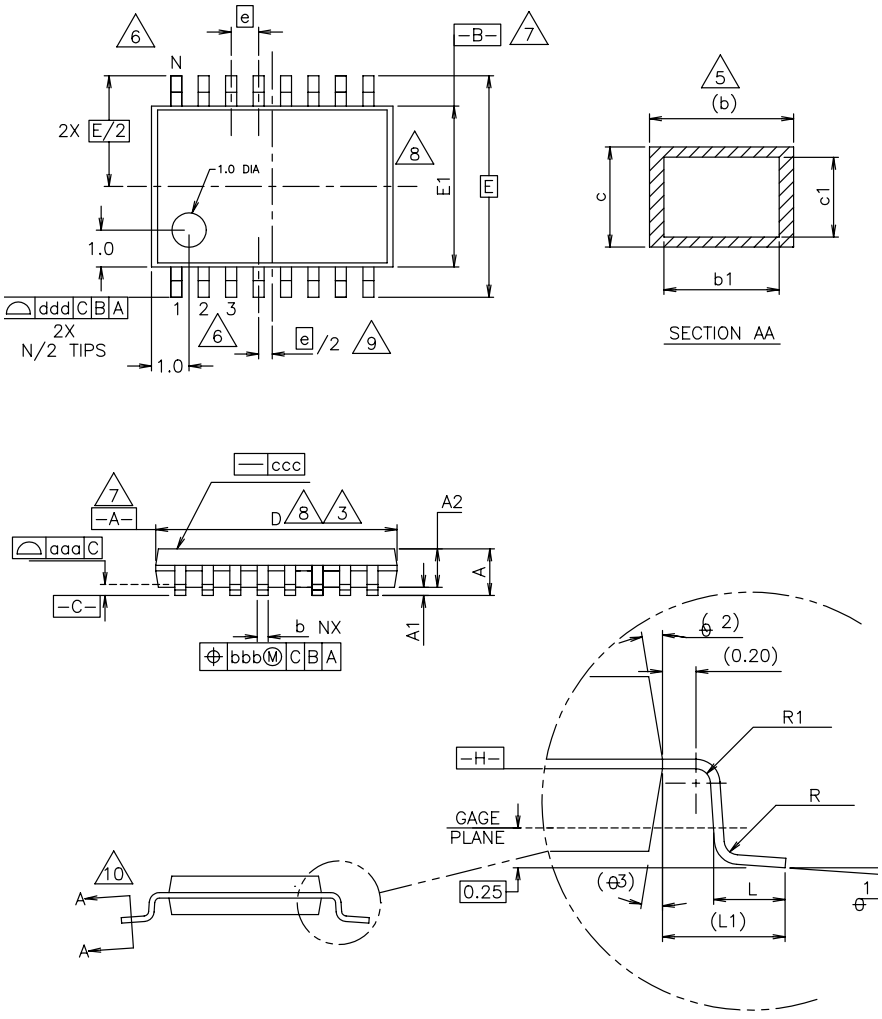


Figure 7 TSSOP Mechanical Outline

SYMBOL	COMMON DIMENSION(MILLIMETERS)							
	0.65mm LEAD PITCH			NOTE	0.50mm LEAD PITCH			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX	
A	---	---	1.10	---	---	---	1.10	---
A1	0.05	---	0.15	---	0.05	---	0.15	---
A2	0.85	0.90	0.95	---	0.85	0.90	0.95	---
L	0.50	0.60	0.75	---	0.45	0.60	0.75	---
R	0.09	---	---	---	0.09	---	---	---
R1	0.09	---	---	---	0.09	---	---	---
b	0.19	---	0.30	5	0.17	---	0.27	5
b1	0.19	0.22	0.25	---	0.17	0.20	0.23	---
c	0.09	---	0.20	---	0.09	---	0.20	---
c1	0.09	---	0.16	---	0.09	---	0.16	---
θ1	0°	---	8°	---	0°	---	8°	---
L1	1.0 REF			---	1.0 REF			---
aaa	0.10			---	0.10			---
bbb	0.10			---	0.08			---
ccc	0.05			---	0.05			---
ddd	0.20			---	0.20			---
e	0.65 BSC			---	0.50 BSC			---
θ2	12° REF			---	12° REF			---
θ3	12° REF			---	12° REF			---
NOTE	1,2				1,2			
ISSUE	A				A			

SYMBOL	NJR 1			NOTE
	MIN	NOM	MAX	
D	9.60	9.70	9.80	3,8
E1	4.30	4.40	4.50	4,8
E	6.4 BSC			
e	0.50 BSC			
N	38			6
NOTE	1,2,11			
ISSUE	---			

Figure 8 38 Lead TSSOP Dimensions

JEDEC Reference MO-153-BD-1

ORDERING INFORMATION

DEI PN	TEST INPUTS	TEMPERATURE RANGE	PACKAGE TYPE
DEI1046-TES	YES	-55/+85 ºC	38 lead TSSOP
DEI1047-TES	NO	-55/+85 ºC	38 lead TSSOP