DEVICE
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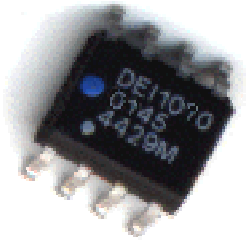
DEI1070, DEI1071, DEI1072
ARINC 429 LINE DRIVER WITH RATE SELECT

FEATURES

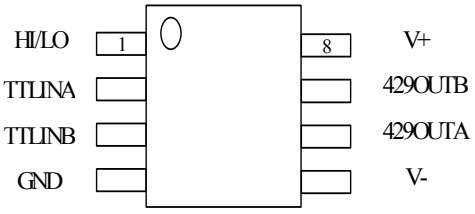
- TTL/CMOS TO ARINC 429 Line Driver.
- Rate control input set Hi (100KBS) or Lo (12.5KBS) speed slew rates.
- Operates from ±9.5V to ±16.5V power supply.
- Drives full ARINC load.
- Output resistor options: 0, 10 or 37.5 Ohms.
- CERDIP and thermally enhanced 8 lead SOIC package.
- Outputs Short Circuit Protected.



GENERAL DESCRIPTION

The DEI107[0/1/2] family of 8 pin BiCMOS integrated circuits are line drivers designed to directly drive the ARINC 429 avionics serial digital data bus. The device converts TTL/CMOS serial input data to the tri-level RZ bipolar differential modulation format of the ARINC bus. A TTL/CMOS control input selects the output slew rate for HI (100KBS) and LOW (12.5KBS) speed operation. No external timing capacitors are required.

The DEI1070 has internal 37.5 Ohm output resistors, the DEI1071 has 10 Ohm resistors, and the DEI1072 has none. The 10 and 0 Ohm options require external series resistors which are typically used to implement a transient voltage protection network.



Note: SOIC heatsink pad is V-

Table 1 PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	HI/LO	**LOGIC INPUT.** Slew rate control. 1 = Hi speed. 0 = Low speed.
2	TTLINA	**LOGIC INPUT.** Serial digital data input A.
3	TTLINB	**LOGIC INPUT.** Serial digital data input B.
4	GND	**POWER INPUT.** Ground.
5	V-	**POWER INPUT.** –9.5 to –16.5 VDC
6	420OUTA	**429 OUTPUT.** ARINC 429 format serial digital data output A.
7	429OUTB	**429 OUTPUT.** ARINC 429 format serial digital data output B.
8	V+	**POWER INPUT.** +9.5 to +16.5 VDC.

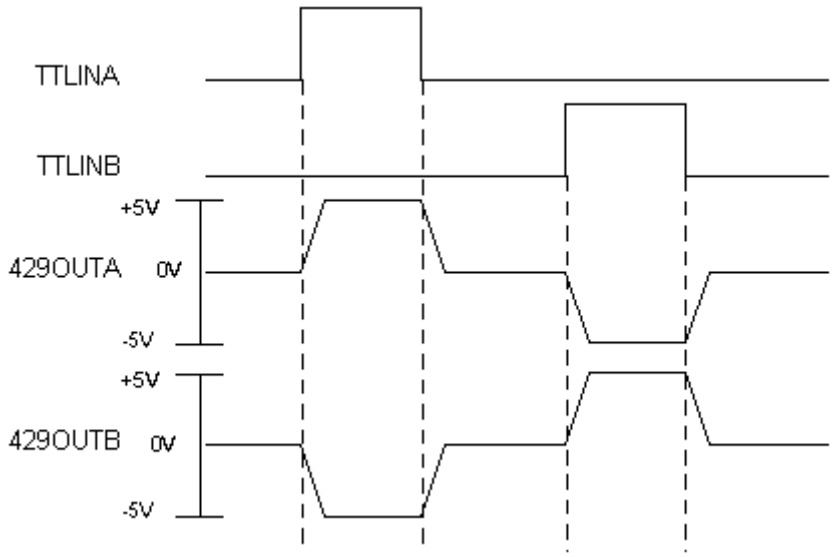
FUNCTIONAL DESCRIPTION

Table 2 Speed Control Truth Table

HILO	OUTPUT TRANSITION TIME
0	10uS (12.5 KBS data)
1	1.5uS (100KBS data)

Table 3 Transmit Data Truth Table

TTLINA	TTLINB	429OUTA	429OUTB	NOTES
0	0	0V	0V	Null output
0	1	-5V	5V	zero (-1) output
1	0	5V	-5V	One (+1) output
1	1	0V	0V	Undefined.



LINE DRIVER WAVEFORMS

Output Circuit Protection:
The device is protected against one or both outputs shorted to Ground and against both outputs shorted together while the device is operating continuously at 100% duty cycle.

ELECTRICAL DESCRIPTION

Table 4 Absolute Maximum Ratings

PARAMETER Voltages referenced to Ground	MIN	MAX	UNITS
V+ Supply Voltage	-0.3	+20	V
V1- Supply Voltage	0.3	-20	V
Operating Temperature Plastic Package Ceramic Packages	 -55 -55	 +85 +125	 °C
Storage Temperature	-65	+150	°C
Input Voltage TTLIN and HI/LO Inputs 429OUT Outputs	 V_{SS} – 0.3 V_- – 0.3	 V_+ +0.3 V_+ +0.3	 V V
Power Dissipation @ 85 °C: (> 10 Sec) 8 Lead EQ SOIC, thermal pad soldered to heat spreader land		 0.8	 W
Junction Temperature: Tjmax, Plastic Packages (Limited by molding compound Tg) Tjmax, Ceramic Packages		 145 175	 °C °C
ESD per JEDEC A114-A Human Body Model		2000	V
Lead Soldering Temperature (10 sec duration)		280	°C
Notes: Stresses above absolute maximum ratings may cause permanent damage to the device.			

Table 5 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	V+ V-	9.5 to 16.5V -9.5 to –16.5V

Table 6 Electrical Characteristics

Conditions: Temperature: -55°C to +85°C for plastic, -55°C to +125°C for ceramic, V+/- = +/-9.5 to +/-16.5V Unless otherwise noted.

PARAMETER	TEST CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
LOGIC INPUTS						
Input Voltage, Logic 1		V_{IH}	2.0		V+	V
Input Voltage, Logic 0		V_{IL}	-0.3		0.8	V
Input Current, Logic 1	VIN = 5.0V	I_{IH}	0		100	uA
Input Current, Logic 0	VIN = 0.0V	I_{IL}	0		-100	uA
ARINC OUTPUTS						

Conditions: Temperature: -55°C to +85°C for plastic, -55°C to +125°C for ceramic, V+/- = +/-9.5 to +/-16.5V Unless otherwise noted.						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN**	**NOM**	**MAX**	**UNITS**
ARINC Output Voltage (Differential) One (+1) Null (null) Zero (-1)	Differential Output Voltage = 429OUTA – 429OUTB. No Load.	 V_{DIF+1} $V_{DIFnull}$ V_{DIF-1}	 9.0 -0.5 -9.0	 10.0 0 -10.0	 11.0 +0.5 -11.0	 V V V
ARINC Output Voltage (Ref erenced to Gnd) OUTA +1, OUTB –1 Null (null) Zero (-1)	No Load.	 Vo_{A+1} Vo_{B-1} Vo_{Anull} Vo_{B-null} Vo_{A-1} Vo_{B+1}	 4.5 -0.5 -0.5 -5.5	 5.0 0 0 -5.0	 5.5 +0.5 +0.5 -4.5	 V V V V
ARINC Output Short Circuit Current, peak OUTA+1, OUTB-1 OUTA-1, OUTB+1	Outputs shorted to Ground. Continuous current may be reduced by thermal cutoff or signal transition boost cutoff.	 Isc_{A+1} Isc_{B-1} Isc_{A+1} Isc_{B-1}		 131 -130		 mA mA
Output Resistance: DEI1070 DEI1071 DEI1072	25 ºC Calculated from Open circuit output voltage and 400 Ohm load output voltage	 Rout37 Rout10 Rout0		 37.5 10 0		 Ohms Ohms Ohms
Output Slew Rate, Hi Speed Lo to Hi and Hi to Lo transitions	HI/LO = 1 No Load 10% to 90% voltage amplitude of differential output.	T_{HI}	1.0		2.0	uS
Output Slew Rate, Lo Speed Lo to Hi and Hi to Lo transitions	HI/LO = 0 No Load Measured from 10% to 90% voltage amplitude of differential output.	T_{LO}	5		15	uS
Output skew time between A and B outputs.	HI/LO = 1 Measured at 50% voltage amplitude of both outputs	Tskew			200	nS
Supply Current						
Quiescent Operating Supply Current: IV+ IV-	V+ =15V, V- = -15V HI/LO = 0 or 1 TTLINA=TTLINB= 0V No Load	 I_{+V} I_{-V}	 - -14.0	 6.0 -6.0	 14.0 -	 mA mA

DESIGN CONSIDERATIONS

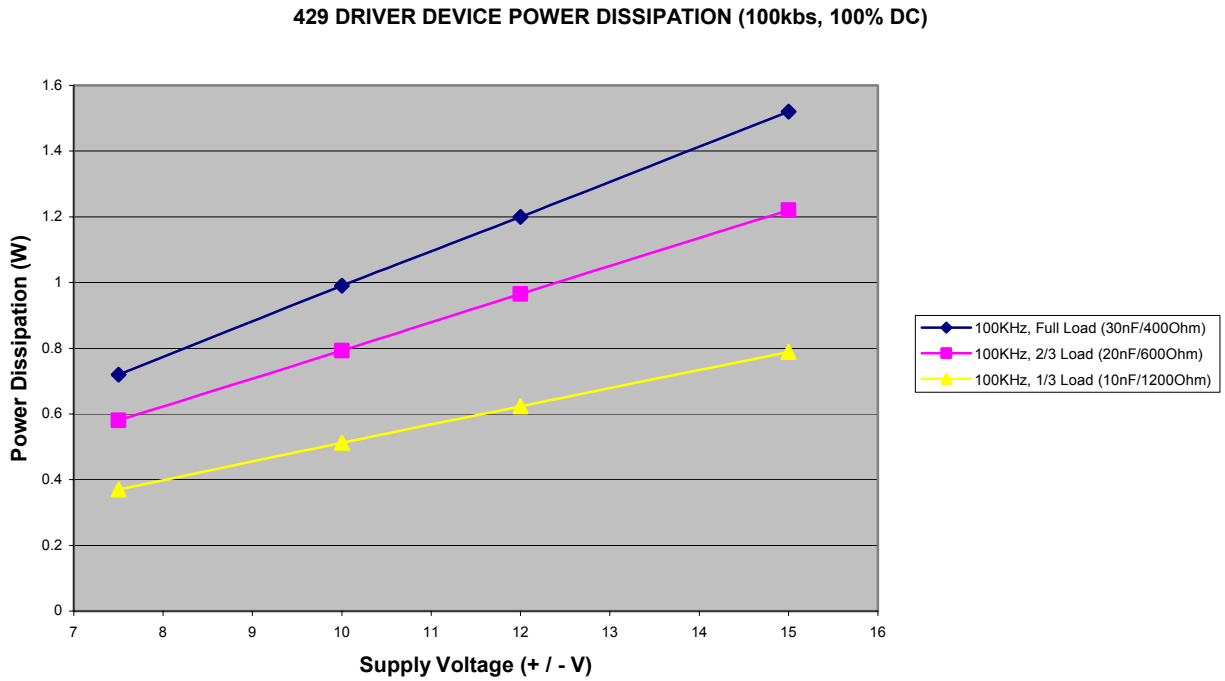
Transient Voltage Protection

External transient voltage suppressing devices are required to protect the device from stress such as that defined by DO160D Section 22, Lightning Induced Transient Susceptibility. The output stage of the driver includes intrinsic clamp diodes to the V+ and V- power Rails. Consider using the 0 Ohm output option to allow use of an external 36 Ohm current limiting resistor and transient voltage suppressor. Transients at the device must be limited to less than one diode drop beyond the power rails to prevent excessive current to the device.

Thermal Management

Device power dissipation varies greatly as a function of data rate, load capacitance, data duty cycle, and supply voltage. Proper thermal management is important in designs operating at the HI speed data rate (100KBS) with high capacitive loads and high data duty cycles. Dissipation may be estimated from the graph below which shows the approximate power dissipation for various loads and supply voltages. It is calculated for 100% data duty cycle at 100KBS with no word gap null times and must be reduced by the appropriate data duty cycle. Adjust for the application data duty cycle using a factor of (total bits transmitted in 10 sec period / 1,000,000) = (32 x total ARINC words transmitted in 10 sec period / 1,000,000).

Heat transfer from the IC package should be maximized. Use maximum trace width on all power and signal connections at the IC. The exposed heat sink pad of the SOIC package should be soldered to a heat spreader land on the PCB. The pad is internally connected to the V- power rail. Maximize land size by extending beyond the IC outline if possible. Place vias on the signal/power traces close to the IC and on the heat spreader land to maximize heat flow to the internal power planes.



PACKAGE DESCRIPTION

8 Lead EDQUAD SOIC

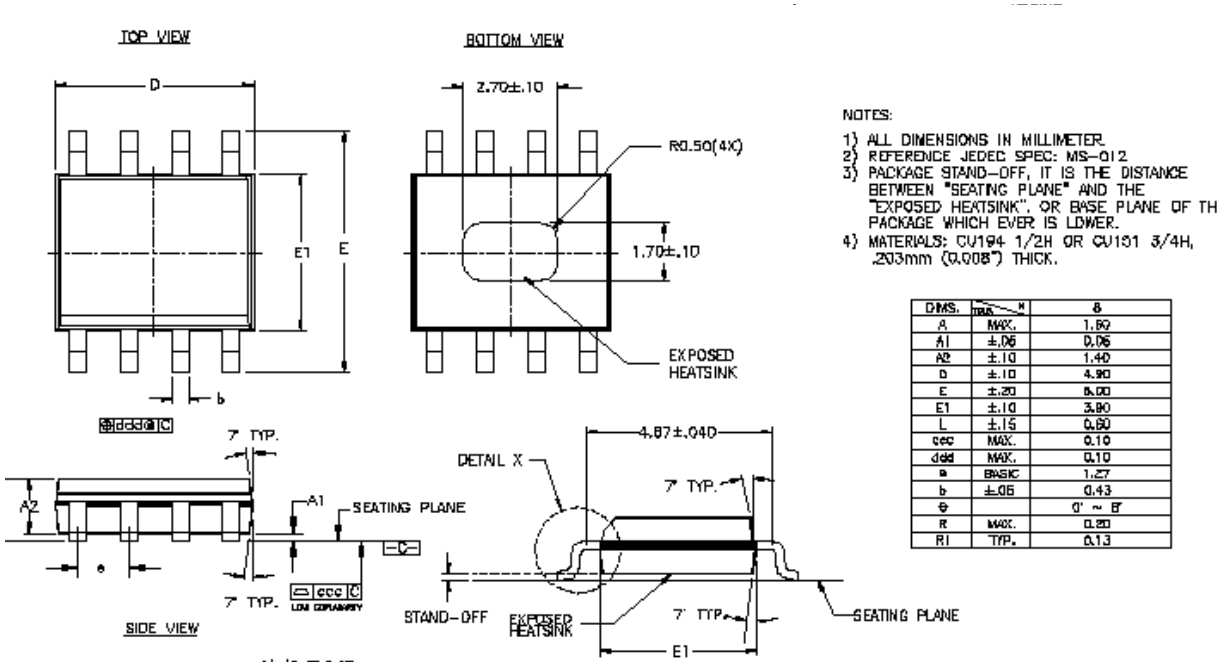


Table 7 8 Lead EDQUAD SOIC Characteristics

SYMBOL	DESCRIPTION	VALUE	UNITS
$Theta_{jc}$	Junction to Case	TBD	°C/W
$Theta_{ja}$	Junction to Ambient. 4 layer board with 2 internal power planes. Exposed pad soldered to PCB heat spreader land.	75	°C/W
MSL	JEDEC Moisture Sensitivity Level	3	-

ORDERING INFORMATION

Part Number	Marking	Package	Output Resistor	Temperature
DEI1070-SES	DEI1070	8 EQ SOIC	37	-55 / +85 ºC
DEI1071-SES	DEI1071	8 EQ SOIC	10	-55 / +85 ºC
DEI1072-SES	DEI1072	8 EQ SOIC	0	-55 / +85 ºC
DEI1070-CMS	DEI1070	8 CERDIP	37	-55 / +125 ºC
DEI1071-CMS	DEI1071	8 CERDIP	10	-55 / +125 ºC
DEI1072-CMS	DEI1072	8 CERDIP	0	-55 / +125 ºC