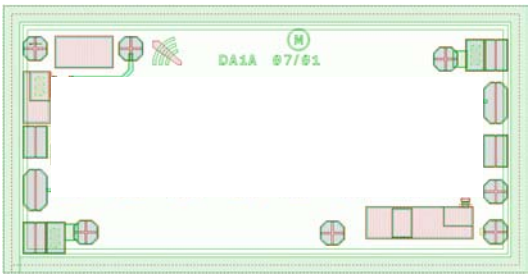
CENTELLAX

SPEED INNOVATION

DA1A Broadband 40Gb/s Amplifier

Part Number: DA1A0001

Data Sheet: rev.07 March 2002



1640 X 830 um

- **> 10 db Gain**
- **17dBm Psat**
- **Fast Rise Time**
- **Low Jitter**
- **Dynamic Gain Control**
- **DC to 65GHz Bandwidth**
- **Low Power Dissipation**

Application

The DA1A MMIC Amplifier is designed for OC768 (40Gbs) optical communication systems. The amplifier can be used as a trans-impedance amplifier (TIA), small signal gain block, and as a driver amplifier for electro-absorption modulators (EAM).

Description

The DA1A is a seven stage medium power broadband Traveling Wave Amplifier. The amplifier has been designed for low jitter and constant group delay over the 40Gb/s operating range. By using external components the bandwidth of operation can be extended to low frequencies <100 KHz. A bonding pad is provided for dynamic gain control.

Optical Microwave

The DA1A Amplifier is optimized for 40 Gb/s EAM and TIA applications. It is an excellent selection as an optical receiver gain block or as a medium power modulator driver amplifier. The amplifier features a rise time of less than 8 ps.

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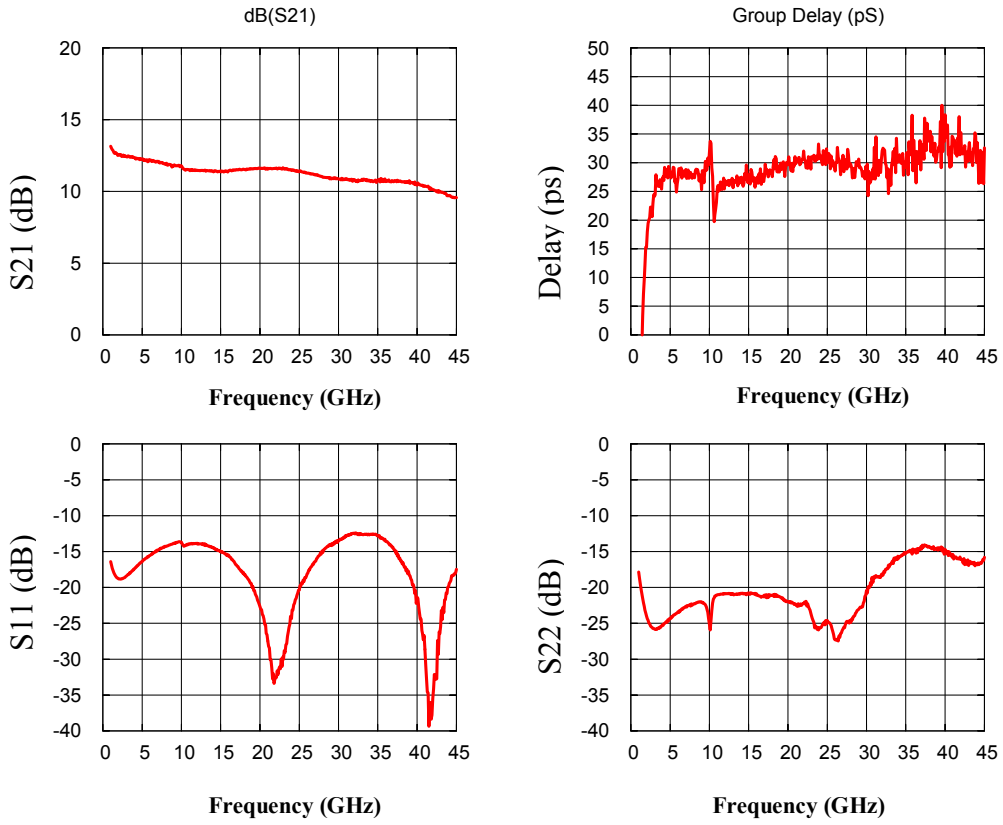
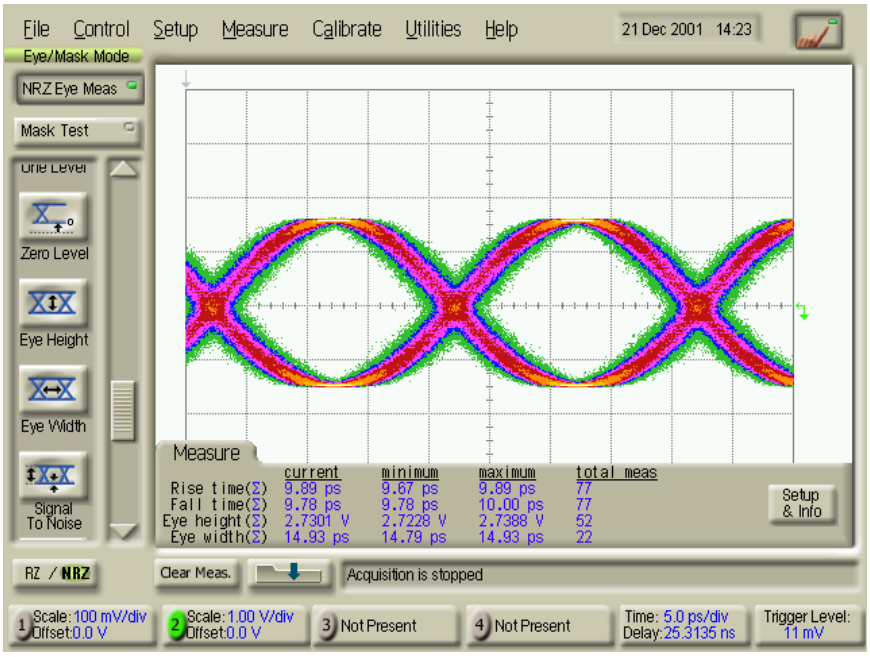
RF Specifications

Vdd = 4.5V, Idd = 85mA, Zo = 50 Ohms

Parameter	Description	Min	Typ	Max
S11/S22 (dB)	DC-45 GHz	-10	-12	-
S21 (dB)	Small Signal Gain @ 25 GHz	10	12	
S21 (dB)	Small Signal Gain @ 65 GHz	6	7.5	
Z_T (Ohms)	AC Transimpedance	160	200	
Isolation (dB)	Reverse Isolation	20	30	
Bandwidth (GHz)	1 – 65 GHz			
P-1dB (dBm)	1dB Gain Compression		14	
Psat (dBm)	Saturated Output Power		17	
Rise Time ps	25 GHz Rise Time			8
Voltage Output (V)	Peak to peak output voltage at 25 GHz	3.5	3.8	
Pdc (mW)	DC Power Dissipated		382	

Measured Performance*: Vdd 4.5V; Idd = 85mA





50 GB/s [101010…] Pattern

$$Tr \approx \sqrt{\Sigma_i (Tri)^2}$$

$$Tr \approx \sqrt{(Tr)^2_{Amp} + (Tr)^2_{TestEquipment}}$$

$$Tr_{Amp} < 8 \text{ ps}$$

DC/RF Operation

Parameter	Description	Min	Typ	Max
Vdd	Drain Bias	3 V	4.5V	7.5 V
Idd	Drain Current	-	85mA	200 mA
Vgg	Gate Bias	-4 V	-	0 V
Vgc	Gain Control	-4 V	N.C.	4 V
Pdc	Power Dissipation	0.22 W	0.4W	1.5 W
Pin	Input Power (CW)	-		20 dBm
Tch	Channel Temperature			150° C
Θ_{ch}	Thermal Resistance (T_{case}= 25°C)		60 °C/Watt	
Idss			100	

Biasing Info

DC Bias

The DA1A is biased using a positive voltage on the drain (Vdd), and by setting the drain current (Idd) using a negative voltage on the gate (Vgg). When zero volts is applied to the gate the drain to source channel is open which results in high Ids. When Vgg is negative the drain to source channel is "pinched off" and Ids is lowered with increasing negative voltage. Applications using high Vdd may need to apply Vgg before Vdd to remain below maximum power dissipation (1.5W).

The nominal bias condition is Vdd = 4.5V, Ids = 90mA. This condition is a good starting point for most designs. Minor improvements in performance and efficiency are possible depending on the application. The drain bias voltage range is 3V to 8V. For applications needing lower noise figure and/or small signal amplification lower drain voltages and currents should be considered. When power performance or slightly higher output voltage is required higher drain voltage and currents may improve performance.

Operation Design Considerations

The DA1A has been designed so that the bandwidth can be extended to low frequencies. The low frequency limit and performance is a function of external circuitry.

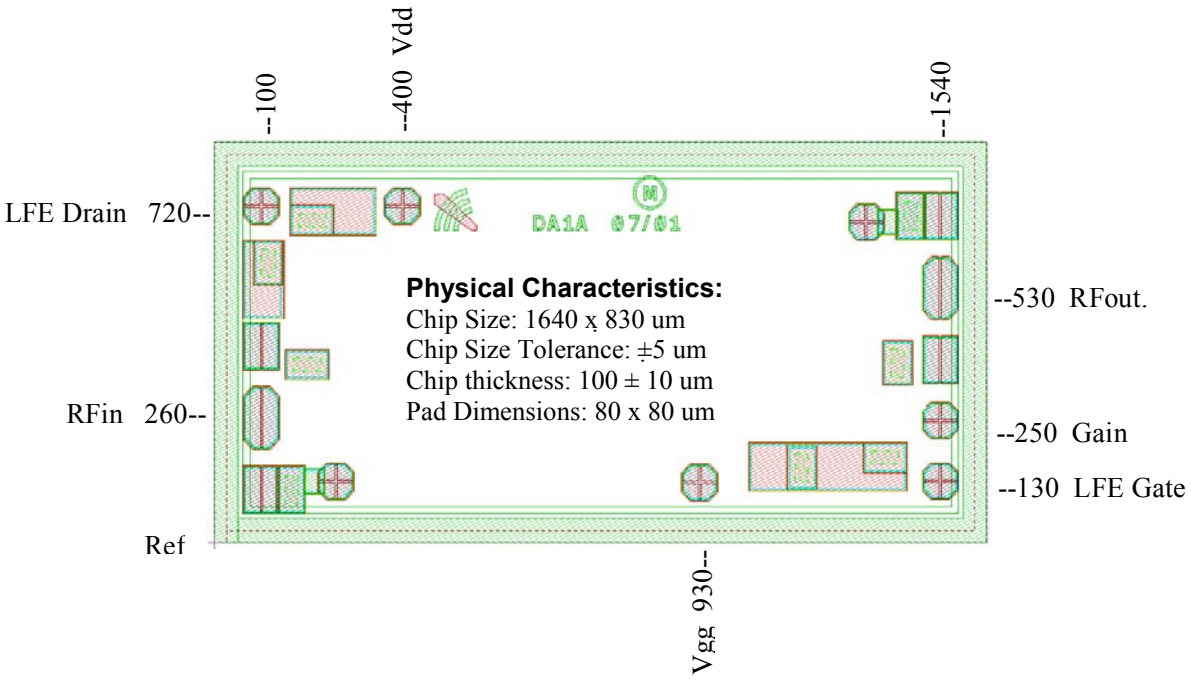
Matching: The amplifier incorporates on chip termination resistors for RF input and output. These resistors are RF grounded through on-chip capacitors, which are small and become open circuits at low frequencies <1GHz. Bonding pads (LFEin and LFEout) have been provided for connecting external RF grounding capacitors used in the low frequency extension network.

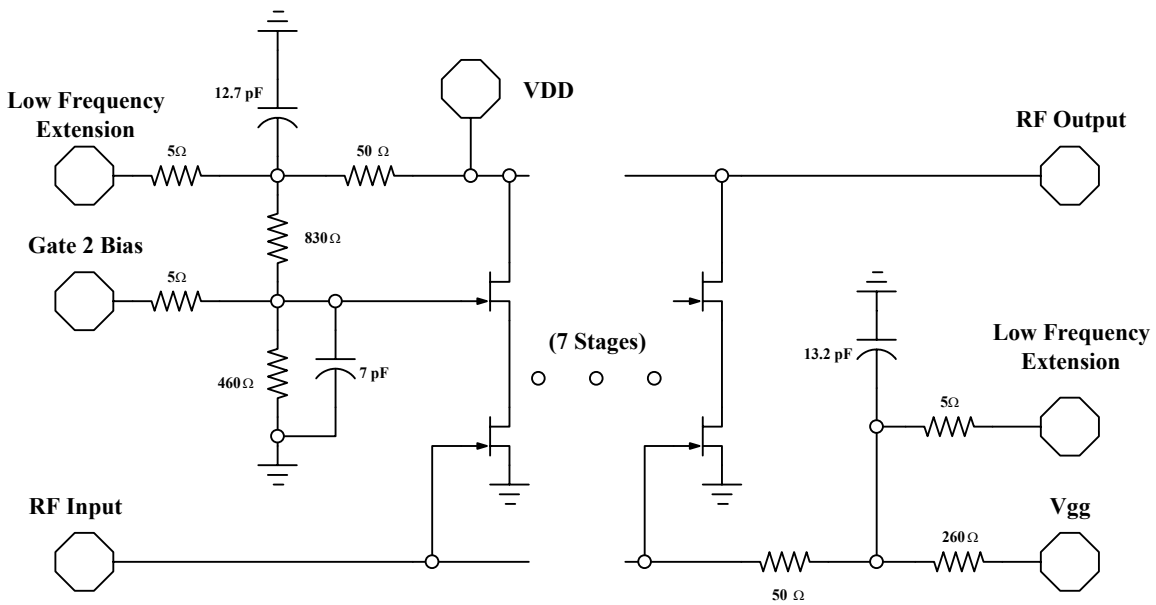
Inductor Bias: DC bias Vdd is applied directly to the RF output path through a biasing inductor and must be decoupled down to the lowest operating frequency. Inductive biasing may be applied to the on chip Vdd pad or through the RFout port.

DC Blocks: Since the amplifier is DC coupled on the RFin and RFout ports the DC appearing on these ports must be isolated from external circuitry.

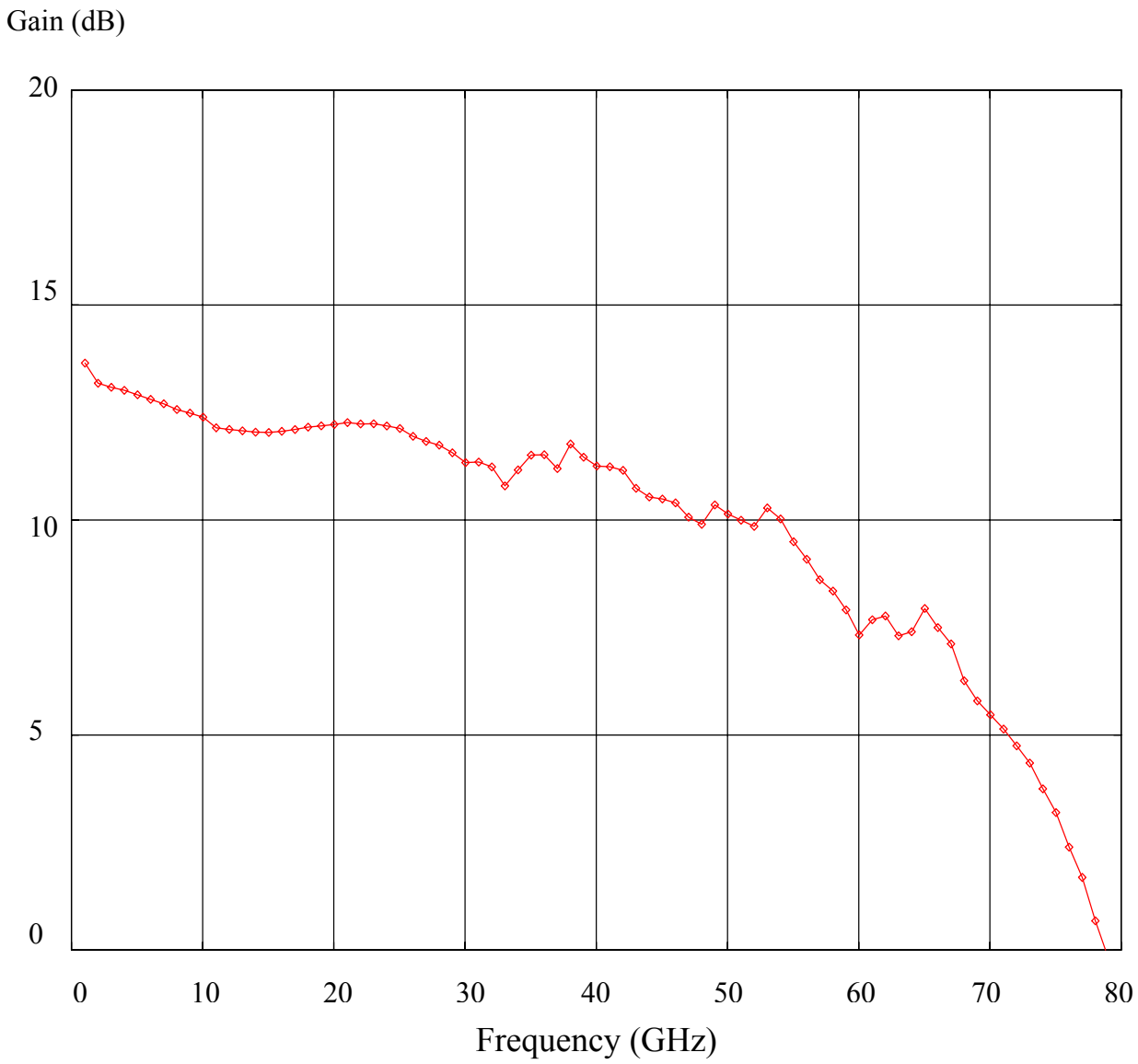
Gain Control: Negative voltage applied to Vg2 pad reduces the amplifier gain. Dynamic gain control is possible when operating the amplifier in the linear gain region.

ESD Handling and Bonding: This MMIC is ESD sensitive and preventive measures should be taken during handling, die attach and bonding.





Low Frequency Schematic Circuit
For the DA1A Amplifier



DA1A Gain vs. Frequency (Vds=4.5 V Ids=85 mA)

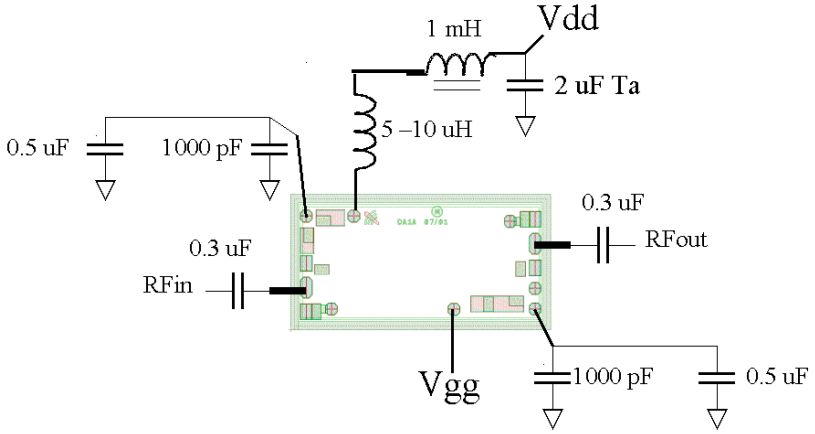
Centellax DA1A Amplifier Low Frequency Extension

The DA1A amplifier's broadband performance can be extended to low frequencies using external components. Examples include telecom standards requiring operation to frequencies below 100 kHz. Operating at these low frequencies requires the use of components that can seriously degrade millimeter wave performance. For example, large value capacitors typically have significant series inductance while large valued inductors exhibit parasitic inter-winding capacitance. Both types of parasitic effects cause series and/or parallel resonances, which can lead to suck-outs in the gain response, poor return loss, or inter-symbol interference. Careful attention to the design of these external low frequency circuits is essential to obtain broadband performance.

Maintaining broadband performance while extending the response to low frequencies requires careful attention to two areas of design:
Maintaining 50 Ohms impedance on the RF input and output for good matching
Decoupling the drain bias from the RF output to the lowest frequency of operation.

1) Traveling wave amplifier design requires proper termination of the incoming and outgoing waves. The gate and drain load resistors are on chip and terminated to RF ground by means of small integrated MIM capacitors. These capacitors are typically only a few pF in size and cause the termination resistors to open up at low GHz frequencies. Bond pads on the DA1A allow for the connection of larger valued, external capacitors in order to provide RF ground down to lower frequencies. Choice and placement of these components is critical to maintaining the required 50 Ohms terminating impedance for the RF input and output. Operation to frequencies ~ 10 MHz is achieved using microwave chip capacitors of approximately 1000 pF. These capacitors should be physically small, placed close to the chip, and connected to the MMIC bond pads with short bond wires. For frequencies below 100 kHz, an additional monoblock capacitor (0.1uF or greater) with low series inductance is placed in parallel with the microwave chip capacitor by attaching one end of the monoblock to the top of the chip capacitor and the other end to ground.

2) Inductive decoupling of the drain bias to the lowest frequency of operation requires careful design. The large values of inductance (~500 uH) required to isolate the DC & RF to low frequencies typically imply physically large components. These large components are difficult to integrate into the microwave package and have many parasitic effects which can lead to narrow band resonances, thus degrading the amplifier's broadband performance. Two or three inductors in series with one large bypass capacitor connected to ground form the typical design approach. It is important to minimize all capacitance to ground between the multiple inductors to prevent unwanted resonances. A tantalum capacitor greater than 2 uF provides good bypassing as well as suppression of low frequency bias oscillations. Piconics Inc. has designed a series of conical shaped inductors which provide good de-coupling from millimeter wave frequencies down to ~ 1 MHz. A second, large inductance valued inductor in series completes the de-coupling circuit. The drain bias to the MMIC can be supplied to the RF output port in place of the drain bias pad on the MMIC. DC blocking capacitors may be required at the input and output ports.



Assembly Diagram