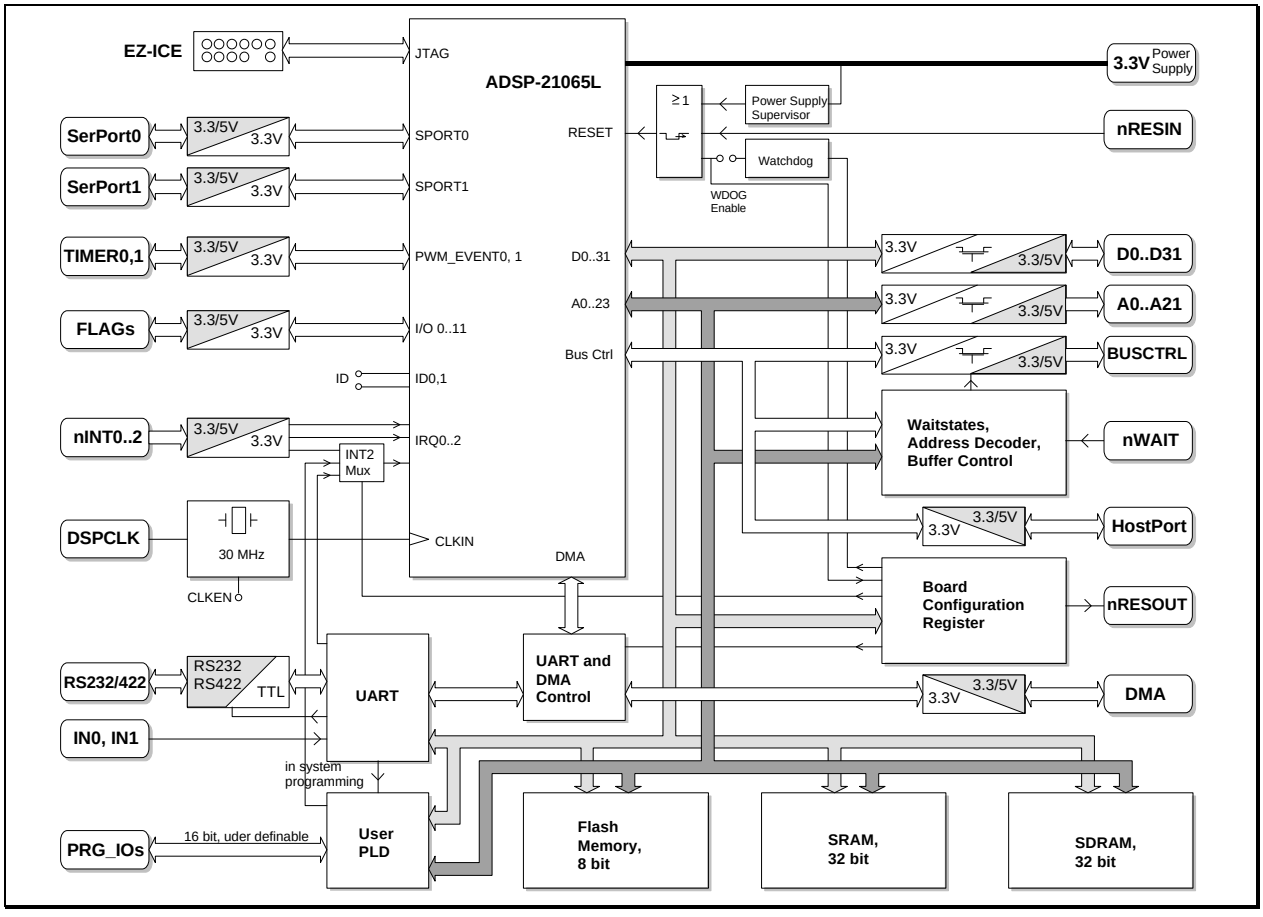
**SUMMARY**

- **High Performance Floating Point DSP Computer Module for I/O and communication intense applications requiring highest performance and precision**
- **30 MHz 180 MFLOPS ADSP-21065L DSP**
- **Stand-alone Operation**
- **Watchdog and Power Supply Supervisor**
- **256 kByte SRAM, 16 MByte SDRAM and 512 kByte non-volatile Flash Memory Expansion**
- **Two Multichannel Serial Ports, 5V tolerant**
- **External Bus Interface for memory and I/O expansion, 5V tolerant**
- **Wait State Logic for all on-board devices**
- **Three pre-decoded memory select signals**
- **Host Interface**
- **Dual Processor Support**
- **Zero Overhead Communications: UART with auto-flow-control and DMA support, up to 460 kBaud**
- **User configurable 32 macrocell CPLD for I/O expansion, serial and parallel interfaces and Bus adaptation**
- **Two 32 bit Timers with Capture and PWM, 5V tolerant**
- **Three external Interrupts**
- **28 individually configurable I/O signals: 12 direct I/O signals to/from DSP, 5V tolerant plus 16 I/O signals to/from the CPLD**
- **JTAG Emulation Port**
- **Small Size: only 85 x 59 mm**
- **3.3V Single Supply**
- **D.Module.BIOS Application Programming Interface**


The D.Module family of DSP based Computer Modules offers a standardised hardware platform for embedded DSP applications. Mechanics and pinout are identical throughout the family members. 111 signals are reserved and provide identical functionality. In combination with the D.Module.BIOS - a hardware independent application programming interface for onboard components UART, Flash Memory etc. - portability is maintained. Re-engineering is reduced to a minimum if your system's requirements change.

## DSP

The heart of the D.Module.21065 is the SHARC® (Super Harvard Architecture) Floating Point DSP ADSP-21065L from Analog Devices. This DSP offers 32/40 bit IEEE floating point and 32 bit integer arithmetic with a maximum performance of 180 MFLOPS. 68 kByte internal dual-ported RAM can be configured for 48 bit program and 32 or 40 bit data, an instruction cache reduces memory conflicts.

The serial ports provide a direct connection to industry standard Codecs, A/D and D/A converters, the multichannel support allows direct connection to T1/E1 signals. Communication up to 30 MBit / sec is possible. The multichannel capabilities make the serial ports usable for inter-processor networks as well. Control signals for external driver/receiver circuits are provided. Serial ports are connected to level shifters which allow direct interfacing of 5V equipment.

The CPU is relieved from data transfer tasks by a ten channel DMA controller with advanced features like DMA chaining, FIFOs and auto-initialisation. DMA is also possible to and from external memory and a host processor.

The ADSP-21065's twelve individually configurable I/O ports are buffered with level shifter circuits to enable a direct integration into 5V environments. In combination with the user-configurable CPLD up to 28 I/O ports are provided by the D.Module.21065.

The module fully supports dual processor operation, a daughter module with a second ADSP-21065L can be connected in shared memory configuration to double the processing power.

## MEMORY

The DSP itself is equipped with 544 kBit dual-ported memory, configurable for program and data words. On the D.Module.21065, this is expanded by 256 kByte zero wait state SRAM, organised as 64k x 32 bit. Optionally 1 MByte (256k x 32bit) is available. This external memory can be used to store data as well as instruction words. Program parts which are not time-critical can be executed directly from the SRAM (two memory accesses are required to load a 48 bit instruction) thus saving internal dual-ported RAM for data and parameter storage.

If large data buffers are a requirement, the module can be equipped with 16 or 32 MByte SDRAM, organised as 4M or. 8M x 32 bit.

The Flash Memory is used for non-volatile data and program storage. A sector architecture is used which provides individually erasable blocks of 64 kByte each. The DSP has direct access to the Flash Memory, the BIOS functions handle device identification, erase and program sequencing. An on board wait state generator provides the required wait states for the Flash Memory while retaining zero wait state access to SRAM, SDRAM, the CPLD, the Board Configuration Register and external memory areas.

For external memory expansion three memory areas and pre-decoded select signals exist. These are primarily intended for the connection of parallel interface data acquisition and communication devices, dual-ported memories and FIFOs, but can be used for asynchronous static SRAM expansion and/or additional Flash Memory as well. One of these select lines is used to decode the on board SDRAM, it is not available as an external select signal on modules with SDRAM.

## CLOCKS

An on board oscillator generates the 30 MHz master clock for the module. This clock is fed to the DSPCLK pin, it can be configured as an output to other devices or as an input if the module should be synchronised to your system. The UART has it's own clock generation circuit, independent of the DSP clock. The serial ports can be clocked externally or generate clocks and frame syncs based on the DSP clock. Additional clocks for external peripherals can be generated using the two timer circuits.

## POWER SUPPLY

The D.Module.21065 requires a 3.3V single voltage power supply. Secondary voltages for RS232 and the 5V level shifters are generated on board by charge pump devices. A microprocessor supervisor circuit monitors the supply voltage and holds the module in reset while the power supply is below the specified limits.

## EXTERNAL BUS INTERFACE

The external bus interface provides a 32 bit wide data bus, 22 address lines and control signals. Wait states for devices connected to the three pre-decoded memory areas are software selectable, the nWAIT input can be used to request additional wait states for slow peripherals. The entire bus interface is 5V tolerant and isolates external devices during on-

board access to minimise bus loading during fast SRAM or SDRAM cycles. The external bus interface is capable of a maximum transfer rate of 120 MByte/sec.

The user-configurable CPLD can be used to adapt the bus interface to different formats - e.g. to connect ISA bus devices - by integrating the required state-machines and decoders. Glueless integration into a variety of host systems is made possible.

### HOST INTERFACE

A host controller can be interfaced via the external bus interface as well. The host has access to the ADSP-21065 internal I/O processor, which allows to access any memory location via DMA, communicate via message passing registers etc. The host data bus can be 8, 16 or 32 bit wide. If no other parallel devices except the host are connected to the module, the level shifters can be used to connect the host data bus to the module, providing a glueless interface. The user-configurable CPLD can be used to implement decoders and bus adaptation for the host.

### UART

The UART offers powerful features: 32 word receive and transmit FIFOs and automatic flow control - RTS/CTS and Xon/Xoff - relieve the DSP from time-consuming interrupt driven data transfers. Baud rates up to 460 kBaud are possible. The line interface is RS232, optionally RS422/485 is available. The on-board wait state logic generates the required wait states for UART accesses while retaining fast access to other asynchronous memory devices or expansions. These features have been combined with the ADSP-21065 external DMA signals to enable zero overhead communications: all the data transfer is handled by DMA without DSP core intervention.

The UART is fully supported by the D.Module.BIOS: initialisation, busy-polling and DMA driven communication functions are provided.

### USER-CONFIGURABLE CPLD

One of the major challenges in DSP design is the integration into a host system and interfacing peripherals. To facilitate this we have integrated a 32 macrocell in-system programmable CPLD. 8 bit data bus, address lines, control and clock signals and an interrupt / DMA request signal are pre-connected to the DSP. The CPLD can be re-programmed via the module's Set-Up Utility program by uploading the JEDEC file. Typical uses of the PLD are additional parallel and serial ports, interrupt controller, bus interface adaptation, clock generation and more. 16 I/Os are available and can be individually configured as input, output, bi-directional or three-state signals.

Please note: currently these signals are not 5V tolerant. Configured as output, they can directly drive 5V TTL logic, configured as input or bidirectional, level shifters or current limiting resistors have to be used for 5V interfaces.

### BOOT OPTIONS

By default the D.Module.21065 is boot-loaded from the Flash Memory. In this mode, the BIOS and the Set-Up Utility are loaded first. The nSETUP signal (IN0) is sampled, if low, the Set-Up mode is entered which allows to store programs and data in the Flash Memory, (re-)program the CPLD by uploading the JEDEC file and execute diagnostic functions via a RS232 terminal connection. If nSETUP is not asserted at reset, the BIOS bootloader loads and executes your application program.

The BIOS provides a bootload function which allows to load the application program from any location in the DSP memory space - e.g. from a dual ported memory - or via the host port.

### MODULE CONFIGURATION

A module configuration register controls additional I/O signals and module settings: Watchdog Trigger, Reset-Output, Interrupt and DMA multiplexer. The module's reset source can be determined from the configuration register which allows to identify a reset caused by a watchdog timeout.

The DMA and Interrupt multiplexer selects the sources for the DSP interrupt IRQ2 and external DMA channels DMAR1 and DMAR2. These signals can be driven by either external signals, the CPLD, the UART receiver and the UART transmitter.

### RESET AND WATCHDOG

A micro-processor supervisor circuit monitors the power supply and resets the module during power-up, power-down and brown-out conditions. A re-triggerable single-shot guarantees a minimum reset pulse width of 140 msec.

A debounced external reset input can be used to connect a system reset signal or a push-button for manual reset. An open drain reset output is con-

trolled via the module configuration register and can be used to initialise external peripherals.

A watchdog provides security against program lock-ups and hardware failures as required by most embedded applications. The watchdog timer must be re-triggered at least every 1.6 seconds, otherwise a reset is generated. The watchdog trigger is generated by the module configuration register. The module configuration register latches the state of the watchdog at reset which allows to distinguish between power fail / manual reset and a reset caused by a watchdog timeout.

### EXTERNAL INTERRUPTS

The ADSP-21065 features three external interrupt inputs which are available on the D.Module.21065. These interrupt inputs are provided with 5V tolerant buffers, INT2 is multiplexed with the UART and CPLD interrupt. This multiplexer is software-controlled via the module configuration register. Interrupt inputs are falling edge triggered. If more interrupts are a requirement, the user-configurable CPLD can be used to implement an additional interrupt processor.

### MULTIPROCESSING

The D.Module.21065 is designed to support a dual-processor shared memory configuration. A daughter module (D.Module.21065-co) with a second ADSP-21065L can be connected to the module and has access to all on-board devices. This provides a straightforward upgrade path if your processing requirements grow.

In a dual-processor configuration the on-board resources are shared by both processors: SRAM, SDRAM, Flash Memory, UART, CPLD, Module Configuration Register and the External Bus (nIOSEL and nMEMSEL memory range). Such a system provides a total of 8 serial port receivers, 8 serial port transmitters, 4 timers with PWM capabilities and 40 I/O signals.

### BIOS

The D.Module.BIOS is an application programming interface for all on board resources. It encapsulates the hardware dependencies and provides functions for

- Module initialisation (wait states, SDRAM initialisation, dual-processor synchronisation)
- UART initialisation , send and receive functions including error and break detection and handshake.
- Flash Memory programming support: identify device, erase a sector, programming
- Module configuration: set and clear bits and bitfields in the module configuration register
- Miscellaneous functions: bootload, watchdog trigger, delay etc.

These functions are identical on all D.Modules and help to maintain program portability throughout the D.Module family. The BIOS is written in hand-coded Assembler language to achieve optimum performance. All functions are C and Assembler callable.

The BIOS fully supports the dual-processor configuration and performs the required synchronisation of both DSPs at system start-up.

The BIOS is copied from Flash Memory to internal and external RAM at system start-up. Frequently called functions are located in internal memory for fast execution whereas initialisation and configuration functions are located in external memory (SRAM).

## MEMORY MAP

| Address | Memory | Wait States | Comment |
|---|---|---|---|
| 0x0000.0000 .. 0x0000.00FF | internal IOP | - | I/O processor |
| 0x0000.0100 .. 0x0000.01FF | IOP (ID1) | WAIT register | I/O registers ID1 (dual-processor system only) |
| 0x0000.0200 .. 0x0000.02FF | IOP (ID2) | WAIT register | I/O registers ID2 (dual-processor system only) |
| 0x0000.8000 .. 0x0000.9FFF | internal mem | - | Block 0, normal addressing<br>(locations 0x8100..0x81AF reserved for BIOS) |
| 0x0000.C000 .. 0x0000.DFFF | internal mem | - | Block 1, normal addressing |
| 0x0001.0000 .. 0x0001.3FFF | internal mem | - | Block 0, short addressing (16 bit data) |
| 0x0001.8000 .. 0x0001.BFFF | internal mem | - | Block 1, short addressing (16 bit data) |
| 0x0002.0000 .. 0x0002.FFFF | SRAM | 0 | external SRAM 64k x 32 bit<br>(0x2.0000 .. 0x2.03FF) reserved for BIOS |
| 0x0080.0000 .. 0x0097.FFFF | Flash Memory | on board hardware | Flash Memory 512k x 8 bit, bit 0..7<br>(the first sector 0x80.0000 .. 0x80.FFFF is reserved for BIOS and Set-Up utility, 448 kByte are available to the user) |
| 0x00A0.0000 .. 0x00A0.0003 | CPLD | 0 | user-configurable CPLD, bit 0..7 |
| 0x00C0.0000 .. 0x00C0.0007 | UART | on board hardware | UART, bit 0..7 |
| 0x00E0.0000 | CFG-Register | 0 | Module Configuration Register, bit 0..9 |
| 0x0100.0000 .. 0x013F.FFFF | SDRAM<br>or<br>ext. memory | WAIT register MS1 or ext. nWAIT | -D0 modules : SDRAM 4M x 32 bit<br>others: nMS1 asserted,<br>external bus connected to DSP |
| 0x0200.0000 .. 0x023F.FFFF | ext. memory | WAIT register MS2 or ext. nWAIT | nIOSEL asserted,<br>external bus connected to DSP |
| 0x0300.0000 .. 0x033F.FFFF | ext. memory | WAIT register MS3 or ext. nWAIT | nMEMSEL asserted,<br>external bus connected to DSP |



## BOARD CONFIGURATION REGISTER

| Bit | D9 | D8 | D7, D6 | D5, D4 | D3, D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| **Signal** | WDOG_RES | WDOG | DMA2_MUX | DMA1_MUX | INT2_MUX | UART_RES | nRESOUT |
| **Bit = 1:** | read only:<br>reset caused by watchdog timeout | WDOG Trigger high | 00: nDMAR2<br>01: UART Rx<br>10: UART Tx<br>11: CPLD | 00: nDMAR1<br>01: UART Rx<br>10: UART Tx<br>11: CPLD | 00: nINT2<br>01: UART<br>10: CPLD<br>11: reserved | UART in Reset | nRESOUT output 3 State (pulled high via resistor) |
| **Bit = 0:** | read only:<br>power-on or manual reset | WDOG Trigger low | connected to DSP signal DMAR2 | connected to DSP signal DMAR2 | connected to DSP signal INT2 | UART in normal operation | nRESOUT output driven low |
| **Reset State** | see text | 0 | 00 | 00 | 00 | 1 | 0 |

## SIGNAL DESCRIPTION

### EXTERNAL BUS INTERFACE

| Signal | Pin | Type | Description |
|---|---|---|---|
| A0 .. A21 | U9 .. U14, V2 .. V14, A14.. A16 | O/Z | address bus, A0 .. A21 via level shifter, 5V TTL compatible, high impedance during on board accesses |
| D0 .. D31 | V15 .. V30 U15.. U30 | I/O/Z | data bus, connected via level shifter, 5V tolerant, high impedance during on board accesses |
| nRD | U2 | O | active low read strobe signal, 5 V TTL compatible, use for asynchronous external accesses |
| nWR | U5 | O | active low write strobe signal, 5 V TTL compatible, use for asynchronous external accesses |
| nIOSEL | U8 | O | active low memory select signal for asynchronous external devices, 5V TTL compatible, connected to ADSP-21065L MS2 signal. |
| nMEMSEL | V31 | O | active low memory select signal for asynchronous external devices, 5V TTL compatible, connected to ADSP-21065L MS3 signal. |
| BUSCLK | U6 | O | clock, all bus cycles are synchronous to this clock, use BUSCLK to latch the state of the external bus, 5V TTL compatible |
| nWAIT | A10 | I | active low, forces wait states for asynchronous external accesses if asserted, on board pull up resistor 470 Ohms, 5V tolerant |
| nDMAR1, nDMAR2 | T28, T30 | I | external DMA request, 5V tolerant, internal pull-up resistor, multiplexed with UART and CPLD via the Board Configuration Register |
| nDMAG1, nDMAG2 | T29, T31 | O | external DMA grant, 5V TTL compatible |
| A22, A23 | A17, A18 | O/Z | address bus for multiprocessor configurations only |
| SDCLK0 | T2 | I/O | for multiprocessor configurations only |
| nSDRAS | T3 | I/O | for multiprocessor configurations only |
| nSDCAS | T4 | I/O | for multiprocessor configurations only |
| nSDWE | T5 | I/O | for multiprocessor configurations only |
| SDA10 | T6 | I/O | for multiprocessor configurations only |
| nMS1 | T7 | I/O | for multiprocessor configurations<br>or as an additional active low memory select signal for asynchronous external devices, 5V TTL compatible, for modules without SDRAM! |
| DQM | T8 | I/O | for multiprocessor configurations only |
| SDCKE | T9 | I/O | for multiprocessor configurations only |
| ACK | T10 | I/O | for multiprocessor configurations only |
| nMS0 | T11 | I/O/Z | for multiprocessor configurations only |
| nBMS | T12 | I/O/Z | for multiprocessor configurations only |
| nBR0, nBR1 | T13, T14 | I/O/Z | for multiprocessor configurations only |
| nSW | T15 | I/O/Z | for multiprocessor configurations only |
| nSBTS | T23 | I | assert to resolve multiprocessor-host deadlocks only |

**SERIAL PORTS**

| Signal | Pin | Type | Description |
|---|---|---|---|
| DAT_RX0 | A26 | I | SPORT0 receiver serial data input, 5V tolerant |
| CLK_RX0 | A27 | I/O | SPORT0 receiver serial clock input or output, 5V tolerant |
| FS_RX0 | A28 | I/O | SPORT0 receiver frame sync input or output, 5V tolerant |
| DAT_TX0 | A29 | O | SPORT0 transmitter serial data output, 5V tolerant |
| CLK_TX0 | A30 | I/O | SPORT0 transmitter serial clock input or output, 5V tolerant |
| FS_TX0 | A31 | I/O | SPORT0 transmitter frame sync input or output, 5V tolerant |
| DAT_RX1 | B26 | I | SPORT1 receiver serial data input, 5V tolerant |
| CLK_RX1 | B27 | I/O | SPORT1 receiver serial clock input or output, 5V tolerant |
| FS_RX1 | B28 | I/O | SPORT1 receiver frame sync input or output, 5V tolerant |
| DAT_TX1 | B29 | O | SPORT1 transmitter serial data output, 5V tolerant |
| CLK_TX1 | B30 | I/O | SPORT1 transmitter serial clock input or output, 5V tolerant |
| FS_TX1 | B31 | I/O | SPORT1 transmitter frame sync input or output, 5V tolerant |
| DAT_RX0B | B22 | I | SPORT0 auxiliary receiver serial data input, 5V tolerant |
| DAT_TX0B | B23 | O | SPORT0 auxiliary transmitter serial data output, 5V tolerant |
| DAT_RX1B | B24 | I | SPORT1 auxiliary receiver serial data input, 5V tolerant |
| DAT_TX1B | B25 | O | SPORT1 auxiliary transmitter serial data output, 5V tolerant |

**TIMERS, FLAGS**

| Signal | Pin | Type | Description |
|---|---|---|---|
| TIMER0 | A21 | I/O | Timer 0 capture input or PWM output, 5V tolerant |
| TIMER1 | A22 | I/O | Timer 1 capture input or PWM output, 5V tolerant |
| FLAG0, FLAG1 | A23, A24 | I/O | Flag 0, 1 general purpose input or output, 5V tolerant |
| FLAG2 .. FLAG5 | B18 .. B21 | I/O | Flag 2..5 general purpose input or output, 5V tolerant |
| FLAG6 .. FLAG11 | T17 .. T22 | I/O | Flag 6..11general purpose input or output, 5V tolerant |

**EXTERNAL INTERRUPTS**

| Signal | Pin | Type | Description |
|---|---|---|---|
| nINT0, nINT1 | U3, U4 | I | external interrupt inputs, falling edge triggered, 5V tolerant, internal pull-up resistor |
| nINT2 | A19 | I | external interrupt input, falling edge triggered, 5V tolerant, internal pull-up resistor,<br>multiplexed with UART and CPLD interrupts via the module configuration register |

**USER-CONFIGURABLE CPLD**

| Signal | Pin | Type | Description |
|---|---|---|---|
| PRG_IO0 ..<br>PRG_IO15 | B2 ..<br>B17 | I/O | programmable I/O, can be used for any purpose, function depends on the PLD-program, configurable as input, output, bi-directional or three state. Note: These signals are not 5V tolerant but can directly drive 5V TTL logic |

**RESET**

| Signal | Pin | Type | Description |
|---|---|---|---|
| nRESIN | A9 | I | debounced reset input, active low, on board pull-up resistor, 5V tolerant |
| nRESOUT | U7 | O/C | reset output, open collector, active low, asserted while module is in reset, onboard pull-up resistor, 5V tolerant, controlled via module configuration register |
| nRESET | T16 | I/O | simultaneous DSP reset for multiprocessor configurations only |

**UART, RS232/422**

| Signal | Pin | Type | Description |
|---|---|---|---|
| RTS / nTxD | A2 | O | RS232 Request To Send flow control output<br>RS422 inverting transmitter output |
| TxD | A3 | O | RS232 transmitter output<br>RS422 non-inverting transmitter output |
| CTS / nRxD | A4 | I | RS232 Clear To Send flow control input<br>RS422 inverting receiver input |
| RxD | A5 | I | RS232 receiver input<br>RS422 non-inverting receiver input |
| IN0 (nSETUP), IN1 | A11, A12 | I | general purpose inputs, on board pull-up resistor, IN0 is sampled at reset to determine Setup-Mode |

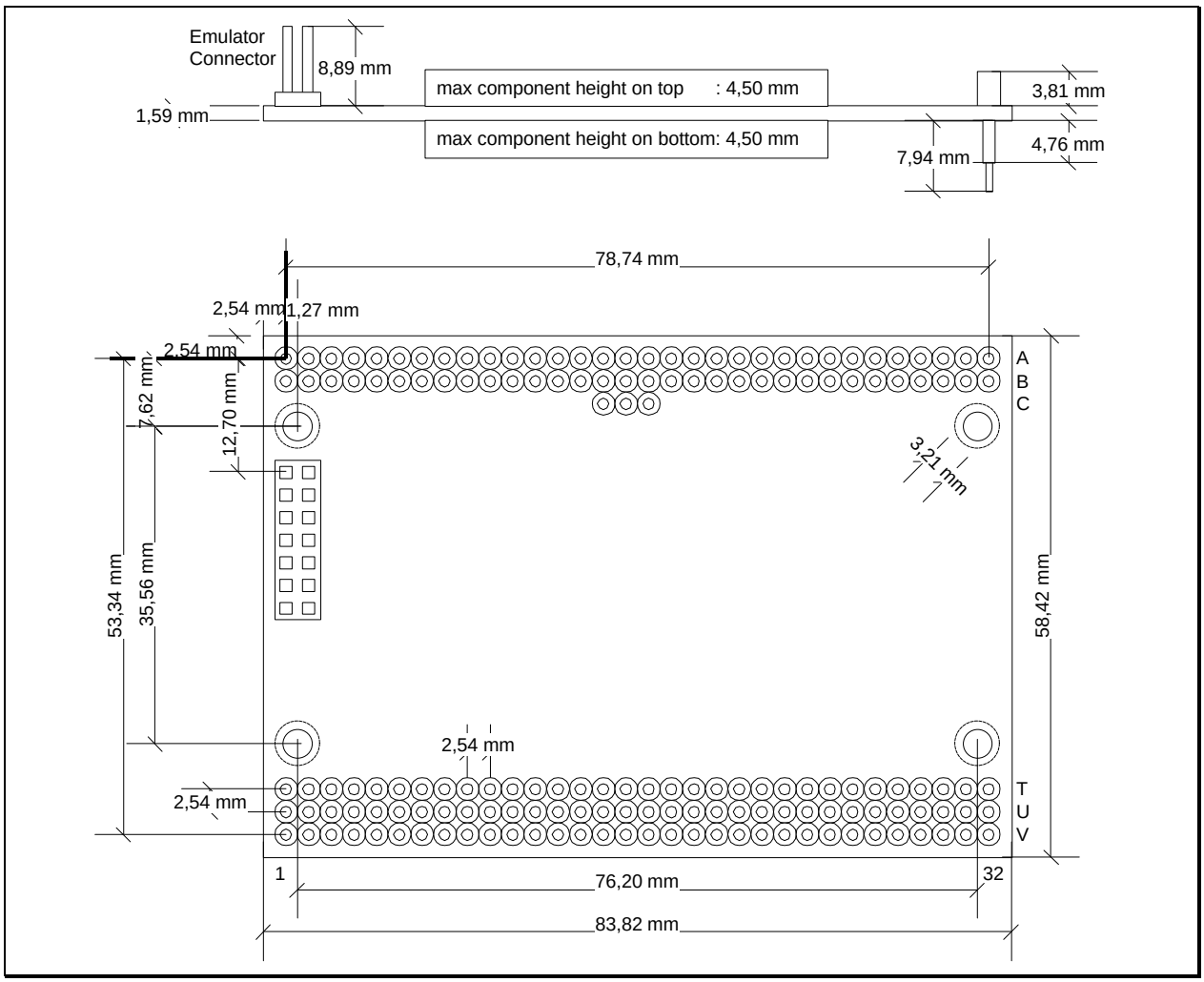
**HOST INTERFACE**

| Signal | Pin | Type | Description |
|---|---|---|---|
| nHBR | T25 | I | Host Bus Request, 5V tolerant, on board pull-up resistor |
| nHBG | T26 | O | Host Bus Grant, 5V TTL compatible |
| nCS | T27 | I | Host Chip Select, 5V tolerant, on board pull-up resistor |
| REDY | T24 | O | DSP ready for Host Transfer, 5V TTL compatible, on board pull-up |

**POWER SUPPLY**

| Signal | Pin | Type | Description |
|---|---|---|---|
| VCC (+3.3V) | A1, B32 | P | power supply, use either A1/B1 or A32/B32 pin pair to avoid loops |
| GND | A32, B1 | P | power supply, use either A1/B1 or A32/B32 pin pair to avoid loops |
| +AVCC | C17, U1 | P | additional supply pins to route a positive analogue power supply line to a daughter module stacked on top of the DSP module, not connected |
| -AVCC | C15, U31 | P | additional supply pins to route a negative analogue power supply line to a daughter module stacked on top of the DSP module, not connected |
| AGND | C16, U32 | P | additional supply pins to route a 0V analogue power supply line to a daughter module stacked on top of the DSP module, not connected |
| VCC5 | T1,V1 | P | additional supply pins to route a 5V power supply line to a daughter module stacked on top of the DSP module, not connected |
| GND5 | T32, V32 | P | additional supply pins to route a 0V power supply line to a daughter module stacked on top of the DSP module, connected to GND |

## MECHANICAL DIMENSIONS




## ELECTRICAL CHARACTERISTICS

### OPERATING CONDITIONS, DC PARAMETERS

| | |
|---|---|
| Supply Voltage VCC | 3.3V +/- 5% |
| Power Consumption | idle: 140mA, max. TBD |
| Operating Temperature | 0..+70 °C |
| High Level Input Voltage | min. 2V, max. VCC+0.2V<br>max. 5.5V for 5V tolerant signals |
| Low Level Input Voltage | min. -0.2V, max. 0.8V |

Power Consumption largely depends on the selected clock frequency and the application. The idle power consumption is measured with the module held in reset, the maximum value is calculated based on Analog Devices data sheet information and experimental results.

**PINOUT**

| Pin | A | B | C | T | U | V |
|---|---|---|---|---|---|---|
| 1 | VCC (3.3V) | GND | | VCC5 *1 5V (nc) | +AVCC *1 (nc) | VCC5 *1 5V (nc) |
| 2 | RTS / nTxD | PRG_IO0 | | SDCLK0 *M | nRD | A6 |
| 3 | TxD | PRG_IO1 | | nSDRAS *M | nINT0 | A7 |
| 4 | CTS / nRxD | PRG_IO2 | | nSDCAS *M | nINT1 | A8 |
| 5 | RxD | PRG_IO3 | | nSDWE *M | nWR | A9 |
| 6 | GND | PRG_IO4 | | SDA10 *M | BUSCLK | A10 |
| 7 | DSPCLK | PRG_IO5 | | nMS1 | nRESOUT | A11 |
| 8 | GND | PRG_IO6 | | DQM *M | nIOSEL | A12 |
| 9 | nRESIN | PRG_IO7 | | SDCKE *M | A0 | A13 |
| 10 | nWAIT | PRG_IO8 | | ACK *M | A1 | A14 |
| 11 | IN0 | PRG_IO9 | | nMS0 *M | A2 | A15 |
| 12 | IN1 | PRG_IO10 | | nBMS *M | A3 | A16 |
| 13 | GND | PRG_IO11 | | nBR1 *M | A4 | A17 |
| 14 | A19 | PRG_IO12 | | nBR2 *M | A5 | A18 |
| 15 | A20 | PRG_IO13 | -AVCC | nSW *M | D16 | D0 |
| 16 | A21 | PRG_IO14 | AGND | nRESET *M | D17 | D1 |
| 17 | A22 *M | PRG_IO15 | +AVCC | FLAG6 | D18 | D2 |
| 18 | A23 *M | FLAG2 | | FLAG7 | D19 | D3 |
| 19 | nINT2 | FLAG3 | | FLAG8 | D20 | D4 |
| 20 | nc | FLAG4 | | FLAG9 | D21 | D5 |
| 21 | TIMER0 | FLAG5 | | FLAG10 | D22 | D6 |
| 22 | TIMER1 | DAT_RX0B | | FLAG11 | D23 | D7 |
| 23 | FLAG0 | DAT_TX0B | | nSBTS | D24 | D8 |
| 24 | FLAG1 | DAT_RX1B | | REDY | D25 | D9 |
| 25 | nc | DAT_TX1B | | nHBR | D26 | D10 |
| 26 | DAT_RX0 | DAT_RX1 | | nHBG | D27 | D11 |
| 27 | CLK_RX0 | CLK_RX1 | | nCS | D28 | D12 |
| 28 | FS_RX0 | FS_RX1 | | nDMAR1 | D29 | D13 |
| 29 | DAT_TX0 | DAT_TX1 | | nDMAG1 | D30 | D14 |
| 30 | CLK_TX0 | CLK_TX1 | | nDMAR2 | D31 | D15 |
| 31 | FS_TX0 | FS_TX1 | | nDMAG2 | -AVCC *1 (nc) | nMEMSEL |
| 32 | GND | VCC (3.3V) | | GND5 *1 (=GND) | AGND *1 (nc) | GND5 *1 (=GND) |

*1) these signals are provided for compatibility to the miniKit family of DSP boards only, do not use for new designs!

*M) these signals are provided for multiprocessing support only, do not make any connections except the related signals of a second ADSP-21065L !

**TIMINGS**

external bus: please refer to the Analog Devices ADSP-21065L data sheet MS2 and MS3 timings

serial interface and timer: please refer to the Analog Devices ADSP-21065L data sheet.

## ORDERING INFORMATION

| | |
|---|---|
| D.Module.21065-60-S0 | ADSP-21065L DSP Computer Module<br>180 MFLOPS, 256 kByte SRAM, 512 kByte Flash Memory |
| D.Module.21065-60-S1 | as above, but 1 MByte SRAM |
| D.Module.21065-60-S0-D0 | ADSP-21065L DSP Computer Module<br>180 MFLOPS, 256 kByte SRAM, 512 kByte Flash Memory, 16 MByte SDRAM |
| D.Module.21065-60-co | ADSP-21065L Co-Processor Module for Dual-Processor Systems |
| DS.21065 | Development Support Base Package<br>Support Software, BIOS license, CPLD library, Base Board, User's Guide and BIOS Reference Manual |
| ADDS-2106x-EZ-ICE | Analog Devices JTAG Emulator for PC (ISA Bus) |
| VDSP-2106x-PC | Analog Devices VisualDSP® integrated development environment (IDE) including Assembler, optimizing C-Compiler, Linker, Simulator, HLL-Debugger and Tools |

## ADDITIONAL OPTION ON VOLUME PURCHASE

For volume purchase D.SignT offers customer-specific modifications of the hardware either to reduce costs through reduced functionality or to increase functionality to meet the customers application requirements. Extensive experience in custom designs and the powerful engineering tools of our development department bring your application and our DSP know how together for your solution. Please contact D.SignT directly.

## TECHNICAL SUPPORT

Our products include free of charge technical support. You can reach the technical support by e-mail (support@dsignt.de) phone or fax.

## PRICING

Please ask for our current price list and volume discounts.

## AVAILABILITY

Our standard D.Modules are available typically ex-stock. For special modifications or non-standard D.Modules please consult our sales department.

## WARRANTY

All D.Modules come with 12 months warranty.



For additional information contact your local distributor who will also support you after your purchase or contact D.SignT directly.

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