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by Guy S. Perry III

CONTENTS

This application note focuses on minimal design changes required by the replacement of the DSP56002 by a DSP56303 in a system. Because the DSP56300 is a rich product family, this document also addresses considerations that facilitate future migration to other DSP56300 devices, where applicable. It includes configuration register settings.

Note: For details on the software differences between the DSP56002 and DSP56303, refer to the application note *AN1829/D*, which covers the differences in the instruction pipeline, the instruction cache controller, and the instruction set. It also covers differences in core modules—such as the arithmetic logic unit and address generation unit—and differences in the programming model. *AN1830/D* compares DSP56002 and DSP56303 hardware differences.

Hardware and configuration differences must be considered when a DSP56002-based system is redesigned to use the DSP56303. The significant differences are described in **Table 1**.

Table 1. DSP56002 and DSP56303 Differences Overview

Category	DSP56002	DSP56303
Package	• 132-pin plastic quad flat pack (PQFP) • 144-pin thin quad flat pack (TQFP) • 132-pin ceramic pin grid array (PGA)	• 144-pin thin quad flat pack (TQFP) • 196-pin molded-array plastic ball grid array (MAP-BGA)
Power	5 V device supports 5 V I/O	3.3 V device supports 3.3 or 5 V I/O
PLL/clock	CKOUT = EXTAL when PLL disabled; low power divider range 2^0–2^{15}; 2 clocks per instruction minimum	CLKOUT = EXTAL/2 when PLL disabled; low power divider range 2^0–2^7; includes predivider (1–16); one clock per instruction minimum
External Bus	24-bit data bus, 16-bit address bus, no DRAM support, assumes DSP is master	24-bit data bus, 18-bit address bus, glueless DRAM support, assumes external device is master
Mode Control/ Interrupts	Three mode/interrupt signals	Four mode/interrupt signals
Host Interface	Single strobe, single host request with interface to external DMA controller	Single/double strobe, single/double host request that can use internal DMA controller
Synchronous Serial Interface (SSI)	One interface on Port C with gated clock mode available	Two interfaces Port C and D with no gated clock mode
Serial Communications Interface (SCI)	One interface incorporated with SSI into Port C	One interface configured as Port E
Timer	One with seven operating modes	Three, each with ten operating modes
Debugging	OnCE™ module with direct access	JTAG TAP to internal OnCE module

Because of these differences, you may wish to perform a complete system hardware redesign to take full advantage of the added functionality provided by the DSP56303 or other members of the DSP56300 family. In that case, refer directly to the *DSP5630x Technical Data* sheet and related documentation for detailed specifications and design recommendations.

1 Package Type Descriptions

The 196-pin MAP-BGA packaged device is strongly recommended for new DSP56303 designs. It is signal-pin compatible with more-advanced, higher-performance members of the DSP56300 family.

Since the internal module functionality and signals/pinouts differ between the two devices, a pin-for-pin comparison between the package layouts is of little value. Instead, this document describes the functional differences between respective modules and, for each signal function used in the DSP56002, indicates the pin connection and requirements for connecting to the DSP56303, thus simplifying direct conversion of existing DSP56002 designs.

2 Power Supply

To convert a DSP56002 design to a DSP56303 design, the power circuits must be able to supply a 3.3 V nominal (3.0–3.6 V) supply for the DSP core and PLL. Systems using 5 V I/O devices do not need to change the design to use 3.3 V I/O devices with a DSP56303. However, conversion to 3.3 V I/O devices is recommended to accommodate future conversions to more advanced devices in the DSP56300 family. Motorola also recommends that the power come from a split power supply that can provide variable outputs, even if the design uses 3.3 V I/O. The more advanced DSP56300 devices use lower core/PLL voltage levels (1.8 or 1.6 V).

Refer to the *DSP56303 Technical Data* sheet for details on power requirements. As noted in that document, DSP56303-based designs require at least six 0.01–0.1 µF bypass capacitors positioned as closely as possible to the four sides of the package to connect the V_{CC} power source to GND to minimize power supply-induced noise. **Table 2** summarizes the power and ground connections by package type.

Table 2. DSP56303 Power and Ground Connections

Signal	MAP-BGA Package Ball Location	TQFP Package Pins
V_{CC}	A7, C7, C9, C11, D14, E2, F12, G13, H2, H12, K1, K12, L12, M4, N9, N19, P9	8, 18, 25, 38, 56, 57, 65, 74, 80, 86, 91, 95, 103, 111, 119, 126, and 129
V_{CCP}	M6	45
GND	D4, D5, D6, D7, D8, D9, D10, D11, E4, E5, E6, E7, E8, E9, E10, E11, F4, F5, F6, F7, F8, F9, F10, F11, G4, G5, G6, G7, G8, G9, G10, G11, H4, H5, H6, H7, H8, H9, H10, H11, J4, J5, J6, J7, J8, J9, J10, J11, K4, K5, K6, K7, K8, K9, K10, K11, L4, L5, L6, L7, L8, L9, L10, and L11	9, 19, 26, 39, 54, 58, 66, 75, 81, 87, 90, 96, 104, 112, 120, 127, and 130
GND_P	N6	47
GND_{P1}	P6	48

Notes: Isolate the PLL power (V_{CCP}, GND_P, and GND_{P1}) from the other power connections (V_{CC} and GND).

3 Phase-Lock Loop (PLL) and Clocking

There are several key differences between the DSP56002 and DSP56303 PLL and clock circuits. **Figure 1** illustrates these differences. **Table 3** compares the different PLL elements shown in the block diagrams.

DSP56002 PLL Block Diagram
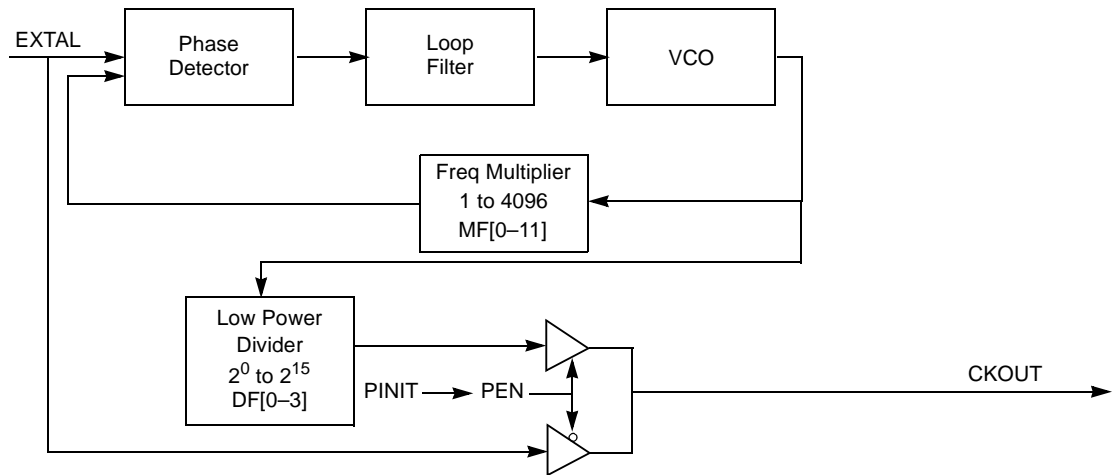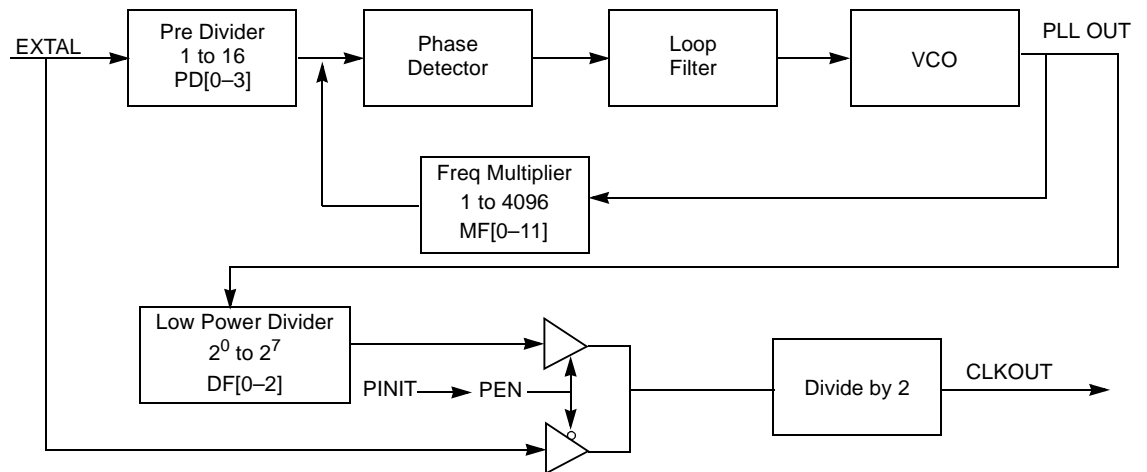
DSP56303 PLL Block Diagram

Figure 1. DSP56002/DSP56303 PLL Block Diagrams

Table 3.   Differences Between the PLL of the DSP56002 and DSP56303

DSP56002	DSP56303
Frequency Pre-divider Not Available	A **frequency pre-divider** is available on the DSP56303. This programmable division factor applies to the PLL input frequency and ranges from 1 to 16. The pre-divider factor bits PD[0–3] are written into bits 20–23 of the PLL Control Register (PCTL).
Fixed Divide by 2 Not Available	In the DSP56300 core, the output of the voltage-controlled oscillator (VCO) is **divided by 2**. This results in a constant $\times 2$ multiplication of the PLL clock output that generates the special chip clock phases.
The **low power divider** divides the output frequency of the VCO by any power of 2 from 2^0 to 2^{15}. The division factor bits DF[0–3] are written into bits 12–15 of the PCTL.	The clock generator performs the low power division. The **low power divider** divides the output frequency of the PLL by any power of 2 from 2^0 to 2^7. The division factor bits DF[0–2] are written into PCTL bits 12–14.

The **operating frequency** is governed by the frequency control bits in the PCTL as follows:
 	
$F_{002} = F_{EXT} \times MF / DF = F_{VCO} / DF$
 	
When the PLL is disabled, the internal chip clock and CKOUT are driven from the EXTAL input.
	The **operating frequency** is governed by the frequency control bits in the PCTL, as follows:
	
	$F_{303} = F_{EXT} \times MF / (PDF \times DF) = F_{VCO}/DF$
	
	where:
	    F_{CHIP} is the chip operating frequency.
	    F_{EXT} is the external input frequency (EXTAL)
	    MF is the multiplication factor defined by the MF[0–11] bits.
	    DF is the division factor defined by the DF[0–3] bits.
	    PDF is the pre-division factor defined by the PD[0–3] bits.
	    F_{VCO} is the output frequency of the VCO.
	
	When the PLL is disabled, the frequency of the CLKOUT is half the EXTAL input.

PLL Filter Capacitor The recommended PCAP value is: • 400 pF for MF $\leq$ 4, or • 540 pF for MF > 4. For example, if a 40 MHz crystal is used and the desired operating frequency is 40 MHz: $F_{002} = F_{EXT} \times MF / DF = 40$ MHz DF and MF should be set to 1. The PCAP value is 400 pF, since MF $\leq$ 4.	**PLL Filter Capacitor** The recommended PCAP value is: • $((500 \times MF) - 150)$ pF for MF $\leq$ 4, or • $(690 \times MF)$ pF for MF > 4. For example, if a 16.9344 MHz crystal is used and the desired operating frequency is approximately 68 MHz: $F_{303} = F_{EXT} \times MF / (PDF \times DF) = 68$ MHz $= 16.9344$ MHz $\times MF$ PDF and DF should be set to 1 and MF to 4. The PCAP is $((500 \times 4) - 150)$ pF = 1850 pF, since MF $\leq$ 4.
PLL Pins The Phase and Frequency Lock (PLOCK) pin is asserted when the PLL is enabled and has locked on the proper phase and frequency of EXTAL. The Clock Output Polarity Control (CKP) pin is an input that defines the polarity of the CKOUT clock output.	**PLL Pins** **PLOCK and CKP pins Not available**

Because the DSP56303 includes a divide-by-2 unit in its clock module, the same EXTAL input used with a DSP56002 design yields half the core frequency in a DSP56300 if the PLL is disabled. With the PLL enabled, the divide and multiply factors can be adjusted as required. For easy reference, **Table 4** lists the DSP56303 PLL and clock connections.

Table 4. DSP56303 PLL and Clock Connections

Signal	MAP-BGA Package Ball Location	TQFP Package Pins
EXTAL	M8	55
XTAL	M6	53
CLKOUT	M9	59
PCAP	P5	46
PINIT/$\overline{\text{NMI}}$	D1	6

Notes:	CLKOUT should be connected to the DSP56002 CKOUT line. To generate the same system frequency as the original design, review the clock and PLL configuration information in the *DSP56303 User's Manual*. Because the DSP56303 processes instructions twice as fast as the DSP56002 at the same core clock frequency, you must ensure that the core processor operation does not stall because of system I/O transfer rates and limitations.

4   External Bus

Both the DSP56002 and DSP56303 have an external 24-bit bus that permits access to external devices (memory and so forth). The DSP56002 address bus has 16 lines and the DSP56303 has 18 address lines. The bus control lines for the two devices share many signals, but there are significant differences that must be addressed in a system redesign. In addition, the two devices have different internal memory sizes.

4.1 External Bus Signals

For easy reference, **Table 5** lists the DSP56303 external bus connections.

Table 5. DSP56303 External Bus Connections

Signal	MAP-BGA Package Ball Location	TQFP Package Pins
A0	N14	72
A1	M13	73
A2	M14	76
A3	L13	77
A4	L14	78
A5	K13	79
A6	K14	82
A7	J13	83
A8	J12	84
A9	J14	85
A10	H13	88
A11	H14	89
A12	G14	92
A13	G12	93
A14	F13	94

External Bus

Table 5. DSP56303 External Bus Connections (Continued)

Signal	MAP-BGA Package Ball Location	TQFP Package Pins
A15	F14	97
A16[1]	E13	98
A17[1]	E12	99
D0	E14	100
D1	D12	101
D2	D13	102
D3	C13	105
D4	C14	106
D5	B13	107
D6	C12	108
D7	A13	109
D8	B12	110
D9	A12	113
D10	B11	114
D11	A11	115
D12	C10	116
D13	B10	117
D14	A10	118
D15	B9	121
D16	A9	122
D17	B8	123
D18	C8	124
D19	A8	125
D20	B7	128
D21	B6	131
D22	C6	132
D23	A6	133
AA0/$\overline{\text{RAS0}}$[2,3]	N13	70
AA1/$\overline{\text{RAS1}}$[2,3]	P12	69
AA2/$\overline{\text{RAS2}}$[2,3]	P7	51
AA3/$\overline{\text{RAS3}}$[2,3]	N7	50
$\overline{\text{RD}}$	M12	68
$\overline{\text{WR}}$	M11	67
$\overline{\text{TA}}$[4]	P10	62
$\overline{\text{BR}}$[5]	N11	63
$\overline{\text{BG}}$[5]	P13	71
$\overline{\text{BB}}$[5]	P11	64
$\overline{\text{CAS}}$[2]	N8	52
BCLK	N10	60
$\overline{\text{BCLK}}$	M10	61

Table 5. DSP56303 External Bus Connections (Continued)

Signal	MAP-BGA Package Ball Location	TQFP Package Pins
Notes:	**1.** Since these signals are not available in the DSP56002, leave them unconnected. **2.** $\overline{RAS}$ and $\overline{CAS}$ are not needed since the DSP56002 does not have glueless DRAM support. Disable DRAM support in the DRAM configuration registers. See the *DSP56303 User's Manual* for details. **3.** The DSP56303 does not support the $\overline{PS}$, $\overline{DS}$, and X/$\overline{Y}$ signals used by the DSP56002 to enable external program and X and Y data memory. However, you can use the AAn lines as chip selects for the memories in a DSP56002 design. Ensure that the AA priority disable bit (APD) bit in the Operating Mode Register is cleared; this enables the AA priority scheme so that only one AAn line can be asserted at a time. Ensure that the system code is modified so that operations driving the $\overline{PS}$, $\overline{DS}$, and X/$\overline{Y}$ signal lines are changed to drive the appropriate AAn lines. Some system logic can be eliminated since you can specify a single line to select X or Y data memory instead of decoding the combination of $\overline{DS}$ and X/$\overline{Y}$. The AA pin is asserted if the address in the appropriate Address Attribute Register AAR[3–0] matches the external address and if the external access is aimed to a space that is enabled in the appropriate AAR register. This is specified by the Address to Compare BAC[11–0] bits and the Number of Address Bits to Compare BNC[3–0]. See the *DSP56303 User's Manual* for details. **4.** The $\overline{TA}$ signal performs the same function as the DSP56002 $\overline{WT}$ signal by adding hardware wait states to a transfer cycle controlled by an external device, but the active signal level is functionally reversed. That is, to extend a transaction cycle in a DSP56002 system, an external device asserts $\overline{WT}$ (holds it low) until the cycle is terminated, and then deasserts the signal. In a DSP56303 system, an external device deasserts the $\overline{TA}$ signal (holds it high) until the cycle is terminated, and then asserts it at the end of the cycle. Therefore, you can pass the $\overline{WT}$ input from a DSP56002 design through an inverter before connecting it to the $\overline{TA}$ input of the DSP56303 to achieve the same function. Note that in the DSP56303, you must set at least one wait state in the Bus Control Register. See the *DSP56303 User's Manual* for details. **5.** The DSP56002 uses the bus control signals $\overline{BS}$, $\overline{BR}$, $\overline{BG}$, and $\overline{BN}$ to access and control the external bus. The DSP56303 uses the bus control signals $\overline{BR}$, $\overline{BG}$, and $\overline{BB}$ to access and control the external bus, but the control direction is not the same. The DSP56002 assumes that it is normally the bus master; therefore, the $\overline{BR}$ signal is an input that allows an external device to request mastership of the bus and the $\overline{BG}$ signal is an output that indicates that bus mastership is granted. The DSP56303 assumes that there is normally an external bus master; therefore, the $\overline{BR}$ signal is an output requesting bus mastership and $\overline{BG}$ is an input signal indicating that mastership is granted. To accommodate this difference, use the following connections: • DSP56002 system $\overline{BR}$ input line through an inverter to the DSP56303 $\overline{BG}$ input • DSP56303 $\overline{BR}$ output to the DSP56002 system $\overline{BN}$ output line • DSP56303 $\overline{BB}$ connection to the DSP56002 system $\overline{BS}$ output line • DSP56303 $\overline{BB}$ connection through an inverter to the DSP56002 system $\overline{BG}$ output line	

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4.2 Internal Memory

Table 6 compares the internal memory of the DSP56002 and the DSP56303.

Table 6. Internal Memory

DSP56002 (24-bit words)			DSP56303 (default) (24-bit words)		
Program RAM	**X-data RAM**	**Y-data RAM**	**Program RAM**	**X-data RAM**	**Y-data RAM**
512	256	256	4 K	2 K	2 K
Program ROM	**X-data ROM**	**Y-data ROM**	**Program ROM**	**X-data ROM**	**Y-data ROM**
64	256	256	192	—	—

The DSP56002 PROM contains the bootstrap program, and the X-data ROM and Y-data ROM contain sine, A-law, and μ-law tables. In contrast, the DSP56303 Program ROM contains the bootstrap program and there is no X-data ROM or Y-data ROM.

Note: To emulate the DSP56002 functionality, load sine, A-law, and m-law tables into the appropriate X- and Y-data RAM space.

Although you can vary the DSP56303 Program RAM, X-data RAM, and Y-data RAM sizes, there is no reason to do so, since the default sizes are much larger than those provided by the DSP56002. You can also leave the instruction cache disabled because the DSP56002 does not support it.

Table 7 shows the off-chip memory expansion for each device.

Table 7. Off-Chip Memory Expansion

Memory Space	DSP56002 (24-bit words)	DSP56303 (24-bit words)
Program RAM	64 K	256 K in 24-bit addressing mode[1] or 64 K in 16-bit addressing mode[2]
X-data RAM	64 K	256 K in 24-bit addressing mode[1] or 64 K in 16-bit addressing mode[2]
Y-data RAM	64 K	256 K in 24-bit addressing mode[1] or 64 K in 16-bit addressing mode[2]
Notes: **1.** This is the maximum range using the basic eighteen address lines. **2.** Because the DSP56002 supports only 16-bit addressing, ensure that the initialization software selects 16-bit addressing mode in the DSP56303 for compatibility with the DSP56002 software.		

5   Mode Control, Interrupts, and Reset

This section compares the DSP56002 and DSP56303 operating mode initialization. It also compares interrupt processing because mode control and external interrupt requests are multiplexed using the same pin connections. **Table 8** lists the location of the MOD/$\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$ pins on the DSP56303.

Table 8.   DSP56303 MOD/$\overline{\text{IRQ}}$, $\overline{\text{NMI}}$, and $\overline{\text{RESET}}$ Connections

Signal	MAP-BGA Package Ball Location	TQFP Package Pins
MODA/$\overline{\text{IRQA}}$[1]	C4	137
MODB/$\overline{\text{IRQB}}$[1]	A5	136
MODC/$\overline{\text{IRQC}}$[1,2]	C5	135
MODD/$\overline{\text{IRQD}}$[3]	B5	134
PINIT/$\overline{\text{NMI}}$[4]	D1	6
$\overline{\text{RESET}}$	N5	44
$\overline{\text{TRST}}$[5]		
Notes:	**1.** MOD[A–C] signals are the equivalent of M[A–C] in the DSP56002. **2.** $\overline{\text{IRQC}}$ is not used on the DSP56002. After reset, pull this signal line up to ensure that no $\overline{\text{IRQC}}$ signal is generated, even as a function of noise. **3.** Neither the MODD nor the $\overline{\text{IRQD}}$ function is used is the DSP56002. After reset, pull this signal line up to ensure that no $\overline{\text{IRQD}}$ signal is generated, even as a function of noise. **4.** Instead of being multiplexed with MC as on the DSP56002, $\overline{\text{NMI}}$ is multiplexed with PINIT on the DSP56303. Connect the DSP56002 $\overline{\text{NMI}}$ signal line to PINIT/$\overline{\text{NMI}}$ on the DSP56303. **5.** $\overline{\text{TRST}}$ must be asserted with the $\overline{\text{RESET}}$ signal to ensure correct operation.	

5.1   Operating Modes

When a DSP56002 or DSP56303 leaves the reset state, it samples its mode pins and loads the values into corresponding values into the Operating Mode Register to set the initial operating mode or bootstrap source.

The DSP56002 uses three mode pins (M[A–C]) and the DSP56303 uses four mode pins (MOD[A–D]). **Table 9** shows the DSP56002 operating modes.

Table 9.   DSP56002 Operating Modes

Operating Mode	MC	MB	MA	Description
0	0	0	0	Single-Chip mode
1	0	0	1	Bootstrap from EPROM
2	0	1	0	Normal Expanded mode
3	0	1	1	Development mode
4	1	0	0	Reserved; if selected, defaults to mode 5
5	1	0	1	Bootstrap from host
6	1	1	0	Bootstrap from SCI
7	1	1	1	Reserved; if selected, defaults to mode 6

Table 10 shows the DSP56303 operating modes. For a complete description of the various modes, refer to the *DSP56303 User's Manual*.

Table 10. DSP56303 Operating Modes

Operating Mode	MODD	MODC	MODB	MODA	Description
0	pull high	0	0	0	Expanded mode
1	pull high	0	0	1	Bootstrap from byte-wide memory
2	pull high	0	1	0	Bootstrap from SCI
4	pull high	1	0	0	HI08 bootstrap in ISA/DSP5630x
5	pull high	1	0	1	HI08 bootstrap in HC11 non-multiplexed
6	pull high	1	1	0	HI08 bootstrap in 8051 multiplexed Bus
7	pull high	1	1	1	HI08 bootstrap in 68302 bus
8	pull high	0	0	0	Expanded mode

Table 11 shows the DSP56303 mode to select for a system based on the mode used by the DSP56002 in the original design.

Table 11. DSP56303 Operating Mode Selection for DSP56002-Based System Conversions

Original DSP56002 Mode	Equivalent DSP56303 Mode
0—Single chip mode	No equivalent (starting address not the same)
1—Bootstrap from EPROM	1—Bootstrap from byte-wide memory
2—Normal expanded mode	No equivalent (starting address not the same)
3—Development mode	No equivalent
4—Reserved, defaults to mode 5	5—Bootstrap from host interface (non-multiplexed)
5—Bootstrap from host interface	5—Bootstrap from host interface (non-multiplexed)
6—Bootstrap from SCI	2—Bootstrap from SCI
7—Reserved, defaults to mode 6	2—Bootstrap from SCI

Note: For code compatibility, ensure that when the DSP56303 initializes, the boot software sets the SC bit in the Status Register (SR) to select 16-bit addressing mode. See the *DSP56303 User's Manual* and the *DSP56300 Family Manual* for details.

5.2 Interrupt Addresses and Sources

The DSP56002 uses a fixed set of interrupt starting addresses. The DSP56300 core has a 24-bit read/write Vector Base Address (VBA) register that allows the interrupt starting address location to be variable; it is a combination of an offset address (which is fixed) added to a programmable base address. The VBA is referenced implicitly by interrupt processing or directly via the MOVEC instruction. **Table 12** shows the interrupt starting addresses and the interrupt priority level ranges for each interrupt source of both the DSP56002 (for which there is no VBA) and the DSP56303.

Table 12. Interrupt Starting Addresses and Sources

DSP56002			DSP56303		
Interrupt Starting Address	Interrupt Priority Level Range	Interrupt Source	Interrupt Starting Address	Interrupt Priority Level Range	Interrupt Source
$00	3	Hardware $\overline{\text{RESET}}$	VBA:$00	3	Hardware $\overline{\text{RESET}}$
$02	3	Stack Error	VBA:$02	3	Stack Error
$04	3	Trace	VBA:$04	3	Illegal Instruction
$06	3	SWI	VBA:$06	3	Debug Request Interrupt
$08	0–2	$\overline{\text{IRQA}}$	VBA:$08	3	Trap
$0A	0–2	$\overline{\text{IRQB}}$	VBA:$0A	3	Non–Maskable Interrupt $\overline{\text{NMI}}$
$0C	0–2	SSI Receive Data	VBA:$0C	3	Available for Host Command
$0E	0–2	SSI Receive Data w/ Exception Status	VBA:$0E	3	Available for Host Command
$10	0–2	SSI Transmit Data	VBA:$10	0–2	$\overline{\text{IRQA}}$
$12	0–2	SSI Transmit Data w/ Exception Status	VBA:$12	0–2	$\overline{\text{IRQB}}$
$14	0–2	SCI Receive Data	VBA:$14	0–2	$\overline{\text{IRQC}}$
$16	0–2	SCI Receive Data w/ Exception Status	VBA:$16	0–2	$\overline{\text{IRQD}}$
$18	0–2	SCI Transmit Data	VBA:$18	0–2	DMA Channel 0
$1A	0–2	SCI Idle Line	VBA:$1A	0–2	DMA Channel 1
$1C	0–2	SCI Timer	VBA:$1C	0–2	DMA Channel 2
$1E	3	Non-Maskable Interrupt $\overline{\text{NMI}}$	VBA:$1E	3	DMA Channel 3
$20	0–2	Host Receive Data	VBA:$20	0–2	DMA Channel 4
$22	0–2	Host Transmit Data	VBA:$22	0–2	DMA Channel 5
$24	0–2	Host Command	VBA:$24	0–2	TIMER 0 Compare
$26	0–2	Available for Host Command	VBA:$26	0–2	TIMER 0 Overflow
$28	0–2	Available for Host Command	VBA:$28	0–2	TIMER 1 Compare
$2A	0–2	Available for Host Command	VBA:$2A	0–2	TIMER 1 Overflow
$2C	0–2	Available for Host Command	VBA:$2C	0–2	TIMER 2 Compare
$2E	0–2	Available for Host Command	VBA:$2E	0–2	TIMER 2 Overflow
$30	0–2	Available for Host Command	VBA:$30	0–2	ESSI0 Receive Data

Table 12. Interrupt Starting Addresses and Sources (Continued)

DSP56002			DSP56303		
Interrupt Starting Address	Interrupt Priority Level Range	Interrupt Source	Interrupt Starting Address	Interrupt Priority Level Range	Interrupt Source
$32	0–2	Available for Host Command	VBA:$32	0–2	ESSI0 Receive Data with Exception Status
$34	0–2	Available for Host Command	VBA:$34	0–2	ESSI0 Receive Last Slot
$36	0–2	Available for Host Command	VBA:$36	0–2	ESSI0 Transmit Data
$38	0–2	Available for Host Command	VBA:$38	0–2	ESSI0 Transmit Data with Exception Status
$3A	0–2	Available for Host Command	VBA:$3A	0–2	ESSI0 Transmit Last Slot
$3C	0–2	Timer	VBA:$3C	0–2	Available for Host Command
$3E	3	Illegal Instruction	VBA:$3E	0–2	Available for Host Command
$40	0–2	Available for Host Command	VBA:$40	0–2	ESSI1 Receive Data
$42	0–2	Available for Host Command	VBA:$42	0–2	ESSI1 Receive Data with Exception Status
$44	0–2	Available for Host Command	VBA:$44	0–2	ESSI1 Receive Last Slot
$46	0–2	Available for Host Command	VBA:$46	0–2	ESSI1 Transmit Data
$48	0–2	Available for Host Command	VBA:$48	0–2	ESSI1 Transmit Data with Exception Status
$4A	0–2	Available for Host Command	VBA:$4A	0–2	ESSI1 Transmit Last Slot
$4C	0–2	Available for Host Command	VBA:$4C	0–2	Available for Host Command
4E	0–2	Available for Host Command	VBA:4E	0–2	Available for Host Command
$50	0–2	Available for Host Command	VBA:$50	0–2	SCI Receive Data
$52	0–2	Available for Host Command	VBA:$52	0–2	SCI Receive Data with Exception Status
$54	0–2	Available for Host Command	VBA:$54	0–2	SCI Transmit Data
$56	0–2	Available for Host Command	VBA:$56	0–2	SCI Idle Line
$58	0–2	Available for Host Command	VBA:$58	0–2	SCI Timer
$5A	0–2	Available for Host Command	VBA:$5A	0–2	Available for Host Command
$5C	0–2	Available for Host Command	VBA:$5C	0–2	Available for Host Command
$5E	0–2	Available for Host Command	VBA:$5E	0–2	Available for Host Command
$60	0–2	Available for Host Command	VBA:$60	0–2	Host Receive Data Full

Table 12. Interrupt Starting Addresses and Sources (Continued)

DSP56002			DSP56303		
Interrupt Starting Address	Interrupt Priority Level Range	Interrupt Source	Interrupt Starting Address	Interrupt Priority Level Range	Interrupt Source
$62	0–2	Available for Host Command	VBA:$62	0–2	Host Transmit Data Empty
$64	0–2	Available for Host Command	VBA:$64	0–2	Host Command
$66	0–2	Available for Host Command	VBA:$66	0–2	Available for Host Command
:	:	:	:	:	:
$7E	0–2	Available for Host Command	VBA:$7E	:	:
:			:	:	:
$FE			VBA:$FE	0–2	Available for Host Command

Note: Although there is some correspondence between the DSP56002 and DSP56303 interrupt starting addresses if VBA is equal to 0, there are still significant differences, partly because the DSP56303 supports peripherals that the DSP56002 does not. Take care when reviewing the system software to ensure that the correct interrupt handler is called for a specific function. In addition to the relocation of some handlers (for example, the SCI handler addresses are at $14–$1C in the DSP56002 and $50–$58 with VBA = 0 in the DSP56303), you must select one of the ESSI channels and one of the timers in the DSP56303 to perform the functions of the single SSI and timer in the DSP56002. Then reference the appropriate handler addresses for the selected functions.

5.3 Interrupt Priority

You can program interrupt priority levels for each on-chip peripheral device and for each external interrupt source under software control by writing to the interrupt priority register. Level 3 interrupts are non-maskable and have the highest priority; level 0 interrupts are maskable and have the lowest priority. **Table 13** shows the DSP56002 Interrupt Priority Register (IPR) configuration.

Table 13. DSP56002 Interrupt Priority Register

Bit No.	Bit Description	
23–18	Reserved	Read as zero
17–16	TIL[1–0]	Timer Interrupt Priority Level
15–14	SCL[1–0]	SCI Interrupt Priority Level
13–12	SSL[1–0]	SSI Interrupt Priority Level
11–10	HPL0	Host Interrupt Priority Level
9–6	Reserved	Read as zero
5–3	IBL[2–0]	$\overline{\text{IRQB}}$ Mode
2–0	IAL[2–0]	$\overline{\text{IRQA}}$ Mode

The DSP56303 has two interrupt priority registers. The IPR-C is dedicated to the DSP56300 core interrupt sources, and the IPR-P is dedicated to the DSP56303 peripherals. **Table 14** and **Table 15** show the bits of each interrupt priority register.

Table 14. DSP56303 Interrupt Priority Register C

Bit No.	Bit Name	
23–22	D5L[1–0]	DMA5 Interrupt Priority Level
21–20	D4L[1–0]	DMA4 Interrupt Priority Level
19–18	D3L[1–0]	DMA3 Interrupt Priority Level
17–16	D2L[1–0]	DMA2 Interrupt Priority Level
15–14	D1L[1–0]	DMA1 Interrupt Priority Level
13–12	D0L[1–0]	DMA0 Interrupt Priority Level
11–9	IDL[2–0]	$\overline{\text{IRQD}}$ Mode
8–6	ICL[2–0]	$\overline{\text{IRQC}}$ Mode
5–3	IBL[2–0]	$\overline{\text{IRQB}}$ Mode
2–0	IAL[2–0]	$\overline{\text{IRQA}}$ Mode

Table 15. DSP56303 Interrupt Priority Register P

Bit No.	Bit Name	
23–10	Reserved	Read as zero
9–8	T0L1–T0L0	Triple Timer Interrupt Priority Level
7–6	SCL1–SCL0	SCI Interrupt Priority Level
5–4	S1L1–S1L0	ESSI1 Interrupt Priority Level
3–2	S0L1–S0L0	ESSI0 Interrupt Priority Level
1–0	HPL1–HPL0	HI08 Interrupt Priority Level

Review the DSP56002 software, determine the programmed priority levels for the selected peripherals, and then modify the programming (based on the specific peripheral selection) of the interrupt priorities in the DSP56303 accordingly. For details, refer to the *DSP56303 User's Manual*.

6 Host Interface

The DSP56002 host interface supports only non-multiplexed buses operating in single-strobe and single host request mode. The DSP56303 HI08 host port supports non-multiplexed or multiplexed buses, single- or dual-strobe buses, and single- or double- host request bus modes. Therefore, the DSP56303 should be configured to match the DSP56002 functionality. The DSP56002 does not use the host interface signals in the same ways as the DSP56303. In addition, the DSP56002 supports DMA transfers for the host interface only, whereas the DSP56303 supports DMA transfers for several peripherals.

6.1 Host Interface Signal Locations

For connection reference, **Table 16** lists the location of the host interface pins on the DSP56303.

Table 16. DSP56303 Host Interface (HI08) Connections[1]

Signal	MAP-BGA Package Ball Location	TQFP Package Pins
H0/HAD0/PB0[2]	M5	43
H1/HAD1/PB1[2]	P4	42
H2/HAD2/PB2[2]	N4	41
H3/HAD3/PB3[2]	P3	40
H4/HAD4/PB4[2]	N3	37
H5/HAD5/PB5[2]	P2	36
H6/HAD6/PB6[2]	N1	35
H7/HAD7/PB7[2]	N2	34
HA0/$\overline{\text{HAS}}$/HAS/PB8[2]	M3	33
HA1/HA8/PB9[2]	M1	31
HA2/HA9/PB10[2]	M2	31
$\overline{\text{HCS}}$/HCS/HA10/PB13[3]	L1	30
HRW/$\overline{\text{HRD}}$/HRD/PB11[4]	J2	22
$\overline{\text{HDS}}$/HDS/$\overline{\text{HWR}}$/HWR/PB12[5]	J3	21
$\overline{\text{HREQ}}$/HREQ/$\overline{\text{HTRQ}}$/HTRQ/PB14[6]	K2	24
$\overline{\text{HACK}}$/HACK/$\overline{\text{HRRQ}}$/HRRQ/PB15[6]	J1	23

Notes:
1. The DSP56002 uses a $\overline{\text{HEN}}$ pin to enable the host interface and perform a chip-select function. The DSP56303 uses software to drive the HEN bit (6) in the Host Port Control Register (HPCR) to enable or disable the host interface. Ensure that the HEN bit is 1 to enable the port if your system uses the host interface. See note 3 for additional information about use of the $\overline{\text{HEN}}$ signal as a chip select for the host interface.

2. GPIO operation for these signals in the DSP56002 is the same as in the DSP56303, so if the GPIO functions are used for these pins, simply connect the appropriate lines from the DSP56002 design to the corresponding DSP56303 connections. If the host interface function is used, the Non-Multiplexed Host Bus mode must be selected (write a 0 to bit 11 of the HPCR). Then connect the H[0–7] and HA[0–2] lines from the DSP56002-based system to the respective signal connections on the DSP56303.

3. The GPIO function for this signal is the same in both devices. If the GPIO function is used, connect the PB13 line from the DSP56002-based system to this connection. If the host interface function is used, the Non-Multiplexed Host Bus mode must be selected (write a 0 to bit 11 of the HPCR). Ensure that the Host Chip Select signal polarity is configured as asserted low ($\overline{\text{HCS}}$) by writing a 0 to bit 13 of the HPCR. Then connect the $\overline{\text{HEN}}$ line from the DSP56002-based design to the $\overline{\text{HCS}}$ connection on the DSP56303.

4. The GPIO function for this signal is the same in both devices. If the GPIO function is used, connect the PB11 line from the DSP56002-based design to this connection. If the host interface function is used, the single data strobe mode must be selected (write a 0 to bit 12 of the HPCR). Then connect the HR/$\overline{\text{W}}$ line from the DSP56002-based design to the HRW connection on the DSP56303.

5. The GPIO function for this signal is the same in both devices. If the GPIO function is used, connect the PB12 line from the DSP56002-based design to this connection. If the host interface function is used, the select single data strobe mode by writing a 0 to bit 12 of the HPCR, and configure the host data strobe ($\overline{\text{HDS}}$) polarity as active low by writing a 0 to bit 9 of the HPCR. Since the DSP56002 uses the $\overline{\text{HEN}}$ signal as the data strobe, connect the $\overline{\text{HEN}}$ line from the DSP56002-based design to the $\overline{\text{HDS}}$ connection on the DSP56303.

6. The GPIO function for PB14 is the same in both devices; PB15 is not supported in the DSP56002, so if the host interface is not used in the design, tie this signal low to minimize input noise. If the host interface is used, select Single Host Request mode by writing 0 to bit 2 of the interface control register (ICR) and configure $\overline{\text{HREQ}}$ and $\overline{\text{HACK}}$ as active low by writing 0s to bits 14 and 15 or the HPCR, respectively. Then connect the $\overline{\text{HREQ}}$ and $\overline{\text{HACK}}$ lines from the DSP56002-based design to the respective connections on the DSP56303.

6.2 Host Interface Control Signals

As noted in **Table 16**, the DSP56002 host interface control signals do not operate in the same way as in the DSP56303. Refer to the notes in **Table 16** for a details on the signal differences.

6.3 Host Interface DMA Transfers

In the host interface registers, you can configure the DSP56002 host interface to work with an external DMA controller to transfer data to and from a host processor. **Section 5.3.6.3** of the *DSP56002 User's Manual* provides details on this type of configuration.

The DSP56303 does not support the external DMA controller directly. Instead, the DSP56303 provides an internal six-channel DMA controller to handle data transfers between the DSP internal memory and the HIO8, ESSI, SCI, timer, or external peripherals. While using the internal DMA controller may eliminate some external hardware, use of DMA transfer capability requires reworking of the configuration and data transfer programming. For details, refer to **Chapter 10** of the *DSP56300 Family Manual* and **Chapter 4** *Core Configuration* in the *DSP56303 User's Manual*. Configuration of the DMA Request Source (DRS[4–0]) field in the DMA Control Register is required to select the HI08 as the source of the DMA request.

The major difference between the DMA transfers is that in the DSP56002, the host interface is enabled for DMA transfers (and the size is specified at the same time) and then $\overline{\text{HREQ}}$ and $\overline{\text{HACK}}$ (as data strobe) are used to transfer data. In the DSP56303, the host receive data full (HRDF) or host transmit data empty (HTDE) bits in the Host Status Register (HSR) are used to trigger the DMA transfer when the DMA controller channel is enabled for the HI08.

7   Synchronous Serial Interface

The DSP56002 provides a single Synchronous Serial Interface (SSI). The DSP56303 has two independent and identical Enhanced Synchronous Serial Interfaces: ESSI0 and ESSI1. The ESSI enhances the Synchronous Serial Interface (SSI) of the DSP56000 family with network, audio, and general improvements. For connection reference, **Table 17** lists the location of the ESSI pins on the DSP56303.

Table 17. DSP56303 Synchronous Serial Interface (ESSI0 and ESSI1) Connections

Signal	MAP-BGA Package Ball Location	TQFP Package Pins
SC00/PC0	F3	12
SC01/PC1	D2	4
SC02/PC2	C1	3
SCK0/PC3	H3	17
SRD0/PC4	E3	7
STD0/PC5	E1	10
SC10/PD0	F2	11
SC11/PD1	A2	144
SC12/PD2	B2	143
SCK1/PD3	G1	16
SRD1/PD4	B1	1
STD1/PD5	C2	2

Table 17. DSP56303 Synchronous Serial Interface (ESSI0 and ESSI1) Connections

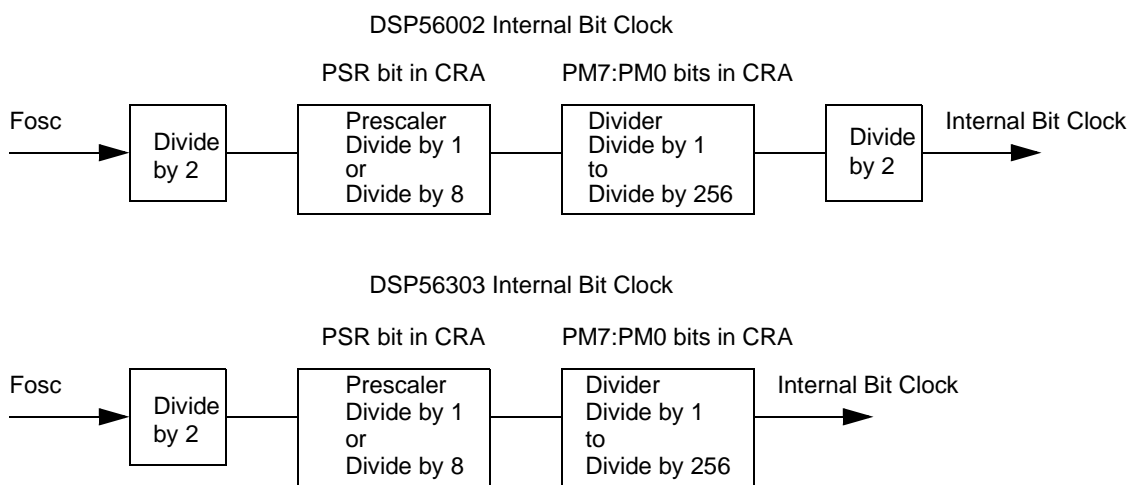| Signal	MAP-BGA Package Ball Location	TQFP Package Pins
Notes: The DSP56002 combines the SCI function with the SSI function as part of the GPIO Port C. Therefore, multiplexed GPIO functions referenced by a DSP56002-based design do not refer to the same GPIO signals as the DSP56303. If the GPIO signals are used, ensure that you know the configuration for each signal from the DSP56002 design and that the selected alternate signal from the DSP56303 is connected, configured, and referenced correctly by the DSP software. If the ESSI functionality is required, select either ESSI0 or ESSI1 and connect the signal lines from the DSP56002-based design (that is, SC0, SC1, SC2, SCK, SRD, and STD) to the respective signals on the selected ESSI.		

Note: Ensure that enhancements not supported by the DSP56002 are disabled in the configuration registers. Also ensure that the Time Slot Mask Registers are configured to allow all data to pass through the interface (default). ESSI network enhancements include time slot registers, the end-of-frame interrupt, and the drive enable signal. See the *DSP56303 User's Manual* for details.

7.1 Drive Enable Signal

When the Select SC1 as Transmitter 0 Drive Enable (SSC1) bit in the CRAx register is set, the SC1 signal acts as the driver enable of transmitter 0 while the SC1 signal is configured as output. This enables the use of an external buffer for the transmitter 0 output. When SSC1 is cleared, the ESSI is configured in synchronous mode, and transmitter 2 is disabled, the SC1 acts as the serial I/O flag and the SC1 signal is configured as output.

7.2 Internal Bit Clock

The divide-by-2 block in the DSP56002 SSI clock generator chain is absent in the DSP56303 ESSI clock generator. **Figure 2** shows the internal bit clock block diagram of each device. Ensure that the divider value in the DSP56303 CRA is set correctly to emulate the DSP56002 internal bit clock frequency.

DSP56002 Internal Bit Clock

Fosc → Divide by 2 → Prescaler Divide by 1 or Divide by 8 (PSR bit in CRA) → Divider Divide by 1 to Divide by 256 (PM7:PM0 bits in CRA) → Divide by 2 → Internal Bit Clock

DSP56303 Internal Bit Clock

Fosc → Divide by 2 → Prescaler Divide by 1 or Divide by 8 (PSR bit in CRA) → Divider Divide by 1 to Divide by 256 (PM7:PM0 bits in CRA) → Internal Bit Clock

Figure 2. DSP56002 and DSP56303 Internal Bit Clock Block Diagram

7.3   CRA Prescaler Range Bit Definition

In the DSP56002, when the Prescaler Range (PSR) bit in the CRA is set, the fixed divide-by-eight prescaler is operational. When PSR is cleared, the fixed prescaler is bypassed. In the DSP56303, the bit definition is reversed. When CRAx[PSR] is set, the fixed prescaler is bypassed. When CRAx[PSR] is cleared, the fixed divide-by-eight prescaler is bypassed. Ensure that the configuration of the selected ESSI takes the bit definition into account and selects the correct bit polarity to match the DSP56002 functionality.

7.4   Gated Clock Mode

In the DSP56002, the Gated Clock Control (GCK) bit in the CRB register selects between a continuously running data clock or a gated clock that runs only when there is data to be sent in the transmit shift register. This mode is not available in the DSP56303.

8   Serial Communications Interface

For connection reference, **Table 18** lists the location of the serial communications interface pins on the DSP56303.

Table 18.   DSP56303 Serial Communications Interface (SCI) Connections

Signal	MAP-BGA Package Ball Location	TQFP Package Pins
RXD/PE0	F1	13
TXD/PE1	G3	14
SCLK/PE2	G2	15
Notes: On the DSP56002, the SCI function is combined with the SSI function as part of the GPIO Port C. Therefore, multiplexed GPIO functions referenced by a DSP56002-based design do not refer to the same GPIO signals as the DSP56303. If the GPIO signals are used, determine the configuration for each signal from the DSP56002 design and ensure that the selected alternate signal from the DSP56303 is connected, configured, and referenced correctly by the DSP software. If the SCI functionality is required, connect the signal lines from the DSP56002-based design to the respective signals on the DSP56303 SCI.		

9   Timer

The DSP56002 provides a single timer module. The DSP56303 has a triple timer module that consists of a common 21-bit prescaler and three independent and identical general-purpose 24-bit timer/event counters, each with its own register set.

For connection reference, **Table 16** lists the location of the host interface pins on the DSP56303.

Table 19.   DSP56303 Timer Connections

Signal	MAP-BGA Package Ball Location	TQFP Package Pins
TIO0	L3	29
TIO1	L2	28
TIO2	K3	27
Notes: The DSP56002 provides one timer. Select one timer from the DSP56303 to perform the required timer functions, and disable the other two timers to minimize the possibility of internal noise generation.		

In the DSP56002, the Timer Control TC[2–0] bits in the Timer Control and Status Register (TCSR) control the source of the timer clock, the behavior of the TIO pin, and the timer mode of operation (see **Table 20**).

Table 20. DSP56002 Timer Modes of Operation

Bit Settings			Mode Characteristics			
TC2	TC1	TC0	Number	Name	TIO	Clock
0	0	0	0	Timer/GPIO	Input/Output	Internal
0	0	1	1	Timer Pulse	Output	Internal
0	1	0	2	Timer Toggle	Output	Internal
1	0	0	4	Pulse Width Measurement	Input	Internal
1	0	1	5	Period Measurement	Input	Internal
1	1	0	6	Standard Timer Counter	Input	External
1	1	1	7	Standard Timer	Input	External

In the DSP56303, the TC[3–0] bits in the TCSR[2–0] registers control the source of each timer clock, the behavior of the TIO signal, and the timer mode of operation. Whereas the DSP56002 supports only timer and measurement modes of operation, the DSP56303 also supports pulse-width modulation and watchdog modes of operation (see **Table 21**).

Table 21. DSP56303 Triple Timer Modes of Operation

Bit Settings				Mode Characteristics			
TC3	TC2	TC1	TC0	Number	Name	TIO	Clock
0	0	0	0	0	Timer/GPIO	Input/Output	Internal
0	0	0	1	1	Timer Pulse	Output	Internal
0	0	1	0	2	Timer Toggle	Output	Internal
0	0	1	1	3	Timer Event Counter	Input	External
0	1	0	0	4	Measurement Input Width	Input	Internal
0	1	0	1	5	Measurement Input Period	Input	Internal
0	1	1	0	6	Measurement Capture	Input	Internal
0	1	1	1	7	Pulse Width Modulation	Output	Internal
1	0	0	1	9	Watchdog Pulse	Output	Internal
1	0	1	0	10	Watchdog Toggle	Output	Internal

When converting a DSP56002-based design, notice that the Timer Modes 6 and 7 are defined differently in the DSP56303. If these modes are required, refer to the *DSP56303 User's Manual* to determine the best mode to use for the functionality required by your design.

10 Debugging

Unlike on the DSP56000 core, the DSP56300 core On-Chip Emulation (OnCE) functionality is accessed through the JTAG Test Access Port (TAP). Since the debugging interface is completely different, refer to the *DSP56303 User's Manual* and the *DSP56300 Family Manual* for details on the JTAG interface system design if this functionality is required.

HOW TO REACH US:

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