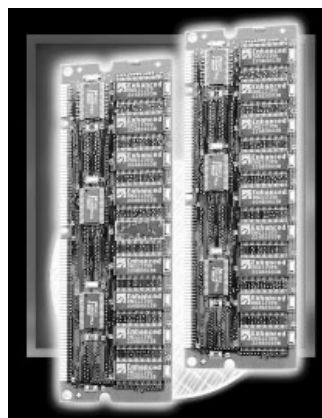![Enhanced Memory Systems Inc. logo]

Features

- 16Kbytes SRAM Cache Memory for 12ns Random Reads Within Eight Active Pages (Multibank Cache)
- Fast 8Mbyte DRAM Array for 30ns Access to Any New Page
- Write Posting Registers for 12ns Random Writes and Burst Writes Within a Page (Hit or Miss)
- 2Kbyte Wide DRAM to SRAM Bus for 113.8 Gigabytes/Second Cache Fill Rate
- On-chip Cache Hit/Miss Comparators Automatically Maintain Cache Coherency on Writes
- Hidden Precharge & Refresh Cycles
- Extended 64ms Refresh Period for Low Standby Power
- CMOS/TTL Compatible I/O and +5 Volt Power Supply
- Linear or Interleaved Burst Mode Configurable Without Mode Register Load Cycles
- Fast Page to Page Move or Read-Modify-Write Cycles
- Output Latch Enable Allows Extended Data Output (EDO) for Faster System Operation

Description

The Enhanced Memory Systems 8MB enhanced DRAM (EDRAM) DIMM module provides a single memory module solution for the main memory or local memory of fast 64-bit PCs, workstations, servers, and other high performance systems. Due to its fast non-interleave architecture, the EDRAM DIMM module supports zero-wait-state burst read or write operation to 100MHz. The EDRAM outperforms conventional SRAM plus DRAM or synchronous DRAM memory systems by minimizing wait states on initial reads (hit or miss) and eliminating writeback delays.

Each 8Mbyte DIMM module has 8Kbytes of SRAM cache organized as eight 256 x 72 row registers with 12ns initial access time. On a cache miss, the fast DRAM array reloads an entire 2Kbyte row register over a 2Kbyte-wide bus in just 18ns for an effective cache fill rate of 113.8 Gbytes/second. During write cycles, dual write posting registers allow the initial writes to be posted as early as 5ns after column address is available. EDRAM supports direct non-interleave page writes at greater than 83MHz. An on-chip hit/miss comparator automatically maintains cache coherency during writes.

The 8Mbyte DIMM module implements the following new features which can be implemented on new designs:

- An optional synchronous burst mode for up to 100MHz burst transfers.
- Concurrent random page write and cache reads from four cache pages allows fast page-to-page move or read-modify-write cycles.
- A controllable output latch provides an extended data output (EDO) mode.

Architecture

The DM1M72 achieves its 1Mb x 72 density by mounting 18 512Kx8 EDRAMs, packaged in low profile 44-pin TSOP-II packages on both sides of the multi-layer substrate. Six high drive series terminated buffer chips buffer address and control lines. Twenty-four surface mount capacitors are used to decouple the power supply bus. The DM1M64 contains 16 512Kx8 EDRAMs. The parity data components are not populated.

The EDRAM memory module architecture is very similar to two standard 4MB DRAM SIMM modules configured in a 64-bit wide, non-interleave configuration. The EDRAM module adds an integrated cache and cache control logic which allow the cache to operate much like a page mode or static column DRAM.

The EDRAM's SRAM cache is integrated into the DRAM array as tightly coupled row registers. Memory reads always occur from the 256 x 72 cache row register associated with a 1MB segment of DRAM. When the on-chip comparator detects a page hit, only the SRAM is accessed and data is available in 12ns from column address. When a page miss is detected, the entire new DRAM row is loaded into cache and data is available at the output within 30ns from row enable. Subsequent reads within a page (burst reads or random reads) will continue at 12ns cycle time. Since reads occur from the SRAM cache,

Functional Diagram
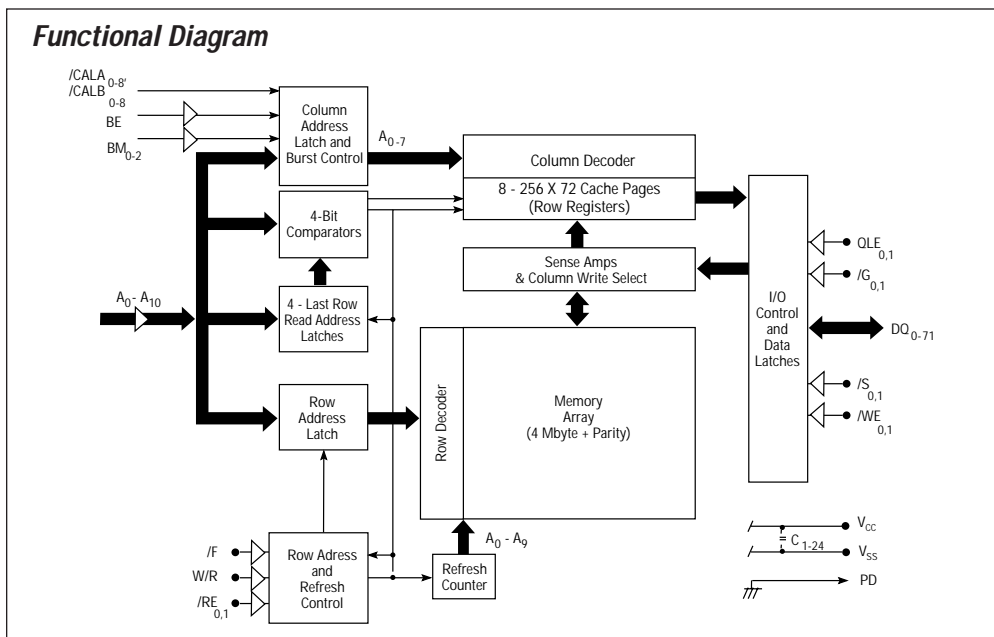
the DRAM precharge can occur simultaneously without degrading performance. The on-chip refresh counter with independent refresh bus allows the EDRAM to be refreshed during cache reads.

Memory writes can be posted as early as 6.5ns after row enable and are directed to the DRAM array. During a write hit, the on-chip address comparator activates a parallel write path to the SRAM cache to maintain coherency. Memory writes do not affect the contents of the cache row register except during write hits.

By integrating the SRAM cache as row registers in the DRAM array and keeping the on-chip control simple, the EDRAM is able to provide superior system performance at less cost, power, and area than systems implemented with complex synchronous SRAM cache, cache controllers, and multilevel data busses.

Functional Description

The EDRAM is designed to provide optimum memory performance with high speed microprocessors. As a result, it is possible to perform simultaneous operations to the DRAM and SRAM cache sections of the EDRAM. This feature allows the EDRAM to hide precharge and refresh operation during reads and maximize hit rate by maintaining page cache contents during write operations even if data is written to another memory page. These capabilities, in conjunction with the faster basic DRAM and cache speeds of the EDRAM, minimize processor wait states.

EDRAM Basic Operating Modes

The EDRAM operating modes are specified in the table.

Hit and Miss Terminology

In this datasheet, "hit" and "miss" always refer to a hit or miss to any of the four pages of data contained in the SRAM cache row registers. There are four cache row registers, one for each of the four banks of DRAM. These registers are specified by the bank select column address bits A_8 and A_9. The contents of these cache row registers is always equal to the last row that was read from each of the four internal DRAM banks (as modified by any write hit data).

Row And Column Addressing

Like common DRAMs, the EDRAM requires the address to be multiplexed into row and column addresses. Unlike other memories, the DM1M72 allows four read pages (DRAM pages duplicated in SRAM cache) and one write page to be active at the same time in each logical bank. To allow any of the four active cache pages to be accessed quickly, the row address bits A_{8-9} (DRAM bank selects) are also duplicated in the column address bits A_{8-9}. This allows any cache bank to be selected by simply changing the column address. The write bank address is specified by row address A_{8-9}, and writes are inhibited when a different column bank select is enabled.

Four Bank Cache Architecture (One of Two Banks)
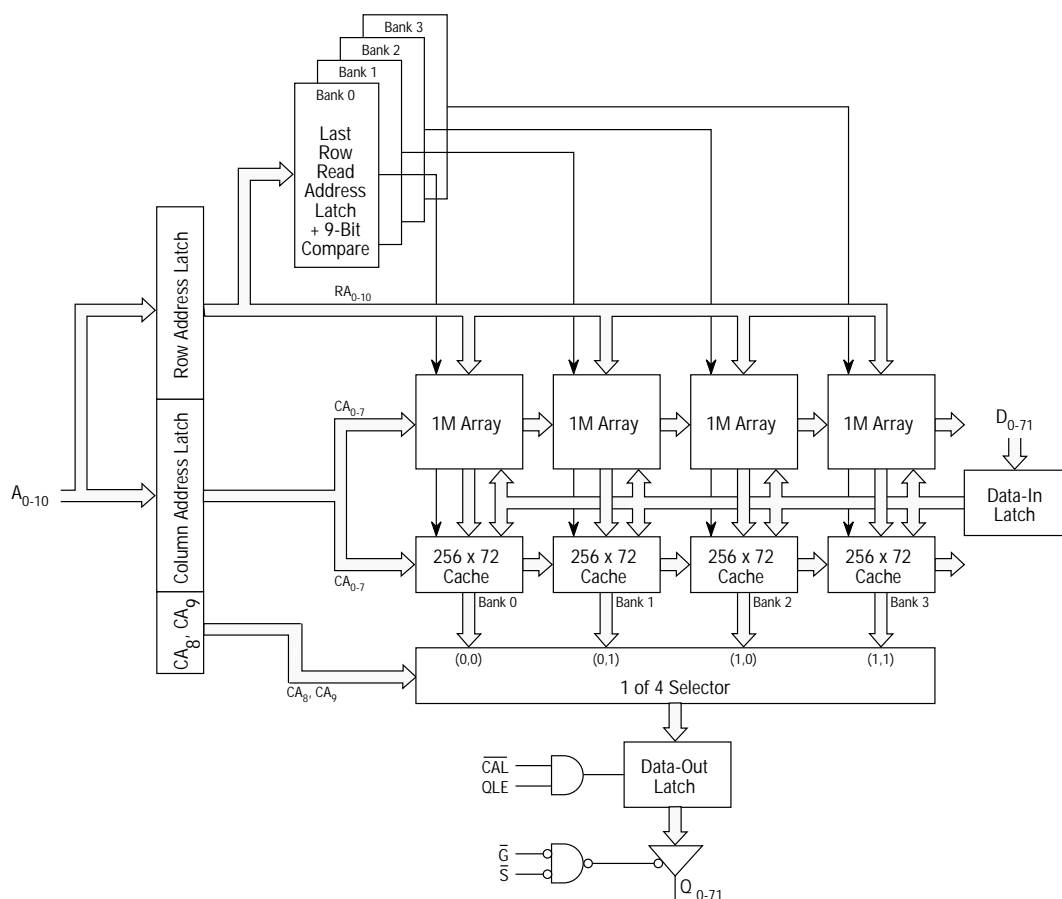
DRAM Read Hit

A DRAM read request is initiated by clocking /RE with W/R low and /F high. The EDRAM will compare the new row address to the last row read address latch for the bank specified by row address bits A_{8-9} (LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address matches the LRR, the requested data is already in the SRAM cache and no DRAM memory reference is initiated. The data specified by the row and column address is available at the output pins at the greater of times t_{AC} or t_{CQV}. Since no DRAM activity is initiated, /RE can be brought high after time t_{RE1}, and a shorter precharge time, t_{RP1}, is required. Additional locations within the currently active page may be accessed concurrently with precharge by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address change in static column mode. During any read cycle, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address. In page mode, data valid time is determined by either t_{AC} and t_{CQV}.

DRAM Read Miss

A DRAM read request is initiated by clocking /RE with W/R low and /F high. The EDRAM will compare the new row address to the LRR address latch for the bank specified by row address bits A_{8-9} (LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address does not match the LRR, the requested data is not in SRAM cache and a new row is fetched from the DRAM. The EDRAM will load the new row data into the SRAM cache and update the LRR latch. The data at the specified column address is available at the output pins at the greater of times t_{RAC}, t_{AC}, and t_{CQV}. /RE may be brought high after time t_{RE} since the new row data is safely latched into SRAM cache. This allows the EDRAM to precharge the DRAM array while data is accessed from SRAM cache. Additional locations within the currently active page may be accessed by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address change in static column mode. During any read cycle, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address. In page mode, data valid time is determined by either t_{AC} and t_{CQV}.

DRAM Write Hit

A DRAM write request is initiated by clocking /RE while W/R, /WE, and /F are high. The EDRAM will compare the new row address to the LRR address latch for the bank specified by row address A_{8-9} (LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address matches the LRR, the EDRAM will write data to both the DRAM page in the specified bank and its corresponding SRAM cache simultaneously to maintain coherency. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low. The write address and data can be latched very quickly after the fall of /RE ($t_{RAH} + t_{ASC}$ for the column address and t_{DS} for the data). During a write burst or any page write sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within the page can occur with write cycle time t_{PC}. With /G enabled and /WE disabled, cache read operations may be performed while /RE is activated. This allows random read from any of the four cache pages and random write, read-modify-write, or write-verify to the current write page with 12ns cycle times. To perform internal memory-to-memory transfers, /WE can be brought low while /G is low to latch the read data into the write posting register. The read/write transfer is complete when the new write column address is latched by bringing /CAL low concurrently with /WE. At the end of any write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. Reads can be performed from any of the cache pages concurrently with precharge by providing the desired column address and column bank select bits CA_{8-9} to the multiplex address inputs. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, the /CAL input can be used as a byte write select in multi-chip systems. If /CAL is not clocked on a write sequence, the memory will perform an /RE only refresh to the selected row and data will remain unmodified. Writes are inhibited for any write having a column address bank select different from the bank selected by the row address.

DRAM Write Miss

A DRAM write request is initiated by clocking /RE while W/R, /WE, and /F are high. The EDRAM will compare the new row address to the LRR address latch for the bank specified by row address A_{8-9} (LRR: a 9-bit row address latch for each internal DRAM bank which is

EDRAM Basic Operating Modes

Function	/S	/RE	W/R	/F	A_{0-10}	Comment
Read Hit	L	↓	L	H	Row = LRR	No DRAM Reference, Data in Cache
Read Miss	L	↓	L	H	Row ≠ LRR	DRAM Row to Cache
Write Hit	L	↓	H	H	Row = LRR	Write to DRAM and Cache, Reads Enabled
Write Miss	L	↓	H	H	Row ≠ LRR	Write to DRAM, Cache Not Updated, Reads Disabled
Internal Refresh	X	↓	X	L	X	
Low Power Standby	H	H	X	X	X	Standby Current
Unallowed Mode	H	L	X	H	X	

H = High; L = Low; X = Don't Care; ↓ = High-to-Low Transition; LRR = Last Row Read

reloaded on each /RE active read miss cycle). If the row address does not match the LRR, the EDRAM will write data only to the DRAM page in the appropriate bank and the contents of the current cache is not modified. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low. The write address and data can be latched very quickly after the fall of /RE ($t_{RAH} + t_{ASC}$ for the column address and t_{DS} for the data). During a write burst or any page write sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within the page can occur with write cycle time t_{PC}. With /G enabled and /WE disabled, cache read operations may be performed while /RE is activated. This allows random read accesses from any of the four cache pages and random writes to the current write page with 12ns cycle times. To perform internal memory-to-memory transfers, /WE can be brought low while /G is low to latch the read data into the write posting register. The read/ write transfer is complete when the new write column address is latched by bringing /CAL low concurrently with /WE. At the end of any write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. Reads can be performed from any of the cache pages concurrently with precharge by providing the desired column address and column bank select bits CA_{8-9} to the multiplex address inputs. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, /CAL can be used as a byte write select in multi-chip systems. If /CAL is not clocked on a write sequence, the memory will perform an /RE only refresh to the selected row and data will remain unmodified. Writes are inhibited for any write having a column address bank select different from the bank selected by the row address.

/RE Inactive Operation

Data may be read from any of the four SRAM cache pages without clocking /RE. This capability allows the EDRAM to perform cache read operations during precharge and refresh cycles to minimize wait states. It is only necessary to select /S and /G and provide the appropriate column address to read data as shown in the table below. In this mode of operation, the cache reads may occur from any of the four pages as specified by column bank select bits CA_{8-9}. To perform a cache read in static column mode, /CAL is held high, and the cache contents at the specified column address will be valid at time t_{AC} after address is stable. To perform a cache read in page mode, /CAL is clocked to latch the column address.

This option allows the external logic to perform fast hit/miss comparison so that the time required for row/column multiplexing is avoided.

Function	/S	/G	/CAL	A_{0-7}
Cache Read (Static Column)	L	L	H	Col Adr
Cache Read (Page Mode)	L	L	↕	Col Adr

EDO Mode and Output Latch Enable Operation

The QLE and /CAL inputs can be used to create extended data output (EDO) mode timings in either static column or page modes. The DM1M72 EDRAM has an output latch enable (QLE) for each logical bank that can be used to extend the data output valid time. The output latch enable operates as shown in the following table.

When QLE is low, the latch is transparent and the EDRAM operates identically to the standard EDRAMs. When /CAL is high during a static column mode read, the QLE input can be used to latch the output to extend the data output valid time. QLE can be held high

during page mode reads, In this case, the data outputs are latched while /CAL is high and open when /CAL is not high.

When output data is latched and /S goes high, data does not go Hi-Z until /G is disabled or either QLE or /CAL goes low to unlatch data.

QLE	/CAL	Comments
L	X	Output Transparent
↕	H	Output Latched When QLE=H (Static Column EDO)
H	↕	Output Latched When /CAL=H (Page Mode EDO)

Burst Mode Operation

Burst mode provides a convenient method for high speed sequential reading or writing of data. To enter burst mode, the starting address, a burst enable signal (BE) and burst mode information (BM_{0-2}) as shown in the following table must be provided. Random accesses using external addresses or new burst sequences may be performed after a burst sequence is terminated.

To start a burst cycle, BE must be brought high prior to the falling edge of /CAL. At the falling edge of /CAL, the EDRAM latches the

$BM_{2,1,0}$	Burst Type	Wrap Length	Address Sequence
0-0-0	Linear	2	0-1 1-0
0-0-1	Linear	4	0-1-2-3 1-2-3-0 2-3-0-1 3-0-1-2
0-1-0	Linear	8	0-1-2-3-4-5-6-7 1-2-3-4-5-6-7-0 2-3-4-5-6-7-0-1 3-4-5-6-7-0-1-2 4-5-6-7-0-1-2-3 5-6-7-0-1-2-3-4 6-7-0-1-2-3-4-5 7-0-1-2-3-4-5-6
0-1-1	Linear	Full Page	(B)(S),(B)(S+1),… (B)(255),(B)(0),…
1-0-0	Interleaved (Scrambled)	2	0-1 1-0
1-0-1	Interleaved (Scrambled)	4	0-1-2-3 1-0-3-2 2-3-0-1 3-2-1-0
1-1-0	Interleaved (Scrambled)	8	0-1-2-3-4-5-6-7 1-0-3-2-5-4-7-6 2-3-0-1-6-7-4-5 3-2-1-0-7-6-5-4 4-5-6-7-0-1-2-3 5-4-7-6-1-0-3-2 6-7-4-5-2-3-0-1 7-6-5-4-3-2-1-0
1-1-1	Linear	All Pages	(B)(S),(B)(S+1),… (B)(255),(B+1)(0),…

NOTES: a) B=Bank Address, S=Starting Column Address;

        b) For $BM_{2,1,0}$=111, wrap length is 1,024 8-bit words with 256 8-bit words for each of the four cache blocks. During read or write sequences, the address count will switch from bank to bank after column address 256. Write operations, however, will only occur when the internally generated bank address A_8 and A_9 matches the row address A_8 and A_9 that were loaded when /RE went low.

starting address and the states of the burst mode pins (BM_{0-2}) which define the type and wrap length of the burst. Once a burst sequence has been started, the internal address counter increments with each low to high transition of /CAL. Burst mode is terminated immediately when either BE goes low or /S goes high (/S must not go high while /RE is low). Burst mode must be terminated before a subsequent burst sequence can be initiated. Furthermore, the state of the address counter is indeterminate following a burst termination and must be reloaded for a subsequent burst operation. Burst reads may be performed from any of the four cache pages and may occur with /RE either active or inactive. As with all writes, however, burst writes may only be performed to the currently active write page (defined by the row address) while /RE is active.

Burst mode may be used with or without output latch enable operation. If burst mode is not used, BE and BM_{0-2} may be tied to ground to disable the burst function.

Write-Per-Bit Operation

The DM1M72 DIMM provides a write-per-bit capability to selectively modify individual parity bits ($DQ_{8, 17, 26, 35, 44, 53, 62, 71}$) for byte write operations. The parity devices (DM2233) is selected via /CALA$_8$, /CALB$_8$. Byte write selection to non-parity bits is accomplished via /CALA$_{0-7}$, /CALB$_{0-7}$. The bits to be written are determined by a bit mask data word which is placed on the parity I/O data pins prior to clocking /RE. The logic one bits in the mask data select the bits to be written. As soon as the mask is latched by /RE, the mask data is removed and write data can be placed on the databus. The mask is only specified on the /RE transition. During page mode write operations, the same mask is used for all write operations.

ECC Operation

The DM1M72DTE-xxN supports error correction coding (ECC) by replacing the parity chips with normal DM2223 devices. This version does not support write-per-bit.

Internal Refresh

If /F is active (low) on the assertion of /RE, an internal refresh cycle is executed. This cycle refreshes the row address supplied by an internal refresh counter. This counter is incremented at the end of the cycle in preparation for the next /F refresh cycle. At least 1,024 /F cycles must be executed every 64ms. /F refresh cycles can be hidden because cache memory can be read under column address control throughout the entire /F cycle. /F cycles are the only active cycles during which /S can be disabled. /RE must be held high for 300ns prior to initialization.

/RE Only Refresh Operation

Although /F refresh using the internal refresh counter is the recommended method of EDRAM refresh, an /RE only refresh may be performed using an externally supplied row address. /RE refresh is performed by executing a *write cycle* (W/R and /F are high) where /CAL is not clocked. This is necessary so that the current cache contents and LRR are not modified by the refresh operation. All combinations of addresses A_{0-9} must be sequenced every 64ms refresh period. A_{10} does not need to be cycled. Read refresh cycles are not allowed because a DRAM refresh cycle does not occur when a read refresh address matches the LRR address latch.

Low Power Mode

The EDRAM enters its low power mode when /S is high. In this mode, the internal DRAM circuitry is powered down to reduce standby current.

Initialization Cycles

A minimum of eight /RE active initialization cycles (read, write, or refresh) are required before normal operation is guaranteed. Following these start-up cycles, two read cycles to different row addresses must be performed for each of the four internal banks of DRAM to initialize the internal cache logic. Row address bits A_8 and A_9 define the four internal DRAM banks.

Unallowed Mode

Read, write, or /RE only refresh operations must not be performed to unselected memory banks by clocking /RE when /S is high.

Reduced Pin Count Operation

Although it is desirable to use all EDRAM control pins to optimize system performance, the interface to the EDRAM may be simplified to reduce the number of control lines by either tying pins to ground or tying one or more control inputs together. The /S input can be tied to ground if low power standby mode is not required. The QLE input can be tied low if output latching is not required, or tied high if "extended data out" (hyper page mode) is required. BE can be tied low if burst operation is not desired. The W/R and /G inputs can be tied together if reads are not required during a write cycle. The simplified control interface still allows the fast page read/write cycle times, fast random read/write times, and hidden precharge functions available with the EDRAM.

Pin Descriptions

/RE$_{0,1}$ — Row Enable

This input is used to initiate DRAM read and write operations and latch a row address. It is not necessary to clock /RE to read data from the EDRAM SRAM row registers. On read operations, /RE can be brought high as soon as data is loaded into cache to allow early precharge.

/CALA$_{0-8}$, /CALB$_{0-8}$ — Column Address Latch

These inputs are used to latch the column address and in combination with /WE to trigger write operations. When /CAL is high, the column address latch is transparent. When /CAL is low, the column address latch contains the address present at the time /CAL went low. Individual /CAL inputs are provided for each byte of each bank of EDRAM to allow byte write capability.

W/R — Write/Read

This input along with /F input specifies the type of DRAM operation initiated on the low going edge of /RE. When /F is high, W/R specifies either a write (logic high) or read operation (logic low).

/F — Refresh

This input will initiate a DRAM refresh operation using the internal refresh counter as an address source when it is low on the low going edge of /RE.

/WE$_{0,1}$ — Write Enable

This input controls the latching of write data on the input data pins. A write operation is initiated when both /CAL for the specified byte and /WE are low.

/BE — Burst Enable

This input is used to enable and disable the burst mode function.

/BM$_{0-2}$ — Burst Mode

These input pins define the burst type and address wrap around length during burst reads and write transfers.

/G_{0,1} — Output Enable

This input controls the gating of read data to the output data pins during read operations.

/S_{0,1} — Chip Select

This input is used to power up the I/O and clock circuitry. When /S is high, the EDRAM remains in a powered-down condition. Read or write cycles must not be executed when /S is high. /S must remain low throughout any read or write operation. Only /F refresh operation can be executed when /S is not enabled.

DQ_{0-71} — Data Input/Output

These CMOS/TTL bidirectional data pins are used to read and write data to the EDRAM. On the DM2233 write-per-bit memory, these pins are also used to specify the bit mask used during write operations.

A_{0-10} — Multiplex Address

These inputs are used to specify the row and column addresses of the EDRAM data. The 11-bit row address is latched on the falling edge of /RE. The 10-bit column address can be specified at any other time to select read data from the SRAM cache or to specify the write column address during write cycles.

$QLE_{0,1}$ — Output Latch Enable

This input enables the EDRAM output latch. When QLE is low, the output latch is transparent. Data is latched when both /CAL and QLE are high. This allows output data to be extended during either static column or page mode read cycles.

PD — Presence Detect

This output will indicate if the DIMM module is inserted in a socket. When a DIMM is inserted, this pin is grounded. When no DIMM is present, the pin is open.

V_{CC} Power Supply

These inputs are connected to the +5 volt power supply.

V_{SS} Ground

These inputs are connected to the power supply ground connection.

Pin Names

Pin Names	Function
A_{0-10}	Address Inputs
$/RE_{0,1}$	Row Enable
DQ_{0-71}	Data In/Data Out
$/CALA_{0-8}$, $/CALB_{0-8}$	Column Address Latch
W/R	Write/Read Control
V_{CC}	Power (+5V)
V_{SS}	Ground

Pin Names	Function
$/WE_{0,1}$	Write Enable
$/G_{0,1}$	Output Enable
/F	Refresh Control
$/S_{0,1}$	Chip Select
BE	Burst Enable
BM_{0-2}	Burst Mode Control
$QLE_{0,1}$	Output Latch Enable
NC	Not Connected

Absolute Maximum Ratings
(Beyond Which Permanent Damage Could Result)

Description	Ratings
Input Voltage (V_{IN})	- 1 ~ V_{CC}+1
Output Voltage (V_{OUT})	- 1 ~ V_{CC}+1
Power Supply Voltage (V_{CC})	- 1 ~ 7v
Ambient Operating Temperature (T_A)	-40 ~ +70°C
Storage Temperature (T_S)	-55 ~ 150°C
Static Discharge Voltage (Per MIL-STD-883 Method 3015)	Class 1
Short Circuit O/P Current (I_{OUT})	50mA*

* One output at a time; short duration.

Capacitance

Description	Max	Pins
Input Capacitance	18pf	A_{0-10}
Input Capacitance	18pf	$/CAL_{0-8}$
Input Capacitance	12pf	/G, QLE
Input Capacitance	18pf	W/R, /F
I/O Capacitance	20pf	DQ_{0-71}
Input Capacitance	16pf	/RE, /S
Input Capacitance	16pf	BE, BM_{0-2}

AC Test Load and Waveforms V_{IN} Timing Reference Point at V_{IL} and V_{IH} V_{OUT} Timing Referenced to 1.5 Volts

5.0V
$R_1 = 828\Omega$
Output
$R_2 = 295\Omega$ $C_L = 50pf$

V_{IH} V_{IH}
V_{IL} V_{IL}
GND
≤5ns   ≤5ns
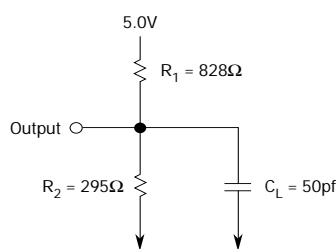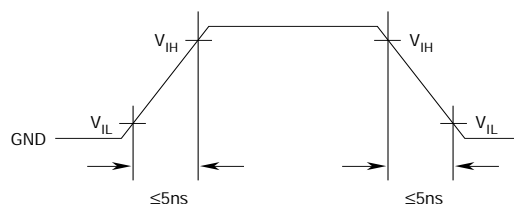
Load Circuit   **Input Waveforms**

Pinout

Pin No.	Function	Interconnect (Component Pin)	Organization	Pin No.	Function	Interconnect (Component Pin)	Organization
1	Vss		Ground	85	V_{SS}		Ground
2	DQ_0	U1-4, U21-4	Byte 0, I/O 0	86	DQ_{36}	U2-4, U20-4	Byte 4, I/O 0
3	DQ_1	U1-6, U21-6	Byte 0, I/O 1	87	DQ_{37}	U2-6, U20-6	Byte 4, I/O 1
4	DQ_2	U1-7, U21-7	Byte 0, I/O 2	88	DQ_{38}	U2-7, U20-7	Byte 4, I/O 2
5	DQ_3	U1-9, U-21-9	Byte 0, I/O 3	89	DQ_{39}	U2-9, U20-9	Byte 4 I/O 3
6	V_{DD}		+5 Volts	90	V_{DD}		+5 Volts
7	DQ_4	U1-13, U21-13	Byte 0, I/O 4	91	DQ_{40}	U2-13, U20-13	Byte 4 I/O 4
8	DQ_5	U1-15, U21-15	Byte 0, I/O 5	92	DQ_{41}	U2-15, U20-15	Byte 4 I/O 5
9	DQ_6	U1-16, U21-16	Byte 0, I/O 6	93	DQ_{42}	U2-16, U20-16	Byte 4, I/O 6
10	DQ_7	U1-18, U21-18	Byte 0, I/O 7	94	DQ_{43}	U2-18, U20-18	Byte 4, I/O 7
11	DQ_8	U5-4, U17-4	Parity, I/O 0	95	DQ_{44}	U5-13, U17-13	Parity, I/O 4
12	V_{SS}		Ground	96	V_{SS}		Ground
13	DQ_9	U3-4, U19-4	Byte 1, I/O 0	97	DQ_{45}	U4-4, U18-4	Byte 5, I/O 0
14	DQ_{10}	U3-6, U19-6	Byte 1, I/O 1	98	DQ_{46}	U4-6, U18-6	Byte 5, I/O 1
15	DQ_{11}	U3-7, U19-7	Byte 1, I/O 2	99	DQ_{47}	U4-7, U18-7	Byte 5, I/O 2
16	DQ_{12}	U3-9, U19-9	Byte 1, I/O 3	100	DQ_{48}	U4-9, U18-9	Byte 5, I/O 3
17	DQ_{13}	U3-13, U19-13	Byte 1, I/O 4	101	DQ_{49}	U4-13, U18-13	Byte 5, I/O 4
18	V_{DD}		+5 Volts	102	V_{DD}		+5 Volts
19	DQ_{14}	U3-15, U19-15	Byte 1, I/O 5	103	DQ_{50}	U4-15, U18-15	Byte 5, I/O 5
20	DQ_{15}	U3-16, U19-16	Byte 1 I/O 6	104	DQ_{51}	U4-16, U18-16	Byte 5, I/O 6
21	DQ_{16}	U3-18, U19-18	Byte 1 I/O 7	105	DQ_{52}	U4-18, U18-18	Byte 5, I/O 7
22	DQ_{17}	U5-6, U17-6	Parity, I/O 1	106	DQ_{53}	U5-15, U17-15	Parity, I/O 5
23	V_{SS}		Ground	107	V_{SS}		Ground
24	V_{SS}		Ground	108	V_{SS}		Ground
25	V_{DD}		+5 Volts	109	V_{DD}		+5 Volts
26	V_{DD}		+5 Volts	110	V_{DD}		+5 Volts
27	$/WE_0$	U10A-8	Write Enable, Bank 0	111	/F	U10D-49, U24C-36	Refresh Pin
28	/CALA0	U1-32	Byte 0 /CAL, Bank 0	112	/CALA1	U3-32	Byte 1 /CAL, Bank 0
29	/CALA2	U6-32	Byte 2 /CAL, Bank 0	113	/CALA3	U8-32	Byte 3 /CAL, Bank 0
30	$/S_0$	U10A-14	Chip Select, Bank 0	114	$/S_1$	U24B-15	Chip Select, Bank 1
31	$/G_0$	U10B-15	Output Enable, Bank 0	115	W/R	U10D-43, U24C-42	Write/Read Mode
32	V_{SS}		Ground	116	V_{SS}		Ground
33	A_0	U10B-21, U24A-8	Address 0	117	A_1	U10C-42, U24D-43	Address 1
34	A_2	U11A-8, U23B-21	Address 2	118	A_3	U10C-36, U24D-49	Address 3
35	A_4	U11A-14, U23B-15	Address 4	119	A_5	U11D-49, U23C-36	Address 5
36	A_6	U11B-15, U23A-14	Address 6	120	A_7	U11D-43, U23C-42	Address 7
37	A_8	U11B-21, U23A-8	Address 8	121	A_9	U11C-42, U23D-43	Address 9
38	A_{10}	U11C-36, U23D-49	Address 10	122	N.C.		
39	N.C.			123	N.C.		
40	V_{DD}		+5 Volts	124	V_{DD}		+5 Volts
41	V_{DD}		+5 Volts	125	QLE_1	U22B-21	Output Latch Enable, Bank 1
42	QLE_0	U12A-8	Output Latch Enable, Bank 0	126	N.C.	N.C.	

Pinout

Pin No.	Function	Interconnect (Component Pin)	Organization	Pin No.	Function	Interconnect (Component Pin)	Organization
43	V_{SS}		Ground	127	V_{SS}		Ground
44	$/G_1$	U24A-14	Output Enable, Bank 1	128	V_{SS}		Ground
45	$/RE_0$	U12A-14	Row Enable, Bank 0	129	$/RE_1$	U22B-15	Row Enable, Bank 1
46	/CALA4	U2-32	Byte 4 /CAL, Bank 0	130	/CALA5	U4-32	Byte 5 /CAL, Bank 0
47	/CALA6	U7-32	Byte 6 /CAL, Bank 0	131	/CALA7	U9-32	Byte 7 /CAL, Bank 0
48	$/WE_1$	U24B-48	Write Enable, Bank 1	132	/CALA8	U5-32	Parity /CAL, Bank 0
49	V_{DD}		+5 Volts	133	V_{DD}		+5 Volts
50	V_{DD}		+5 Volts	134	V_{DD}		+5 Volts
51	V_{SS}		Ground	135	V_{SS}		Ground
52	DQ_{18}	U6-4, U16-4	Byte 2, I/O 0	136	DQ_{54}	U7-4, U15-4	Byte 6, I/O 0
53	DQ_{19}	U6-6, U16-6	Byte 2, I/O 1	137	DQ_{55}	U7-6, U15-6	Byte 6, I/O 1
54	V_{SS}		Ground	138	V_{SS}		Ground
55	DQ_{20}	U6-7, U16-7	Byte 2, I/O 2	139	DQ_{56}	U7-7, U15-7	Byte 6, I/O 2
56	DQ_{21}	U6-9, U16-9	Byte 2, I/O 3	140	DQ_{57}	U7-9, U15-9	Byte 6, I/O 3
57	DQ_{22}	U6-13, U16-13	Byte 2, I/O 4	141	DQ_{58}	U7-13, U15-13	Byte 6, I/O 4
58	DQ_{23}	U6-15, U16-15	Byte 2, I/O 5	142	DQ_{59}	U7-15, U15-15	Byte 6, I/O 5
59	V_{DD}		+5 Volts	143	V_{DD}		+5 Volts
60	DQ_{24}	U6-16, U16-16	Byte 2, I/O 6	144	DQ_{60}	U7-16, U15-16	Byte 6, I/O 6
61	PD		Ground	145	BM2	U12C-36, U22D-49	Burst Mode 2
62	$CALB_8$	U17-32	Parity /CAL, Bank 1	146	BM1	U12C-42, U22D-43	Burst Mode 1
63	BE	U12B-21, U22A-8	Burst Enable	147	BM0	U12B-15, U22A-14	Burst Mode 0
64	V_{SS}		Ground	148	V_{SS}		Ground
65	DQ_{25}	U6-18, U16-18	Byte 2, I/O 7	149	DQ_{61}	U7-18, U15-18	Byte 6, I/O 7
66	DQ_{26}	U5-7, U17-7	Parity, I/O 2	150	DQ_{62}	U5-16, U17-16	Parity, I/O 6
67	DQ_{27}	U8-4, U14-4	Byte 3, I/O 0	151	DQ_{63}	U9-4, U13-4	Byte 7, I/O 0
68	V_{SS}		Ground	152	V_{SS}		Ground
69	DQ_{28}	U8-6, U14-6	Byte 3, I/O 1	153	DQ_{64}	U9-4, U13-4	Byte 7, I/O 1
70	DQ_{29}	U8-7, U14-9	Byte 3, I/O 2	154	DQ_{65}	U9-7, U13-7	Byte 7, I/O 2
71	DQ_{30}	U8-9, U14-9	Byte 3, I/O 3	155	DQ_{66}	U9-9, U13-9	Byte 7, I/O 3
72	DQ_{31}	U8-13, U14-13	Byte 3, I/O 4	156	DQ_{67}	U9-13, U13-13	Byte 7, I/O 4
73	V_{DD}		+5 Volts	157	V_{SS}		+5 Volts
74	DQ_{32}	U8-15, U14-15	Byte 3, I/O 5	158	DQ_{68}	U9-15, U13-15	Byte 7, I/O 5
75	DQ_{33}	U8-16, U14-16	Byte 3, I/O 6	159	DQ_{69}	U9-16, U13-16	Byte 7, I/O 6
76	DQ_{34}	U8-18, U14-18	Byte 3, I/O 7	160	DQ_{70}	U9-18, U13-18	Byte 7, I/O 7
77	DQ_{35}	U5-9, U17-9	Parity, I/O 3	161	DQ_{71}		Parity, I/O 7
78	V_{SS}		Ground	162	V_{SS}		Ground
79	/CALB0	U21-32	Byte 0 /CAL, Bank 1	163	/CALB1	U19-32	Byte 1 /CAL, Bank 1
80	/CALB2	U16-32	Byte 2 /CAL, Bank 1	164	/CALB3	U14-32	Byte 3 /CAL, Bank 1
81	/CALB4	U20-32	Byte 4 /CAL, Bank 1	165	/CALB5	U18-32	Byte 5 /CAL, Bank 1
82	/CALB6	U15-32	Byte 6 /CAL, Bank 1	166	/CALB7	U13-32	Byte 7 /CAL, Bank 1
83	V_{DD}		+5 Volts	167	V_{DD}		+5 Volts
84	V_{DD}		+5 Volts	168	V_{DD}		+5 Volts

Buffer Diagrams

DIMM Edge
Connector

U12A

|42| QLE 0 8 —
- 2 QLE Bank0A
- 3 QLE Bank0B
- 5 QLE Bank0C
- 6 QLE Bank0D

|45| /RE0 14 —
- 9 /RE Bank0A
- 10 /RE Bank0B
- 12 /RE Bank0C
- 13 /RE Bank0D
- 1

U12D

43 —
- 48 N.C.
- 47 N.C.
- 45 N.C.
- 44 N.C.

49 —
- 55 N.C.
- 54 N.C.
- 52 N.C.
- 51 N.C.
- 58

U12B

|147| BM0 15 —
- 16 BMO Bank0A
- 17 BMO Bank0B
- 19 BMO Bank0C
- 20 BMO Bank0D

|63| BE 21 —
- 23 BE Bank0A
- 24 BE Bank0B
- 26 BE Bank0C
- 27 BE Bank0D
- 28

U11A

|34| A2 8 —
- 2 A2 Bank0A
- 3 A2 Bank0B
- 5 A2 Bank0C
- 6 A2 Bank0D

|35| A4 14 —
- 9 A4 Bank0A
- 10 A4 Bank0B
- 12 A4 Bank0C
- 13 A4 Bank0D
- 1

U12C

|145| BM2 36 —
- 34 BM2 Bank0A
- 33 BM2 Bank0B
- 31 BM2 Bank0C
- 30 BM2 Bank0d

|146| BM1 42 —
- 41 BM1 Bank0A
- 40 BM1 Bank0B
- 38 BM1 Bank0C
- 37 BM1 Bank0D
- 29

U11B

|36| A6 15 —
- 16 A6 Bank0A
- 17 A6 Bank0B
- 19 A6 Bank0C
- 20 A6 Bank0D

|37| A8 21 —
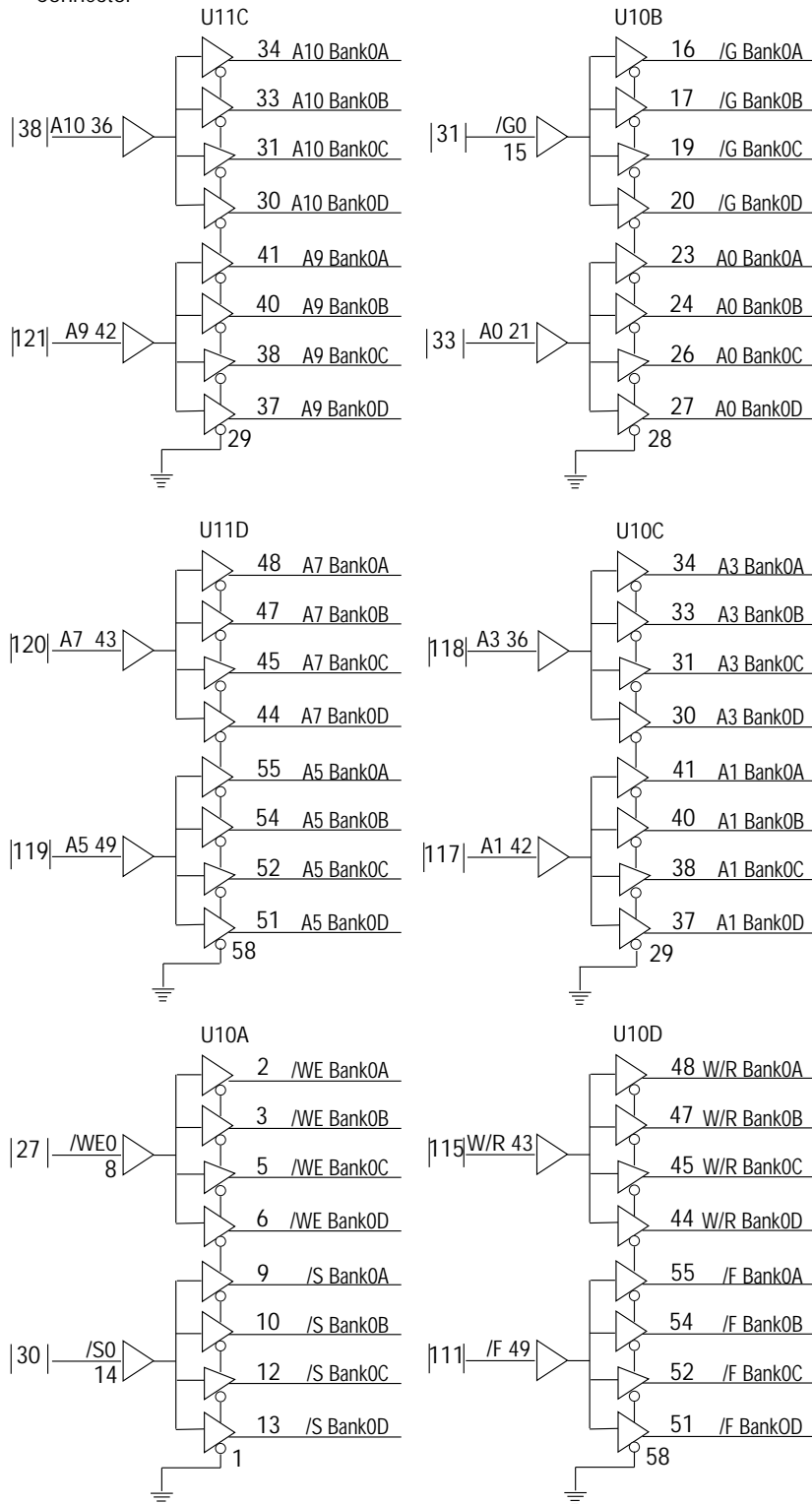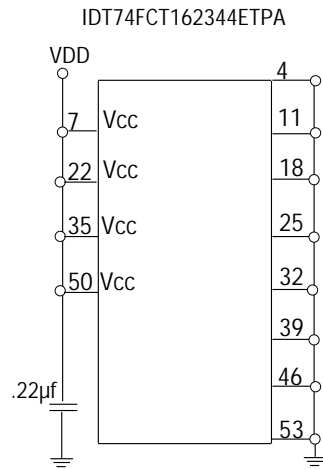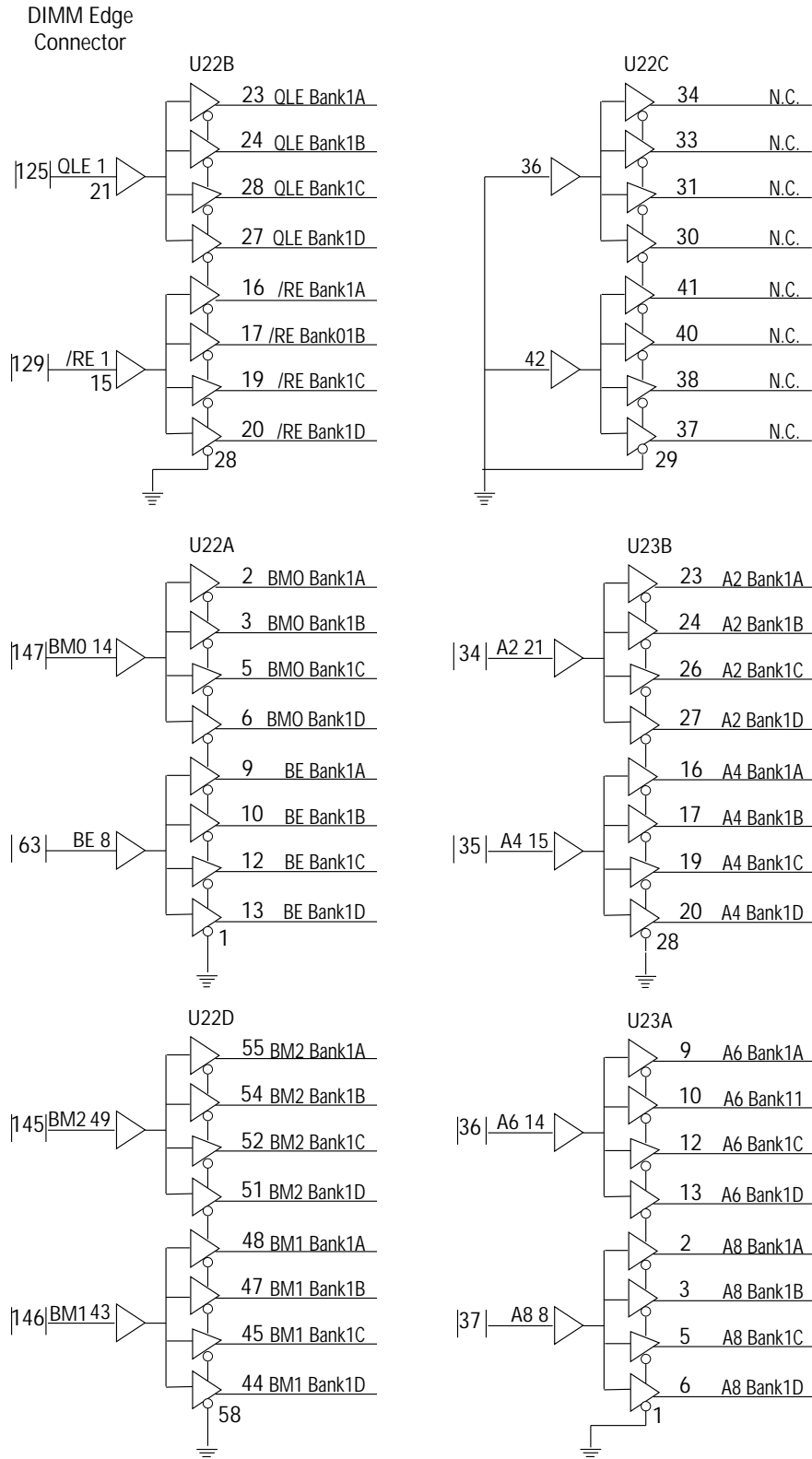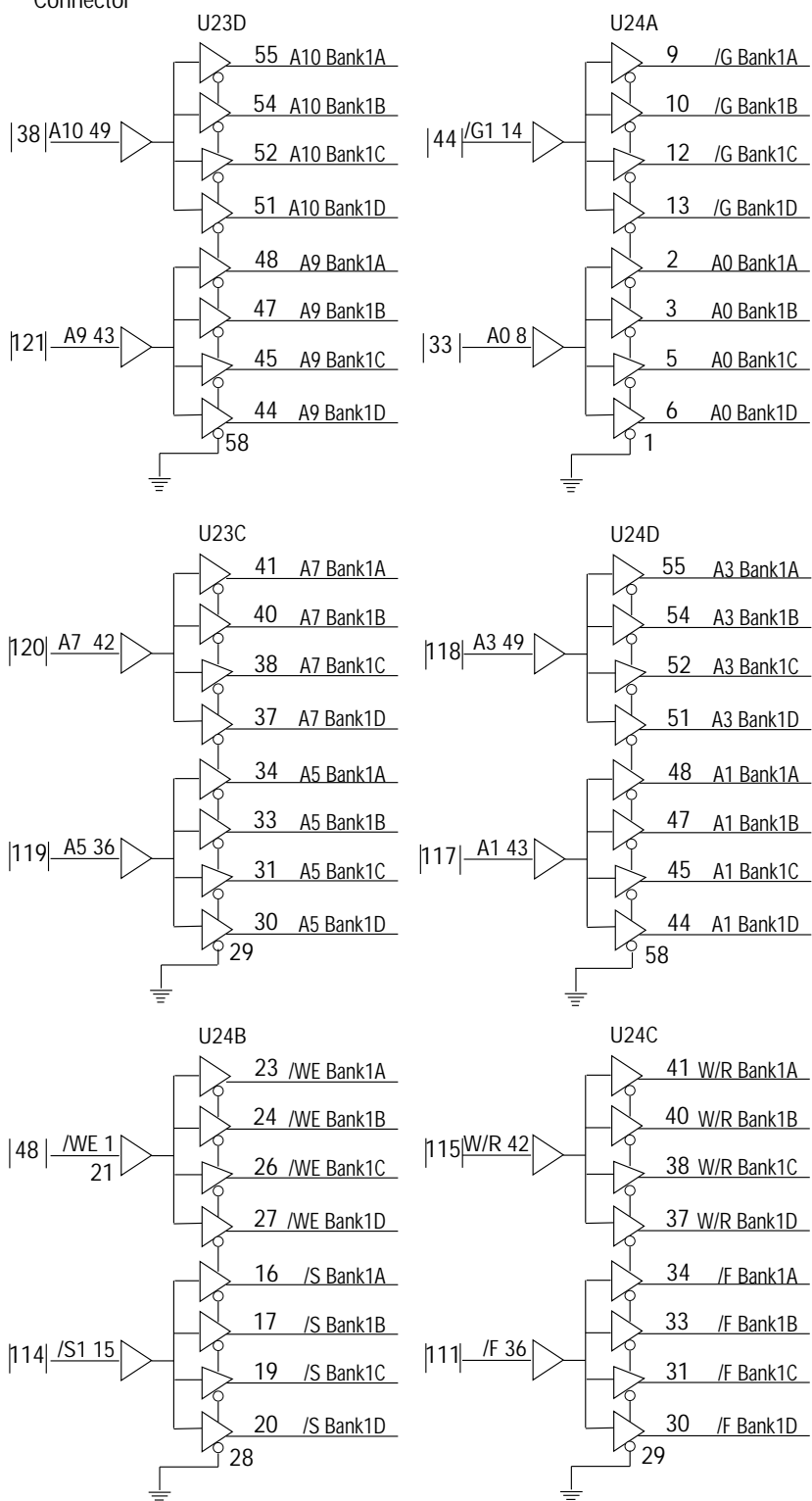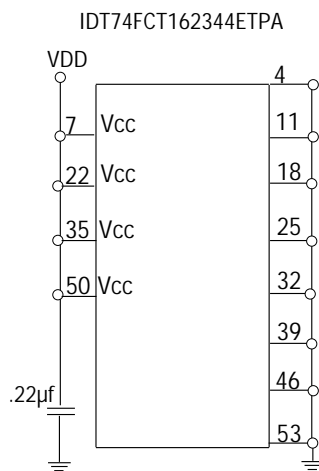- 23 A8 Bank0A
- 24 A8 Bank0B
- 26 A8 Bank0C
- 27 A8 Bank0D
- 28

Note: Address and control buffers add a minimum of 1.5ns and a maximum of 3.8ns delay to each signal path.
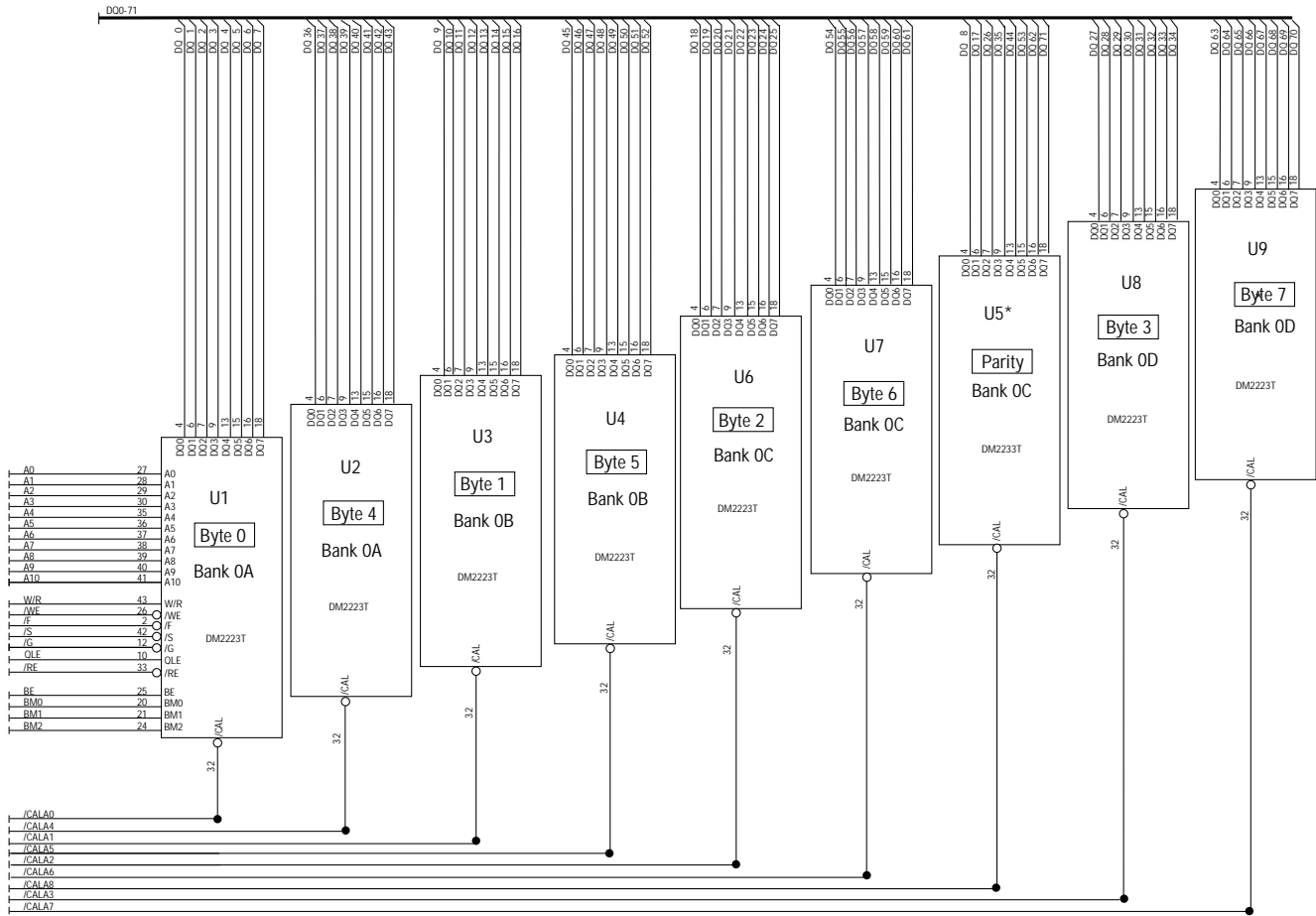
Buffer Diagrams

DIMM Edge
Connector

U11C

38	A10 36		

- 34 A10 Bank0A
- 33 A10 Bank0B
- 31 A10 Bank0C
- 30 A10 Bank0D

121	A9 42

- 41 A9 Bank0A
- 40 A9 Bank0B
- 38 A9 Bank0C
- 37 A9 Bank0D
- 29

U10B

31	/G0 15

- 16 /G Bank0A
- 17 /G Bank0B
- 19 /G Bank0C
- 20 /G Bank0D

33	A0 21

- 23 A0 Bank0A
- 24 A0 Bank0B
- 26 A0 Bank0C
- 27 A0 Bank0D
- 28

U11D

120	A7 43

- 48 A7 Bank0A
- 47 A7 Bank0B
- 45 A7 Bank0C
- 44 A7 Bank0D

119	A5 49

- 55 A5 Bank0A
- 54 A5 Bank0B
- 52 A5 Bank0C
- 51 A5 Bank0D
- 58

U10C

118	A3 36

- 34 A3 Bank0A
- 33 A3 Bank0B
- 31 A3 Bank0C
- 30 A3 Bank0D

117	A1 42

- 41 A1 Bank0A
- 40 A1 Bank0B
- 38 A1 Bank0C
- 37 A1 Bank0D
- 29

U10A

27	/WE0 8

- 2 /WE Bank0A
- 3 /WE Bank0B
- 5 /WE Bank0C
- 6 /WE Bank0D

30	/S0 14

- 9 /S Bank0A
- 10 /S Bank0B
- 12 /S Bank0C
- 13 /S Bank0D
- 1

U10D

115	W/R 43

- 48 W/R Bank0A
- 47 W/R Bank0B
- 45 W/R Bank0C
- 44 W/R Bank0D

111	/F 49

- 55 /F Bank0A
- 54 /F Bank0B
- 52 /F Bank0C
- 51 /F Bank0D
- 58

IDT74FCT162344ETPA

VDD

- 7 Vcc
- 22 Vcc
- 35 Vcc
- 50 Vcc

- 4
- 11
- 18
- 25
- 32
- 39
- 46
- 53

.22μf

Note: Address and control buffers add a minimum of 1.5ns and a maximum of 3.8ns delay to each signal path.

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DIMM Edge
Connector

U22B

| 125 | QLE 1 | 21

23 QLE Bank1A
24 QLE Bank1B
28 QLE Bank1C
27 QLE Bank1D

| 129 | /RE 1 | 15

16 /RE Bank1A
17 /RE Bank01B
19 /RE Bank1C
20 /RE Bank1D
28

U22C

36

34 N.C.
33 N.C.
31 N.C.
30 N.C.

42

41 N.C.
40 N.C.
38 N.C.
37 N.C.
29

U22A

| 147 | BM0 14

2 BM0 Bank1A
3 BM0 Bank1B
5 BM0 Bank1C
6 BM0 Bank1D

| 63 | BE 8

9 BE Bank1A
10 BE Bank1B
12 BE Bank1C
13 BE Bank1D
1

U23B

| 34 | A2 21

23 A2 Bank1A
24 A2 Bank1B
26 A2 Bank1C
27 A2 Bank1D

| 35 | A4 15

16 A4 Bank1A
17 A4 Bank1B
19 A4 Bank1C
20 A4 Bank1D
28

U22D

| 145 | BM2 49

55 BM2 Bank1A
54 BM2 Bank1B
52 BM2 Bank1C
51 BM2 Bank1D

| 146 | BM1 43

48 BM1 Bank1A
47 BM1 Bank1B
45 BM1 Bank1C
44 BM1 Bank1D
58

U23A

| 36 | A6 14

9 A6 Bank1A
10 A6 Bank11
12 A6 Bank1C
13 A6 Bank1D

| 37 | A8 8

2 A8 Bank1A
3 A8 Bank1B
5 A8 Bank1C
6 A8 Bank1D
1

Note: Address and control buffers add a minimum of 1.5ns and a maximum of 3.8ns delay to each signal path.

Buffer Diagrams

DIMM Edge
Connector

U23D

38	A10 49	55 A10 Bank1A
		54 A10 Bank1B
		52 A10 Bank1C
		51 A10 Bank1D

121	A9 43	48 A9 Bank1A
		47 A9 Bank1B
		45 A9 Bank1C
		44 A9 Bank1D

58

U24A

44	/G1 14	9 /G Bank1A
		10 /G Bank1B
		12 /G Bank1C
		13 /G Bank1D

33	A0 8	2 A0 Bank1A
		3 A0 Bank1B
		5 A0 Bank1C
		6 A0 Bank1D

1

U23C

120	A7 42	41 A7 Bank1A
		40 A7 Bank1B
		38 A7 Bank1C
		37 A7 Bank1D

119	A5 36	34 A5 Bank1A
		33 A5 Bank1B
		31 A5 Bank1C
		30 A5 Bank1D

29

U24D

118	A3 49	55 A3 Bank1A
		54 A3 Bank1B
		52 A3 Bank1C
		51 A3 Bank1D

117	A1 43	48 A1 Bank1A
		47 A1 Bank1B
		45 A1 Bank1C
		44 A1 Bank1D

58

U24B

48	/WE 1 21	23 /WE Bank1A
		24 /WE Bank1B
		26 /WE Bank1C
		27 /WE Bank1D

114	/S1 15	16 /S Bank1A
		17 /S Bank1B
		19 /S Bank1C
		20 /S Bank1D

28

U24C

115	W/R 42	41 W/R Bank1A
		40 W/R Bank1B
		38 W/R Bank1C
		37 W/R Bank1D

111	/F 36	34 /F Bank1A
		33 /F Bank1B
		31 /F Bank1C
		30 /F Bank1D

29

IDT74FCT162344ETPA

VDD

7 Vcc	4
22 Vcc	11
35 Vcc	18
50 Vcc	25
	32
	39
	46
	53

.22µf

Note: Address and control buffers add a minimum of 1.5ns and a maximum of 3.8ns delay to each signal path.

Interconnect Diagram - Bank 0 (Components on Front Side)

Note: For reference to buffer connection, append bank name to address or clock name, i.e., A10 + Bank 0A = A10BANK0A. Refer to Buffer Interconnect Diagram for detailed buffer connections. DQ0-71 and /CALA0-8 are directly connected to pins.

* Not Present on DM1M64

Interconnect Diagram - Bank 1 (Components on Back Side)
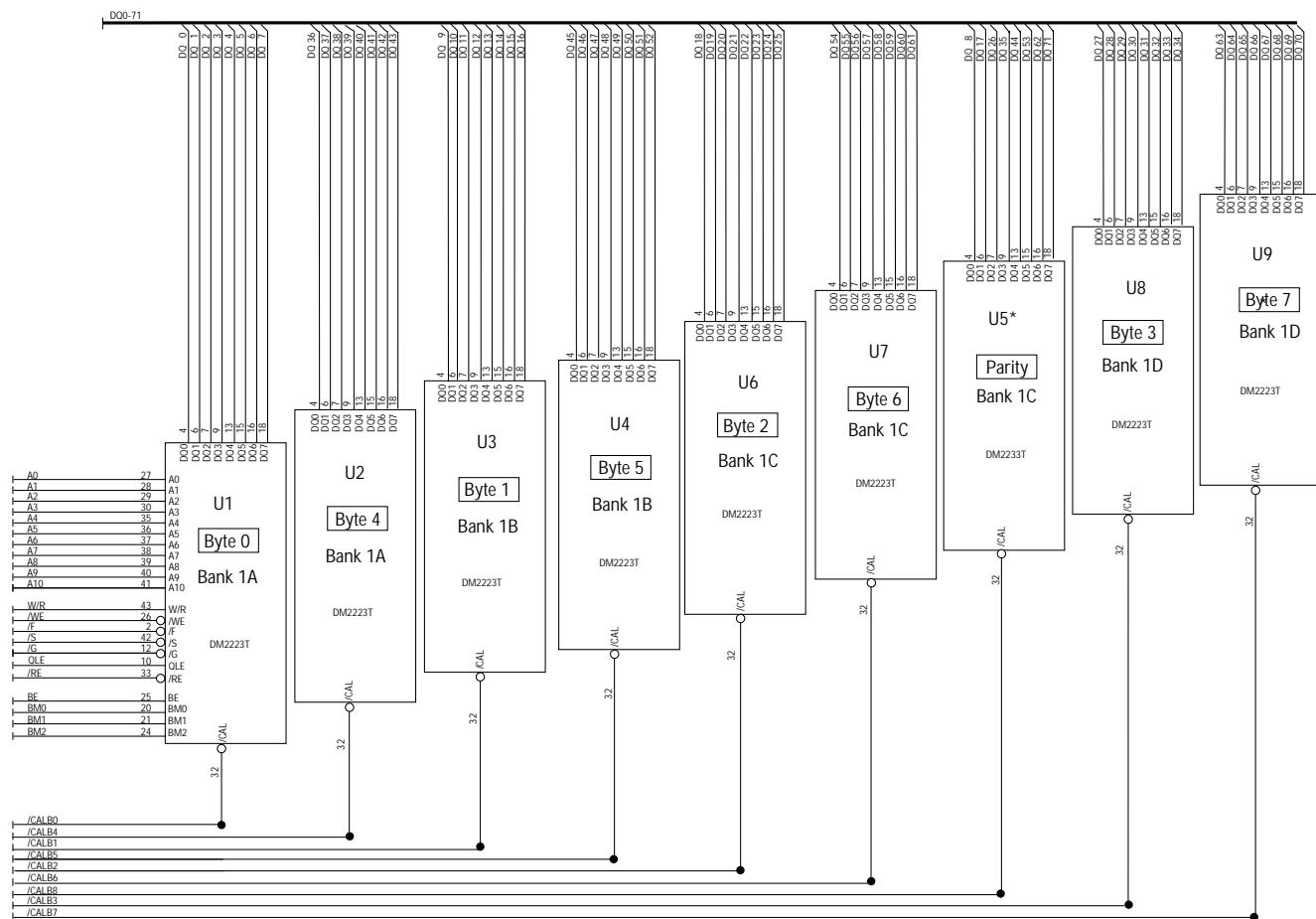
Note: For reference to buffer connection, append bank name to address or clock name, i.e., A10 + Bank 1A = A10BANK1A. Refer to Buffer Interconnect Diagram for detailed buffer connections. DQ0-71 and /CALB0-8 are directly connected to pins.

   * Not Present on DM1M64

Electrical Characteristics

$T_A = 0 - 70°C$ (Commercial)

Symbol	Parameters	Min	Max	Test Conditions
V_{CC}	Supply Voltage	4.75V	5.25V	All Voltages Referenced to V_{SS}
V_{IH}	Input High Voltage	2.4V	$V_{CC}+1$	
V_{IL}	Input Low Voltage	-1.0V	0.8V	
V_{OH}	Output High Level	2.4V	—	$I_{OUT} = -5mA$
V_{OL}	Output Low Level	—	0.4V	$I_{OUT} = 4.2mA$
$V_{i(L)}$	Input Leakage Current	-180µA	180µA	$0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V
$V_{0(L)}$	Output Leakage Current	-180µA	180µA	$0V \leq V_{IN}$, $0V \leq V_{OUT} \leq 5.5V$

DM1M72DTE

Symbol	Operating Current	33MHz Typ[1]	-12 Max	-15 Max	Test Condition	Notes
I_{CC1}	Random Read	1350mA	2913mA	2328mA	/RE, /CAL, /G and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC2}	Fast Page Mode Read	945mA	2184mA	1734mA	/CAL, /G and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC3}	Static Column Read	855mA	1869mA	1509mA	/G and Addresses Cycling: $t_{AC} = t_{AC}$ Minimum	2, 4
I_{CC4}	Random Write	1575mA	2589mA	2049mA	/RE, /CAL, /WE and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC5}	Fast Page Mode Write	810mA	2094mA	1644mA	/CAL, /WE and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC6}	Standby	21mA	21mA	21mA	All Control Inputs Stable $\geq V_{CC} - 0.2V$, Outputs Driven	
I_{CCT}	Average Typical Operating Current	630mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

(1) "33MHz Typ" refers to worst case I_{CC} expected in a system operating with a 33MHz memory bus. See power applications note for further details. This parameter is not 100% tested or guaranteed.
(2) I_{CC} is dependent on cycle rates and is measured with CMOS levels and the outputs open.
(3) I_{CC} is measured with a maximum of one address change while /RE = V_{IL}
(4) I_{CC} is measured with a maximum of one address change while /CAL = V_{IH}

DM1M64DTE

Symbol	Operating Current	33MHz Typ[1]	-12 Max	-15 Max	Test Condition	Notes
I_{CC1}	Random Read	1239mA	2687mA	2147mA	/RE, /CAL, /G and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC2}	Fast Page Mode Read	879mA	2039mA	1619mA	/CAL, /G and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC3}	Static Column Read	799mA	1759mA	1419mA	/G and Addresses Cycling: $t_{AC} = t_{AC}$ Minimum	2, 4
I_{CC4}	Random Write	1439mA	2399mA	1899mA	/RE, /CAL, /WE and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC5}	Fast Page Mode Write	759mA	1959mA	1539mA	/CAL, /WE and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC6}	Standby	19mA	19mA	19mA	All Control Inputs Stable $\geq V_{CC} - 0.2V$, Outputs Driven	
I_{CCT}	Average Typical Operating Current	424mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

(1) "33MHz Typ" refers to worst case I_{CC} expected in a system operating with a 33MHz memory bus. See power applications note for further details. This parameter is not 100% tested or guaranteed.
(2) I_{CC} is dependent on cycle rates and is measured with CMOS levels and the outputs open.
(3) I_{CC} is measured with a maximum of one address change while /RE = V_{IL}
(4) I_{CC} is measured with a maximum of one address change while /CAL = V_{IH}

Switching Characteristics V_{CC} = 5V ± 5%, T_A = 0 to 70°C, (Commercial) C_L = 50pf. Note: These parameters do not include address and control buffer delays. See page 3-75-8 for derating factor.

Symbol	Description	-12 Min	-12 Max	-15 Min	-15 Max	Units
t_{AC}[1]	Column Address Access Time		12		15	ns
t_{ACH}	Column Address Valid to /CAL Inactive (Write Cycle)	12		15		ns
t_{ACI}	Address Valid to /CAL Inactive (QLE High)	12		15		ns
t_{AHQ}	Column Address Hold From QLE High (/CAL=H)	0		0		ns
t_{AQH}	Address Valid to QLE High	12		15		ns
t_{AQX}	Column Address Change to Output Data Invalid	5		5		ns
t_{ASC}	Column Address Setup Time	5		5		ns
t_{ASR}	Row Address Setup Time	5		5		ns
t_{BCH}	BE Hold From /CAL Low	0		0		ns
t_{BHS}	BE High Setup to /CAL Low	5		5		ns
t_{BLS}	BE Low Setup to /CAL Low (Non-Burst Mode)	7		7		ns
t_{BP}	BE Low Time	5		5		ns
t_{BQV}	Data Out Valid From BE Low (/CAL High, QLE Low)		18		20	ns
t_{BQX}	Data Change From BE Low (/CAL High, QLE Low)	5		5		ns
t_{BSR}	BE Low to /RE Setup Time	7		7		ns
t_C	Row Enable Cycle Time	55		65		ns
t_{C1}	Row Enable Cycle Time, Cache Hit (Row=LRR), Read Cycle Only	20		25		ns
t_{CAE}	Column Address Latch Active Time	5		6		ns
t_{CAH}	Column Address Hold Time	0		0		ns
t_{CAH1}	Column Address Hold Time - Burst Mode Entry	2		2		ns
t_{CH}	Column Address Latch High Time (Latch Transparent)	5		5		ns
t_{CHR}	/CAL Inactive Lead Time to /RE Inactive (Write Cycles Only)	-2		-2		ns
t_{CHW}	Column Address Latch High to Write Enable Low (Multiple Writes)	0		0		ns
t_{CLV}	Column Address Latch Low to Data Valid (QLE High)		7		7	ns
t_{CQH}	Data Hold From /CAL ↓ Transaction (QLE High)	0		0		ns
t_{CQV}	Column Address Latch High to Data Valid		15		15	ns
t_{CQX}	Column Address Latch Inactive to Data Invalid	5		5		ns
t_{CRP}	Column Address Latch Setup Time to Row Enable	5		5		ns
t_{CWL}	/WE Low to /CAL Inactive	5		5		ns
t_{DH}	Data Input Hold Time	0		0		ns
t_{DMH}	Mask Hold Time From Row Enable (Write-Per-Bit)	1		1.5		ns
t_{DMS}	Mask Setup Time to Row Enable (Write-Per-Bit)	5		5		ns
t_{DS}	Data Input Setup Time	5		5		ns
t_{GQV}[1]	Output Enable Access Time		5		5	ns
t_{GQX}[2,3]	Output Enable to Output Drive Time	0	5	0	5	ns
t_{GQZ}[4,5]	Output Turn-Off Delay From Output Disabled (/G↑)	0	5	0	5	ns
t_{MCH}	BM_{0-2} Mode Hold Time From /CAL Low	0		0		ns

Switching Characteristics (continued) V_{CC} = 5V ± 5%, T_A = 0 to 70°C, (Commercial) C_L = 50pf. Note: These parameters do not include address and control buffer delays. See page 3-75-8 for derating factor.

Symbol	Description	-12 Min	-12 Max	-15 Min	-15 Max	Units
t_{MCL}	BM_{0-2} Mode to /CAL ↓ Transition	5		5		ns
t_{MH}	/F and W/R Mode Select Hold Time	0		0		ns
t_{MSU}	/F and W/R Mode Select Setup Time	5		5		ns
t_{NRH}	/CAL, /G, and /WE Hold Time For /RE-Only Refresh	0		0		ns
t_{NRS}	/CAL, /G, and /WE Setup Time For /RE-Only Refresh	5		5		ns
t_{PC}	Column Address Latch Cycle Time	12		15		ns
t_{QCI}	QLE High to /CAL Inactive	0		0		ns
t_{QH}	QLE High Time	5		5		ns
t_{QL}	QLE Low Time	5		5		ns
t_{QQH}	Data Hold From QLE Inactive	2		2		ns
t_{QQV}	Data Valid From QLE Low		7.5		7.5	ns
t_{RAC}[1]	Row Enable Access Time, On a Cache Miss		30		35	ns
t_{RAC1}[1]	Row Enable Access Time, On a Cache Hit (Limit Becomes t_{AC})		15		17	ns
t_{RAH}	Row Address Hold Time	1		1.5		ns
t_{RBH}	BE Hold Time From /RE	0		0		ns
t_{RE}	Row Enable Active Time	30	100000	35	100000	ns
t_{RE1}	Row Enable Active Time, Cache Hit (Row=LRR) Read Cycle	8		10		ns
t_{REF}	Refresh Period		64		64	ms
t_{RP}	Row Precharge Time	20		25		ns
t_{RP1}	Row Precharge Time, Cache Hit (Row=LRR) Read Cycle	8		10		ns
t_{RRH}	/WE Don't Care From Row Enable High (Write Only)	0		0		ns
t_{RSH}	Last Write Address Latch to End of Write	12		15		ns
t_{RSW}	Row Enable to Column Address Latch Low For Second Write	35		40		ns
t_{RWL}	Last Write Enable to End of Write	12		15		ns
t_{SC}	Column Address Cycle Time	12		15		ns
t_{SDC}	/S Enable to First /CAL Low	12		15		ns
t_{SH}	/S High to Exit Burst	7		7		ns
t_{SHR}	Select Hold From Row Enable	0		0		ns
t_{SQV}[1]	Chip Select Access Time		12		15	ns
t_{SQX}[2,3]	Output Turn-On From Select Low	0	12	0	15	ns
t_{SQZ}[4,5]	Output Turn-Off From Chip Select	0	8	0	10	ns
t_{SSR}	Select Setup Time to Row Enable	5		5		ns
t_T	Transition Time (Rise and Fall)	1	10	1	10	ns
t_{WC}	Write Enable Cycle Time	12		15		ns
t_{WCH}	Column Address Latch Low to Write Enable Inactive Time	5		5		ns

Switching Characteristics (continued) $V_{CC} = 5V \pm 5\%$, $T_A = 0$ to 70°C, (Commercial) $C_L = 50$pf. Note: These parameters do not include address and control buffer delays. See page 3-75-8 for derating factor.

Symbol	Description	-12		-15		Units
		Min	Max	Min	Max	
t_{WHR}[6]	Write Enable Hold After /RE	0		0		ns
t_{WI}	Write Enable Inactive Time	5		5		ns
t_{WP}	Write Enable Active Time	5		5		ns
t_{WQV}[1]	Data Valid From Write Enable High		12		15	ns
t_{WQX}[2,5]	Data Output Turn-On From Write Enable High	0	12	0	15	ns
t_{WQZ}[3,4]	Data Turn-Off From Write Enable Low	0	12	0	15	ns
t_{WRP}	Write Enable Setup Time to Row Enable	5		5		ns

(1) V_{OUT} Timing Reference Point at 1.5V

(2) Parameter Defines Time When Output is Enabled (Sourcing or Sinking Current) and is Not Referenced to V_{OH} or V_{OL}

(3) Minimum Specification is Referenced from V_{IH} and Maximum Specification is Referenced from V_{IL} on Input Control Signal

(4) Parameter Defines Time When Output Achieves Open-Circuit Condition and is Not Referenced to V_{OH} or V_{OL}

(5) Minimum Specification is Referenced from V_{IL} and Maximum Specification is Referenced from V_{IH} on Input Control Signal

(6) For Write-Per-Bit Devices, t_{WHR} is Limited By Data Input Setup Time, t_{DS}

/RE Inactive Cache Read Hit (Static Column Mode)
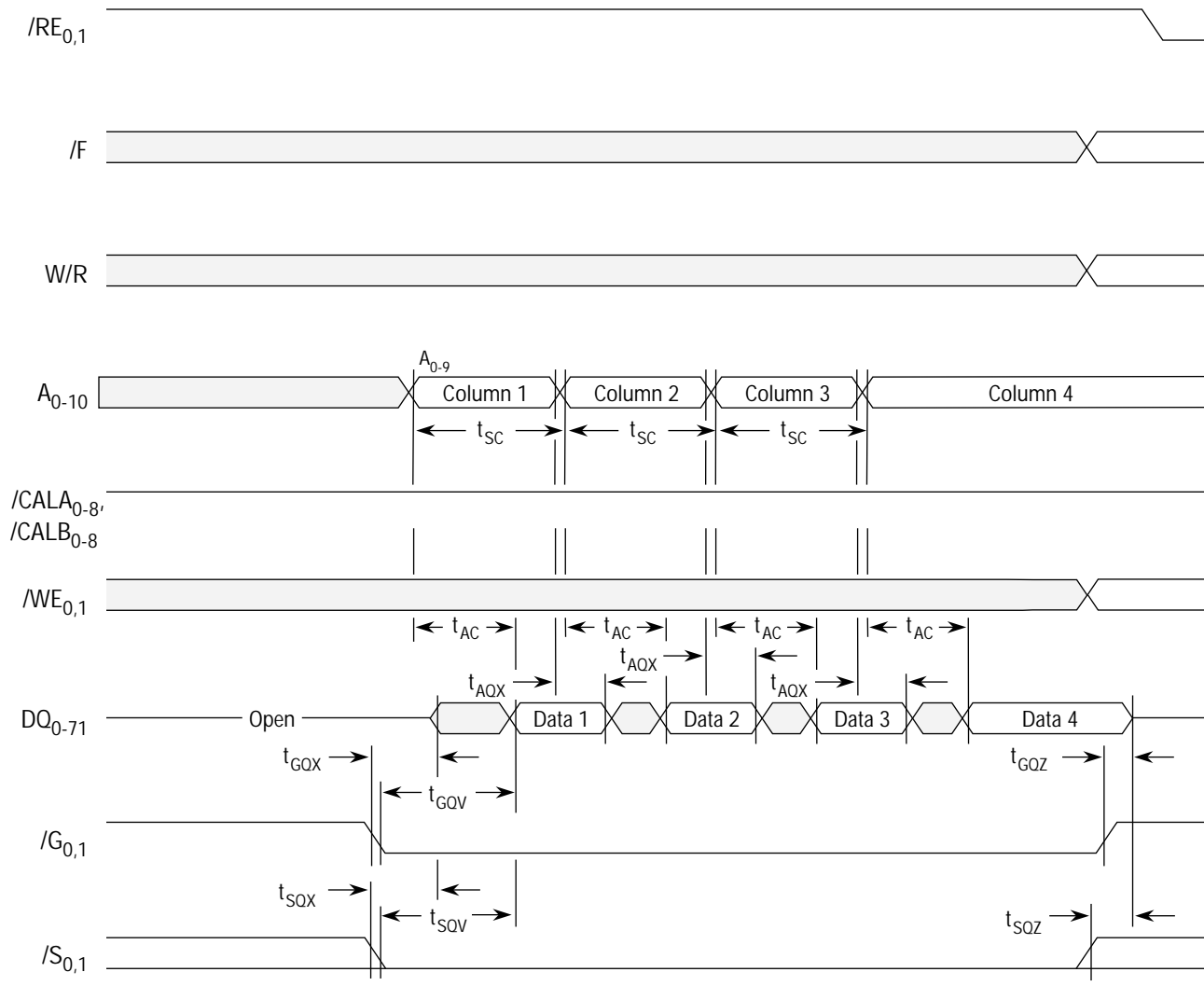
Don't Care or Indeterminate ▢

NOTES: 1. Column address A_{8-9} specify cache bank accessed on each read.

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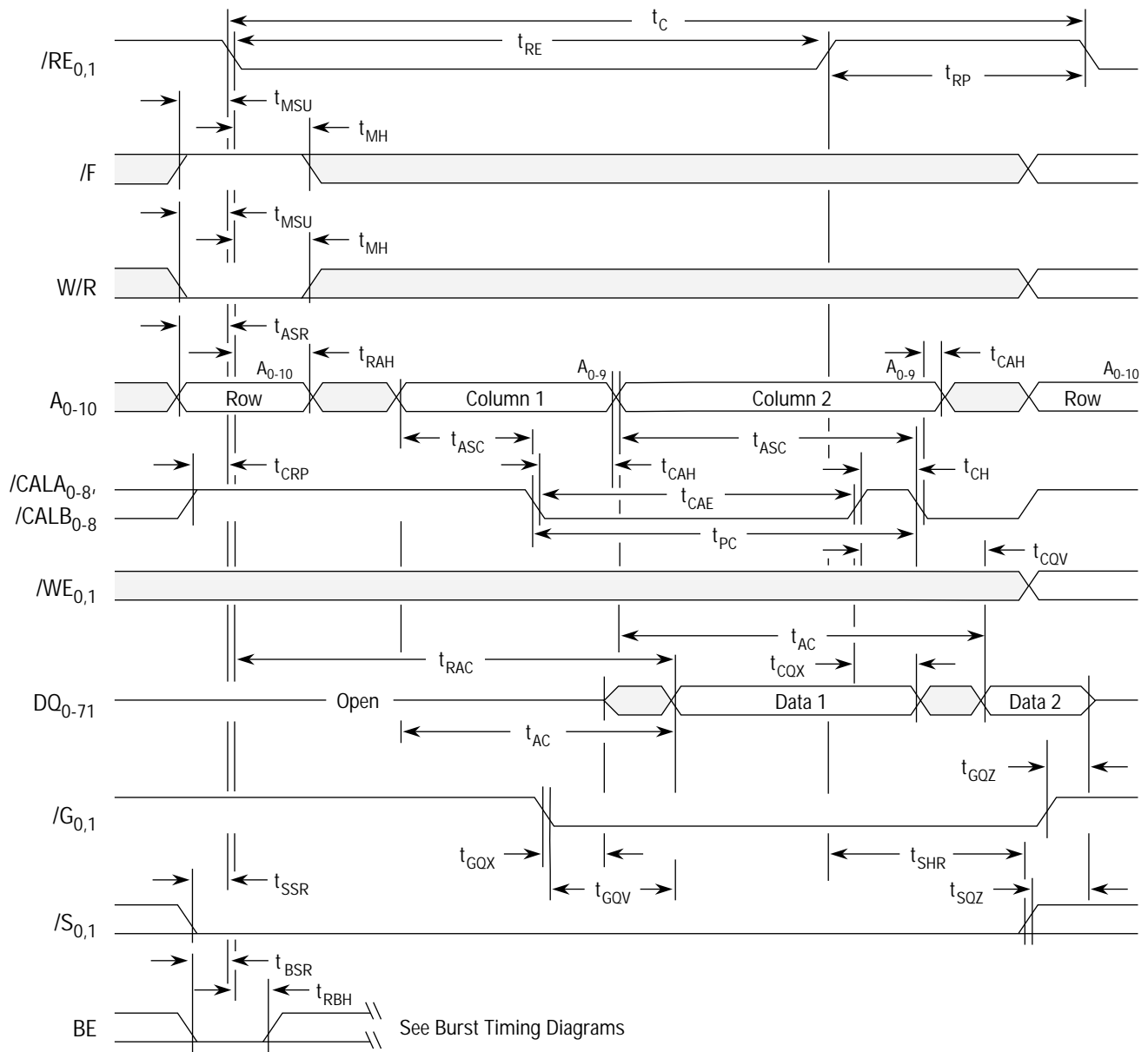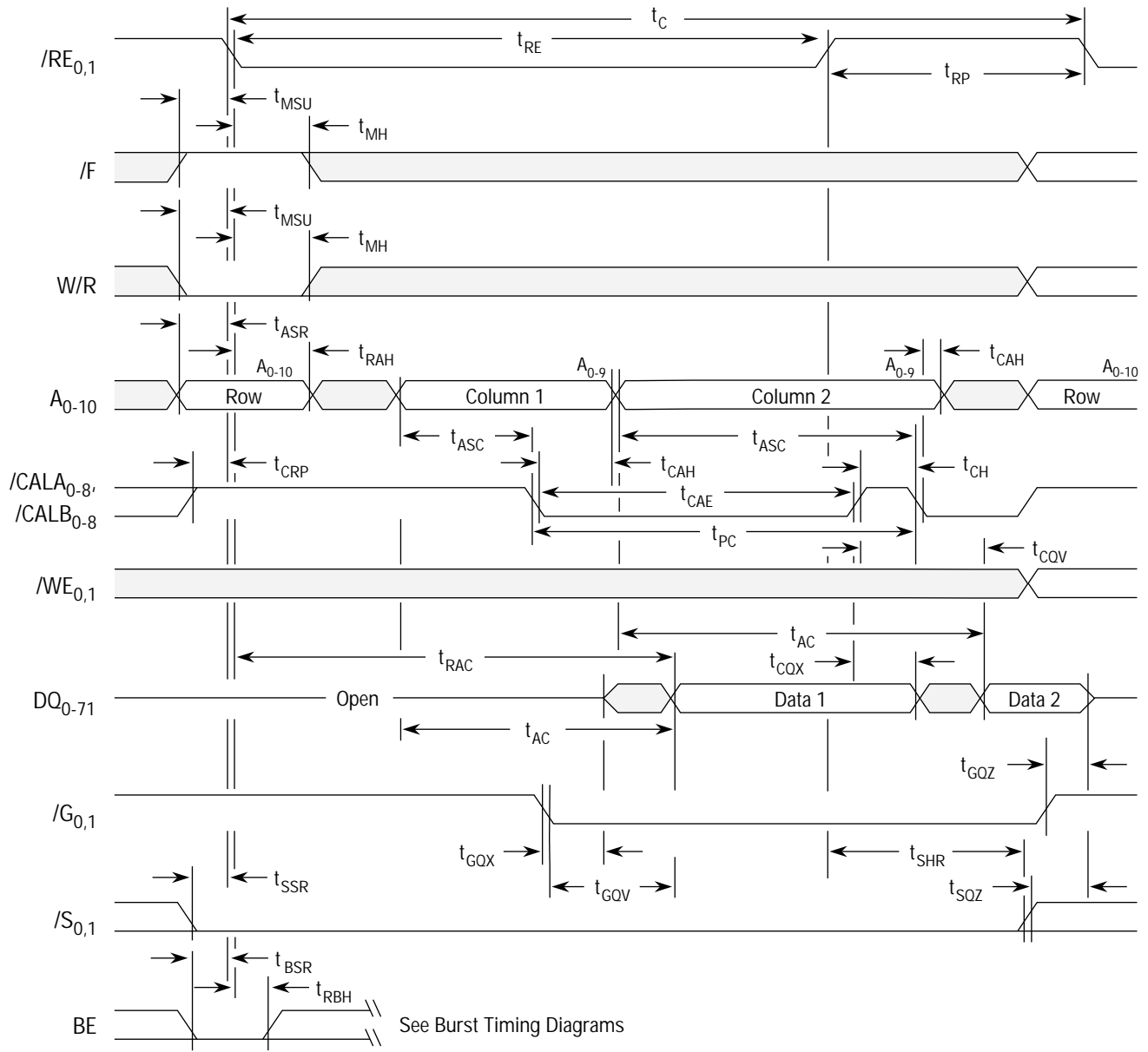## /RE Inactive Cache Read Hit (Page Mode)
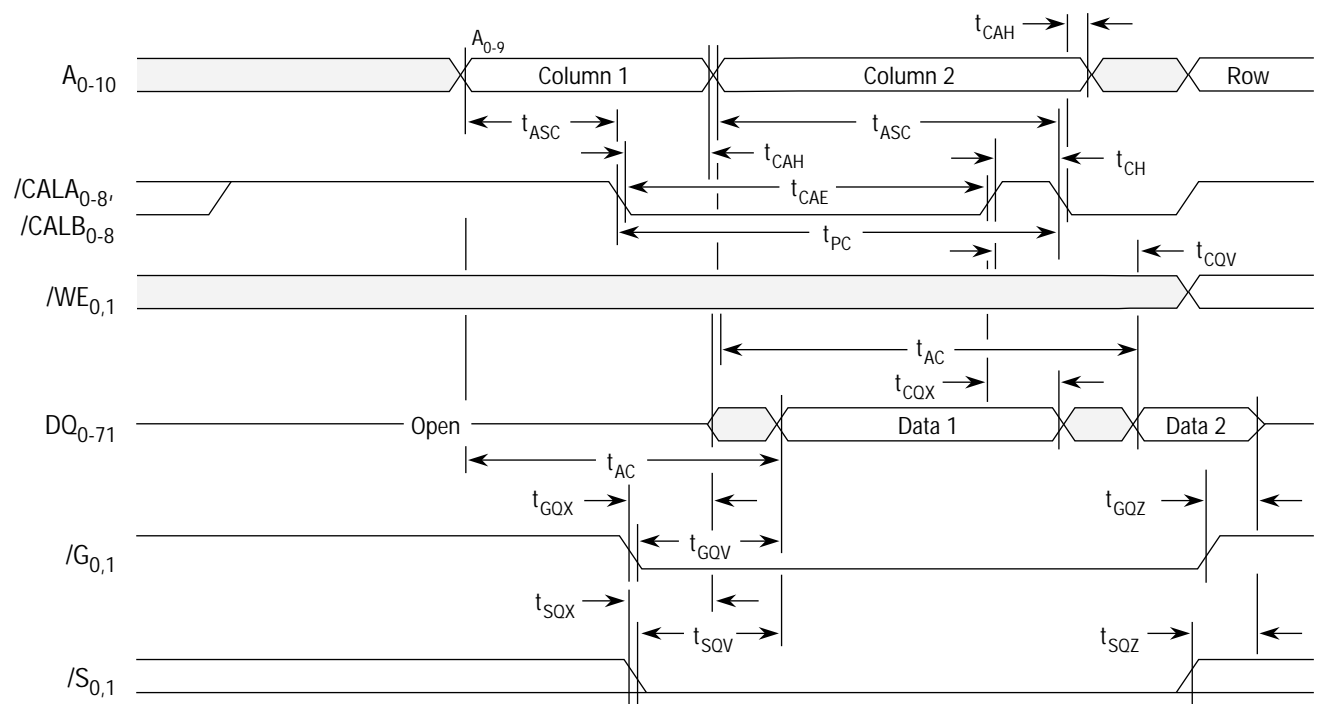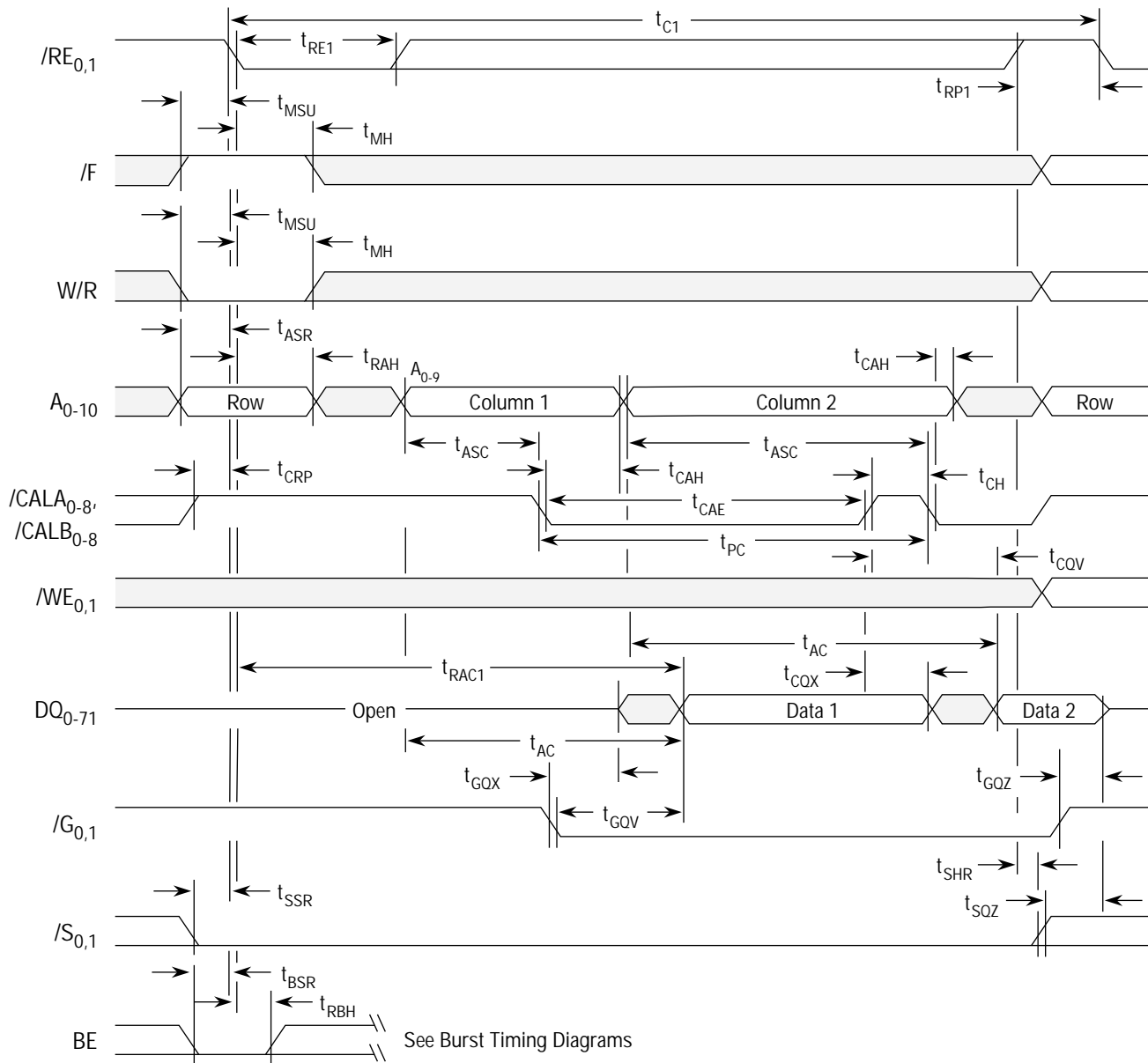
Don't Care or Indeterminate ☐

NOTES: 1. Column address A_{8-9} specify cache bank accessed on each read.

## /RE Inactive Cache Read Hit (EDO Mode)

Don't Care or Indeterminate ☐

NOTES: 1. Column addresses A_{8-9} specify cache bank accessed on each read.

/RE Active Cache Read Hit (Static Column Mode)

NOTES: 1. Column address A_{8-9} specify cache bank accessed on each read.

Don't Care or Indeterminate ☐

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t_{C1}

/RE$_{0,1}$

t_{RE1}

t_{RP1}

t_{MSU}

t_{MH}

/F

t_{MSU}

t_{MH}

W/R

t_{ASR}

t_{RAH} A$_{0-9}$

t_{CAH}

A$_{0-10}$ Row   Column 1   Column 2   Row

t_{ASC} t_{ASC}

t_{CRP} t_{CAH} t_{CH}

/CALA$_{0-8}$, t_{CAE}

/CALB$_{0-8}$ t_{PC}

t_{CQV}

/WE$_{0,1}$

t_{AC}

t_{RAC1} t_{CQX}

DQ$_{0-71}$ Open   Data 1   Data 2

t_{AC}

t_{GQX} t_{GQZ}

/G$_{0,1}$ t_{GQV}

t_{SHR}

t_{SSR} t_{SQZ}

/S$_{0,1}$

t_{BSR}

t_{RBH}

BE   See Burst Timing Diagrams

Don't Care or Indeterminate ▢

NOTES: 1. Column address A$_{8-9}$ specify cache bank accessed on each read.
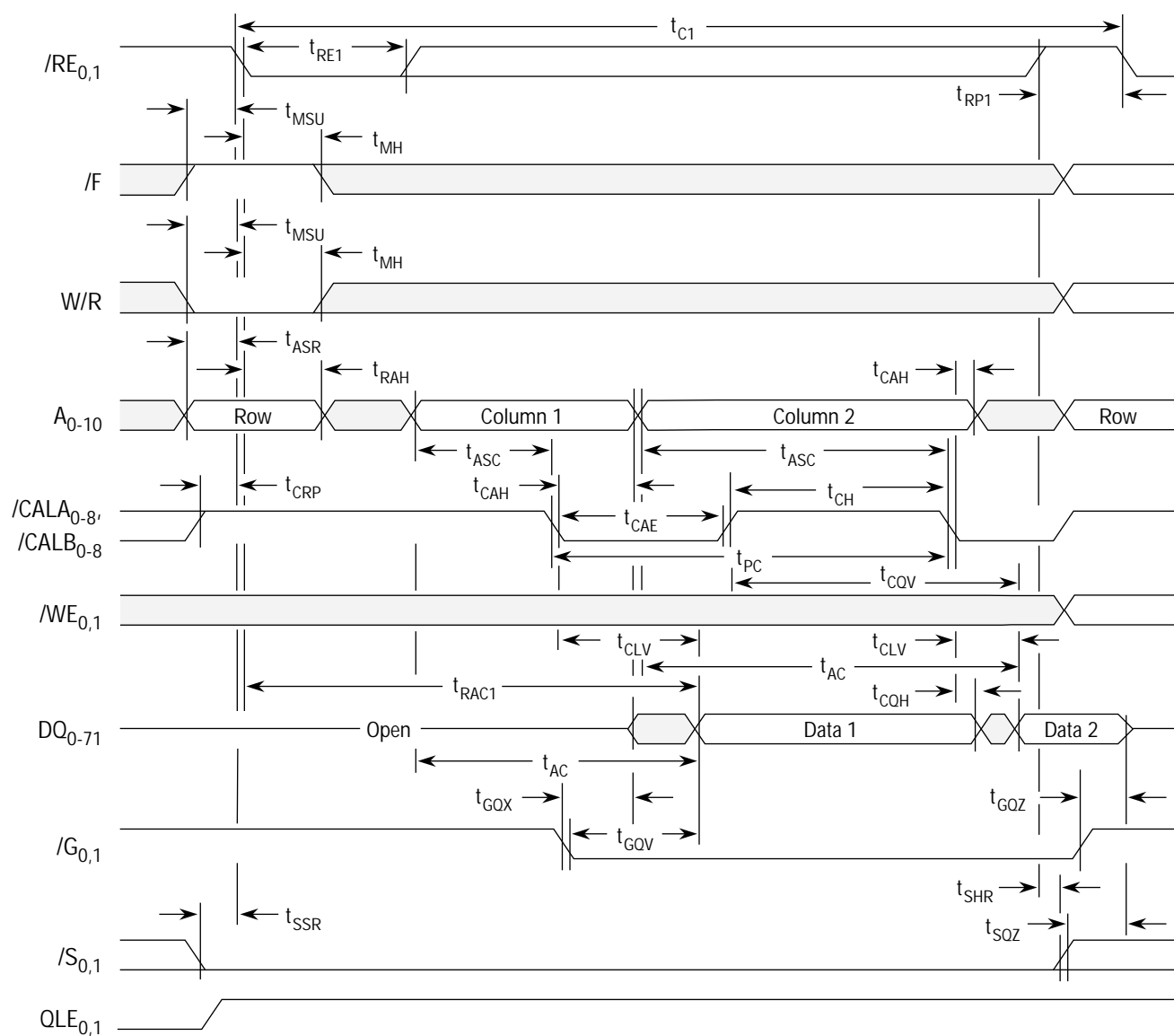
/RE Active Cache Read Hit (EDO Mode)

NOTES: 1. Latched data becomes invalid when /S is inactive.
2. Column addresses A_{8-9} specify cache bank accessed on each read.

Don't Care or Indeterminate ☐

/RE Active Cache Read Miss (Static Column Mode)

t_C

$/RE_{0,1}$ t_{RE} t_{RP}

t_{MSU} t_{MH}

/F

t_{MSU} t_{MH}

W/R

t_{ASR} t_{RAH} t_{CAH}

A_{0-10} A_{0-10} A_{0-9} A_{0-9} A_{0-10}

Row | Column 1 | Column 2 | Row

t_{ASC} t_{ASC} t_{CAH} t_{CH}

$/CALA_{0-8}$, t_{CRP} t_{CAE}
$/CALB_{0-8}$ t_{PC}

t_{CQV}

$/WE_{0,1}$ t_{AC} t_{CQX}

t_{RAC}

DQ_{0-71} Open | Data 1 | Data 2

t_{AC}

t_{GQZ}

$/G_{0,1}$

t_{GQX} t_{SHR}

t_{SSR} t_{GQV} t_{SQZ}

$/S_{0,1}$

t_{BSR} t_{RBH}

BE See Burst Timing Diagrams

Don't Care or Indeterminate ☐

NOTES: 1. Column address A_{8-9} specify cache bank accessed on each read.

/RE Active Cache Read Miss (Page Mode)

/RE$_{0,1}$

t_C

t_{RE}

t_{RP}

/F

t_{MSU}

t_{MH}

W/R

t_{MSU}

t_{MH}

A$_{0-10}$

t_{ASR}

t_{RAH}

A$_{0-10}$ Row

A$_{0-9}$ Column 1

A$_{0-9}$ Column 2

t_{CAH}

A$_{0-10}$ Row

/CALA$_{0-8}$,
/CALB$_{0-8}$

t_{CRP}

t_{ASC}

t_{CAH}

t_{ASC}

t_{CH}

t_{CAE}

t_{PC}

t_{CQV}

/WE$_{0,1}$

t_{AC}

t_{CQX}

t_{RAC}

DQ$_{0-71}$

Open

Data 1

Data 2

t_{AC}

t_{GQZ}

/G$_{0,1}$

t_{GQX}

t_{SHR}

t_{SSR}

t_{GQV}

t_{SQZ}

/S$_{0,1}$

t_{BSR}

t_{RBH}

BE

See Burst Timing Diagrams

Don't Care or Indeterminate ☐

NOTES: 1. Column address A$_{8-9}$ specify cache bank accessed on each read.

/RE Active Cache Read Miss (EDO Mode)
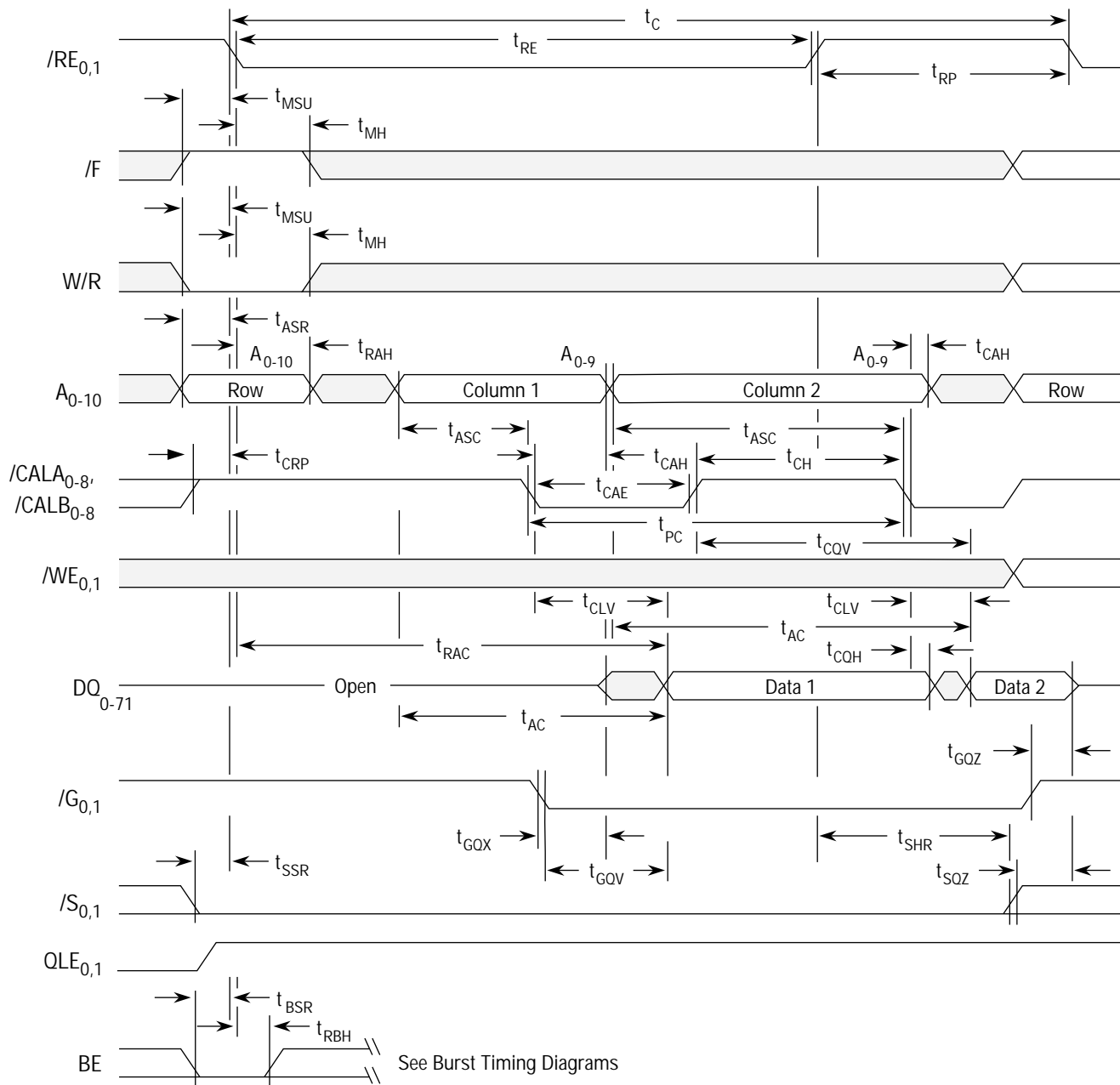
NOTES:
1. Latched data becomes invalid when /S is inactive.
2. This is the only valid /RE active read miss timing if EDO option is selected.
3. Column addresses A_{8-9} specify cache bank accessed during read.

Don't Care or Indeterminate ☐

Output Latch Enable Operation (Static Column EDO Mode Read)
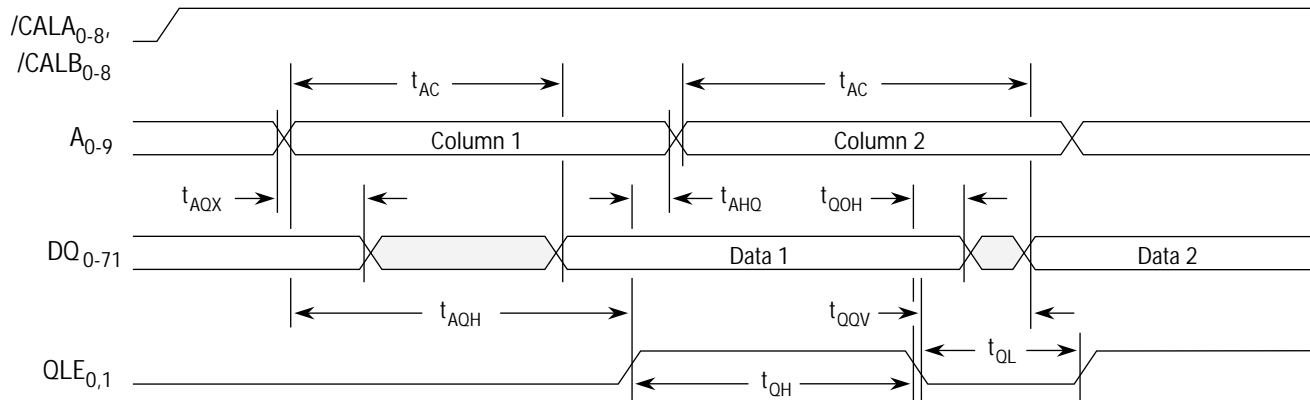
Output Latch Enable Operation (Page Mode EDO Read)
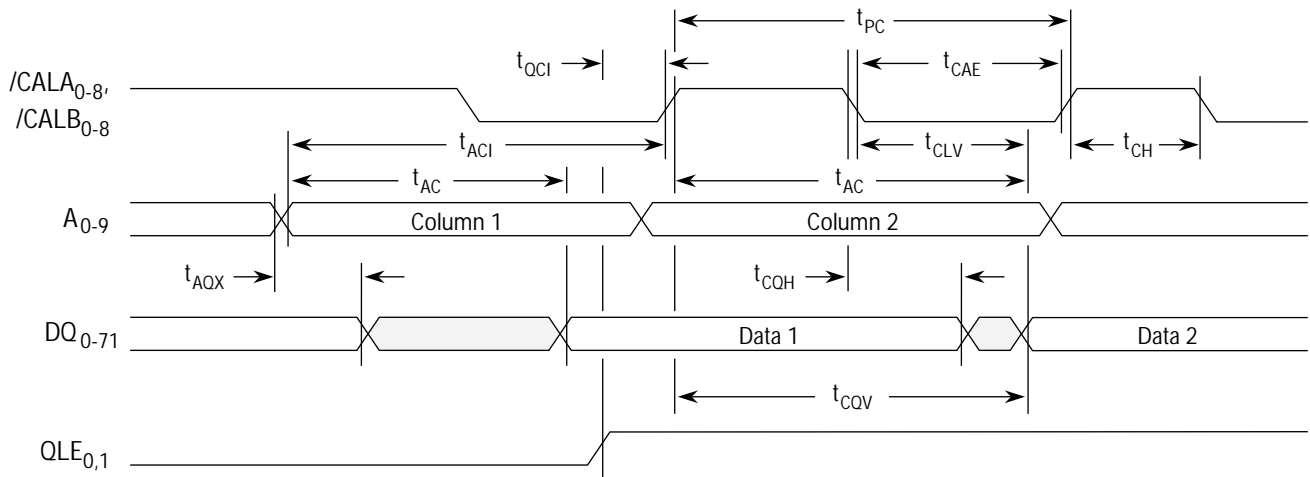
Output Latch Enable Operation (Asynchronous Access)
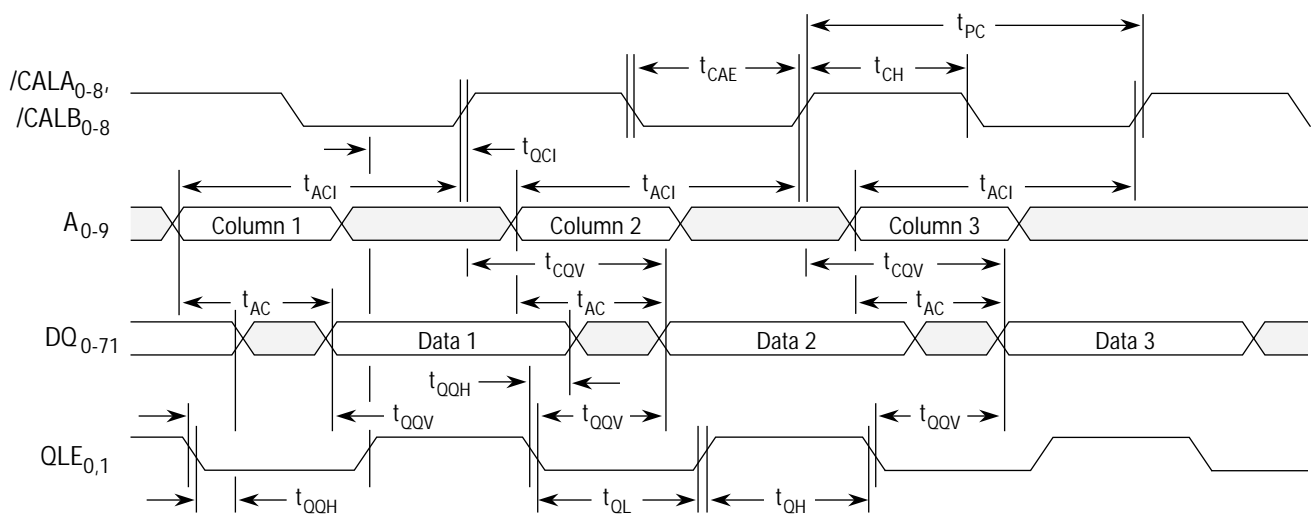
Burst-To-Burst Reads Or Writes
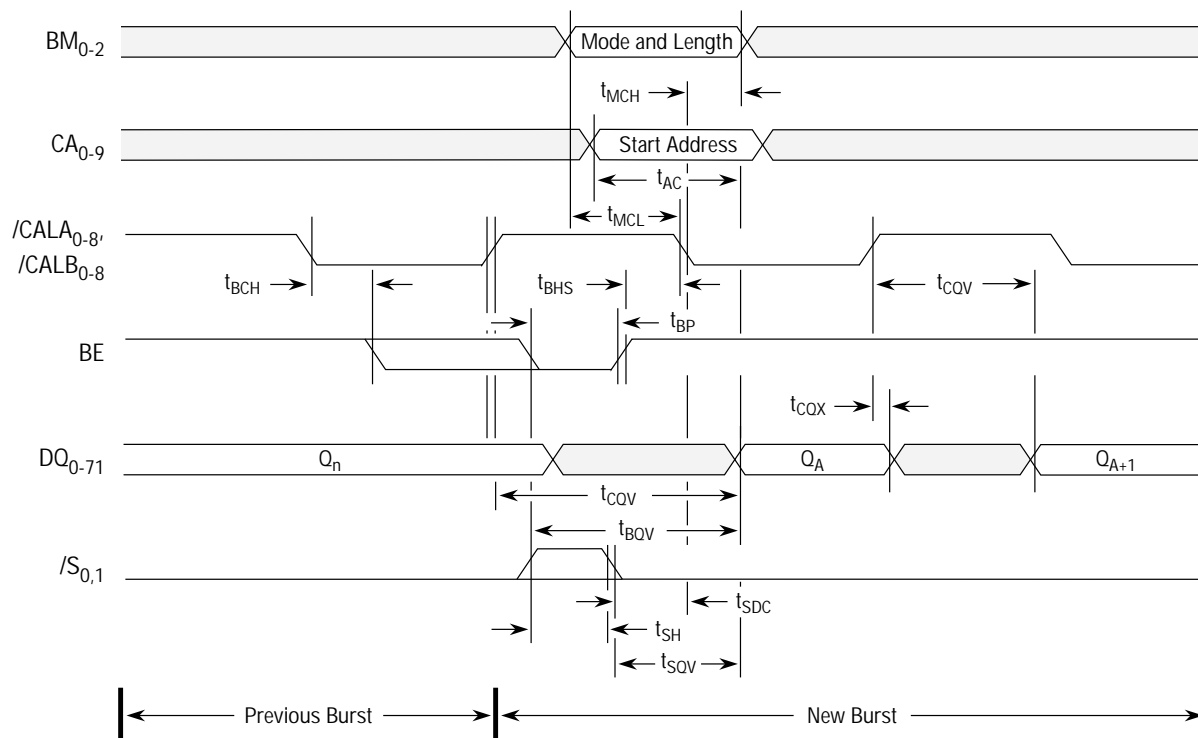
Burst-To-Random Reads Or Writes
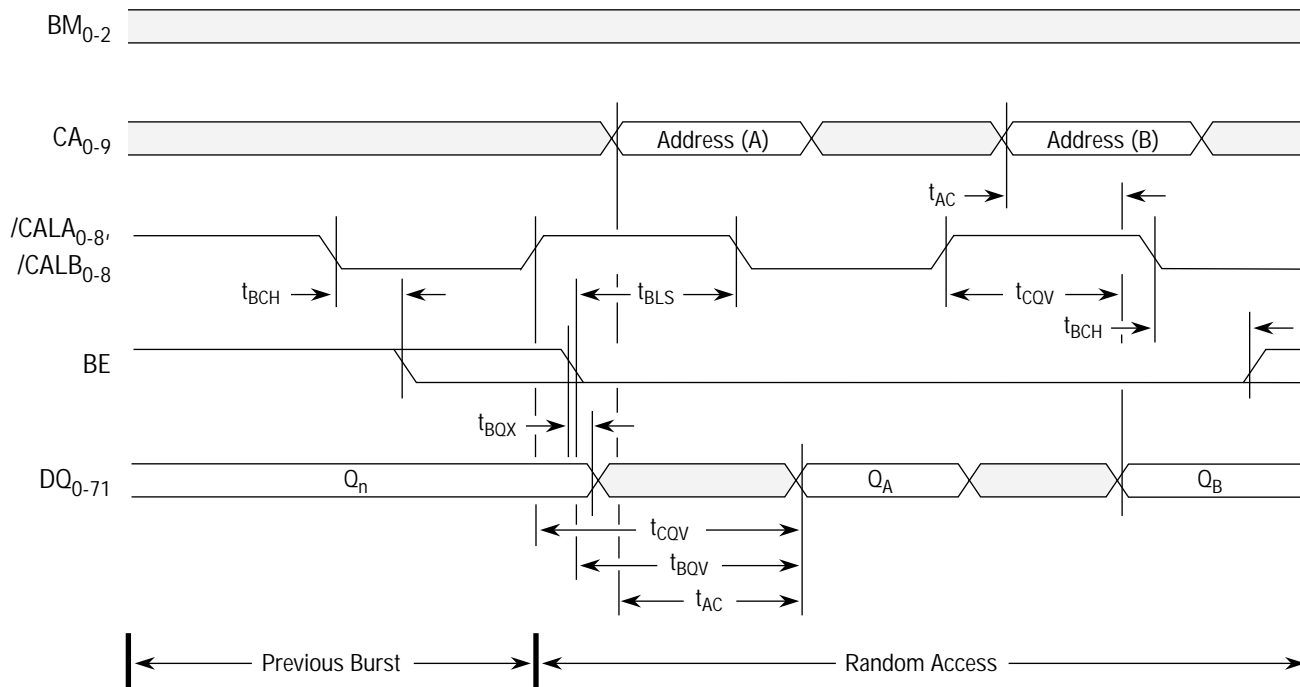
NOTES:
1. All relevant timing relationships between CA_{0-9}, /CAL, /WE, and DQ_{0-71} as shown in other timing diagrams applies to burst mode.
2. Bringing either BE low when /CAL is high or bringing /S high will exit burst mode.
3. /S may only go high when /RE is inactive or during an internal (/F) refresh.

/RE Inactive Burst Read Hit (EDO Mode)
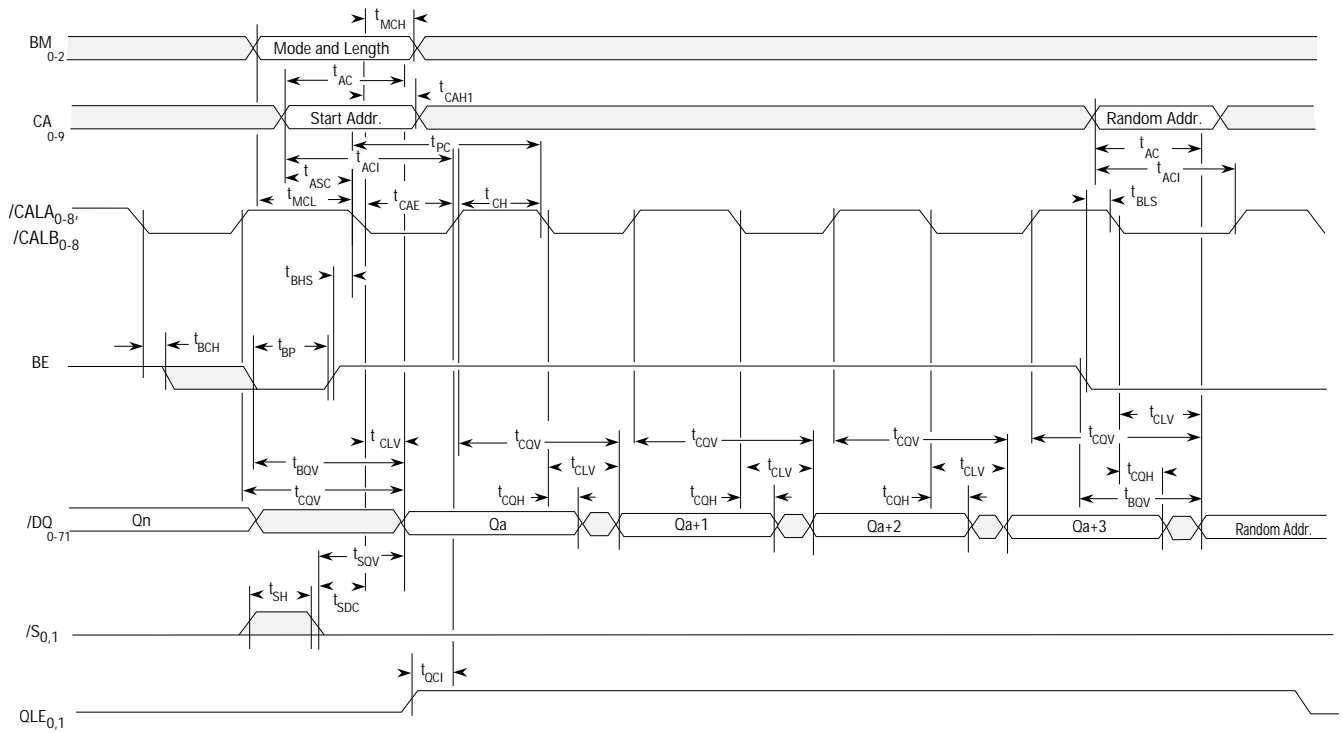
Note: 1. Column addresses A_{8-9} specify cache bank accessed on cache read.

/RE Active Burst Read Miss (EDO Mode)
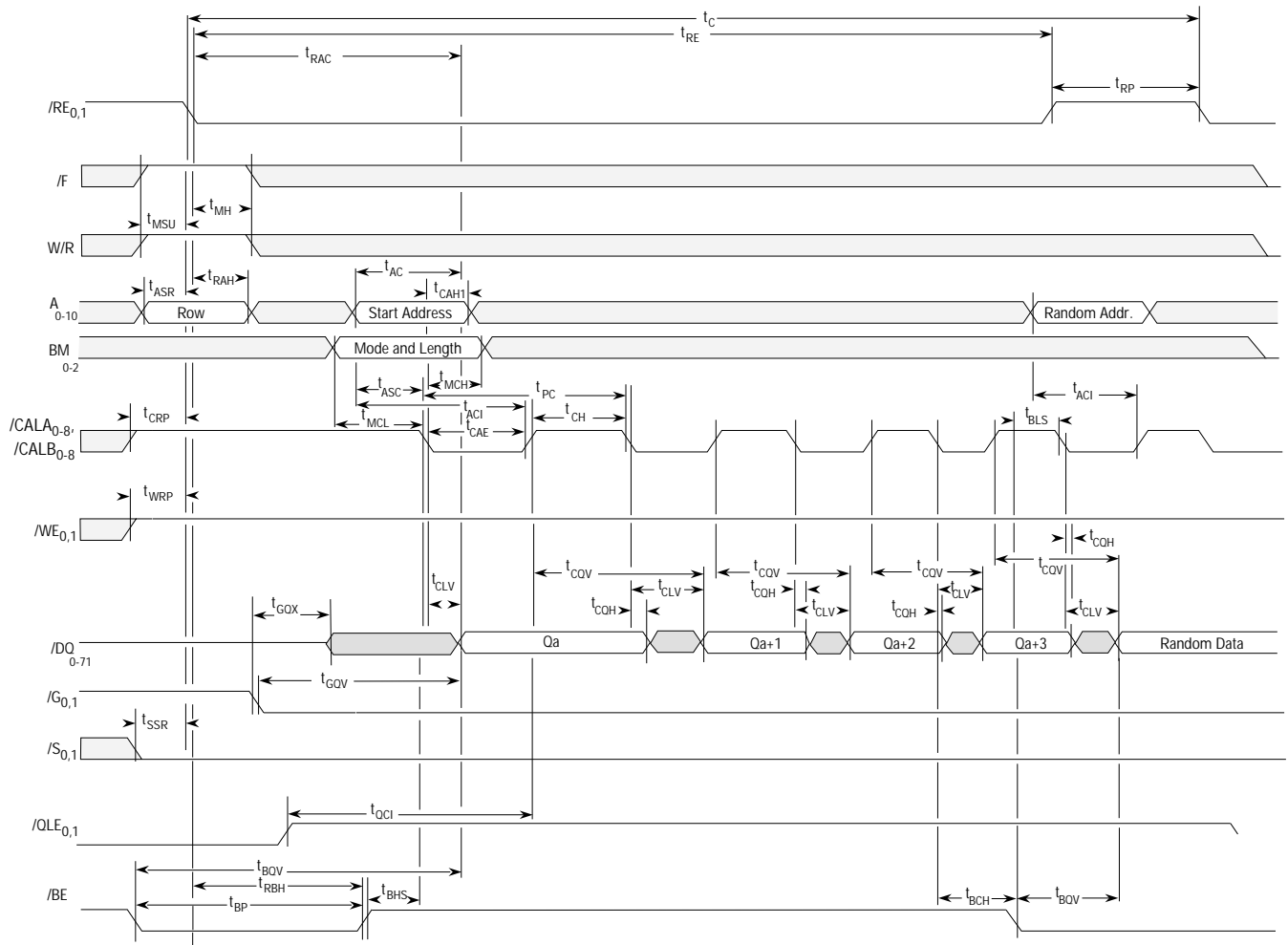
Note: 1. Column addresses A_{8-9} specify cache bank accessed on cache read.

/RE Active Burst Write Followed by Random Read in EDO Mode
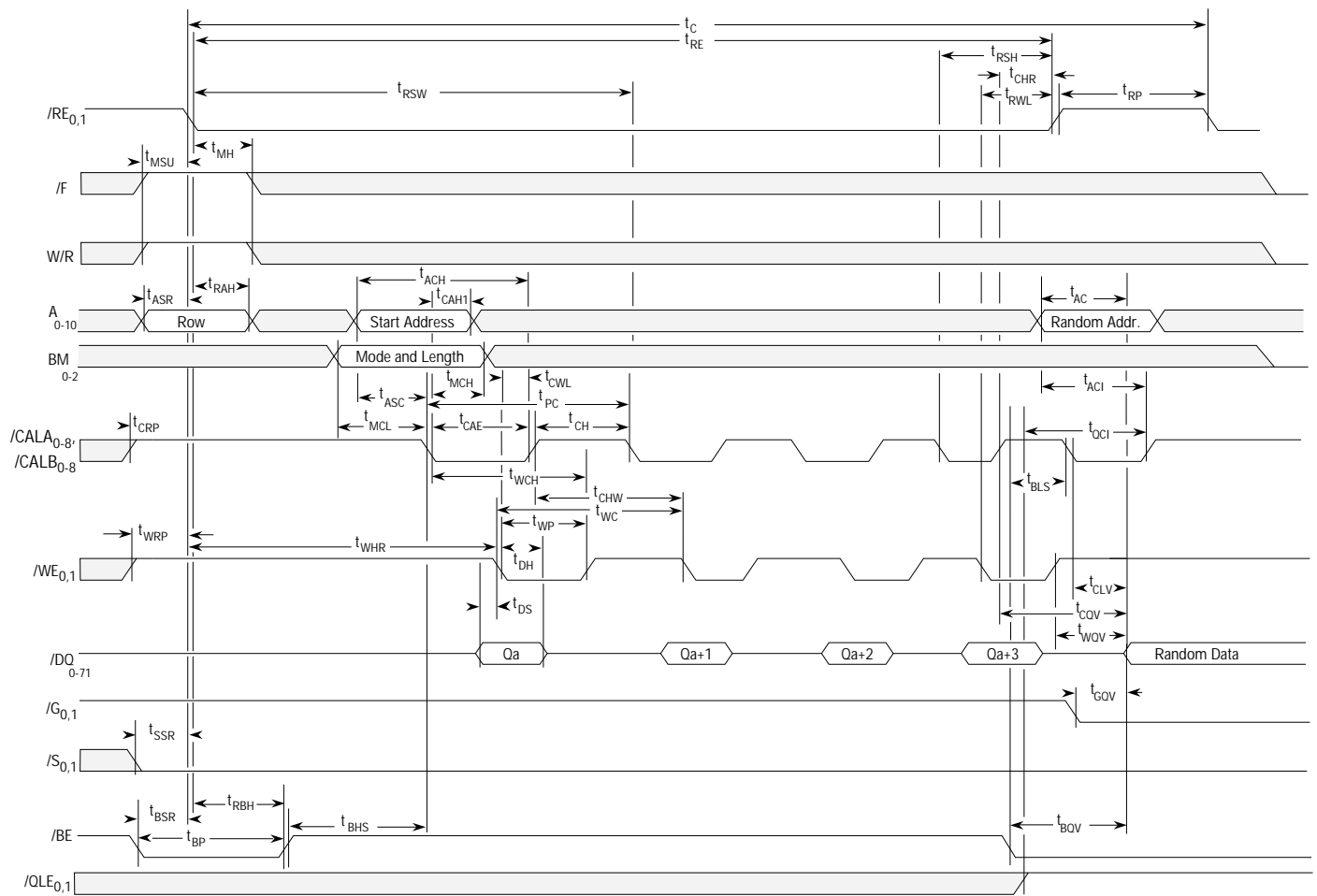
Note: 1. Column addresses A_{8-9} must be the same as row addresses A_{8-9} for writes.

Burst Write (Hit or Miss) Followed By /RE Inactive Cache Reads
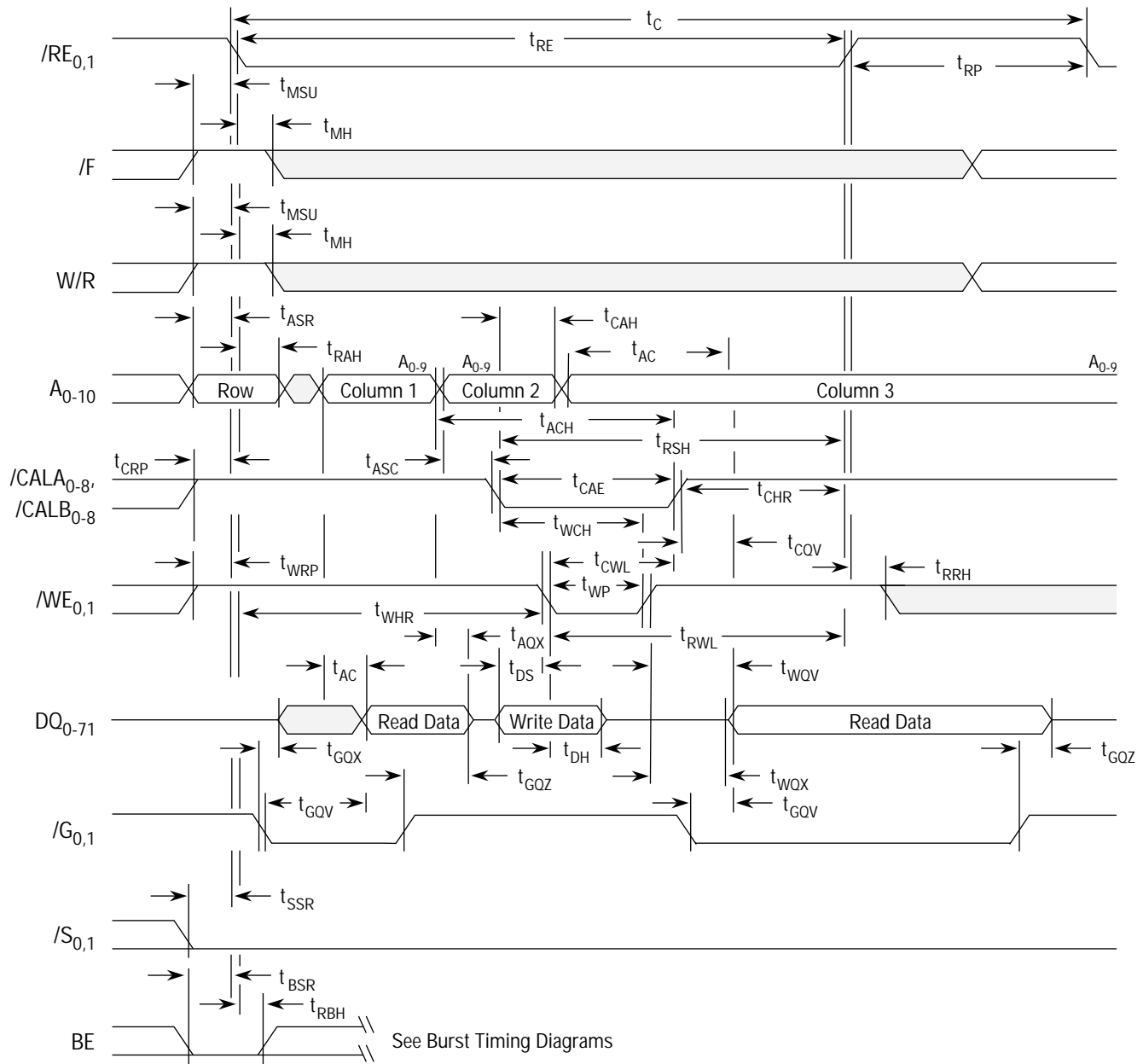
Don't Care or Indeterminate ▨

NOTES: 1. If column address one equals column address two, then a read-modify-write cycle is performed.
2. Reads and writes can occur to different banks.

Read/Write During Write Hit Cycle (Can Include Read-Modify-Write)
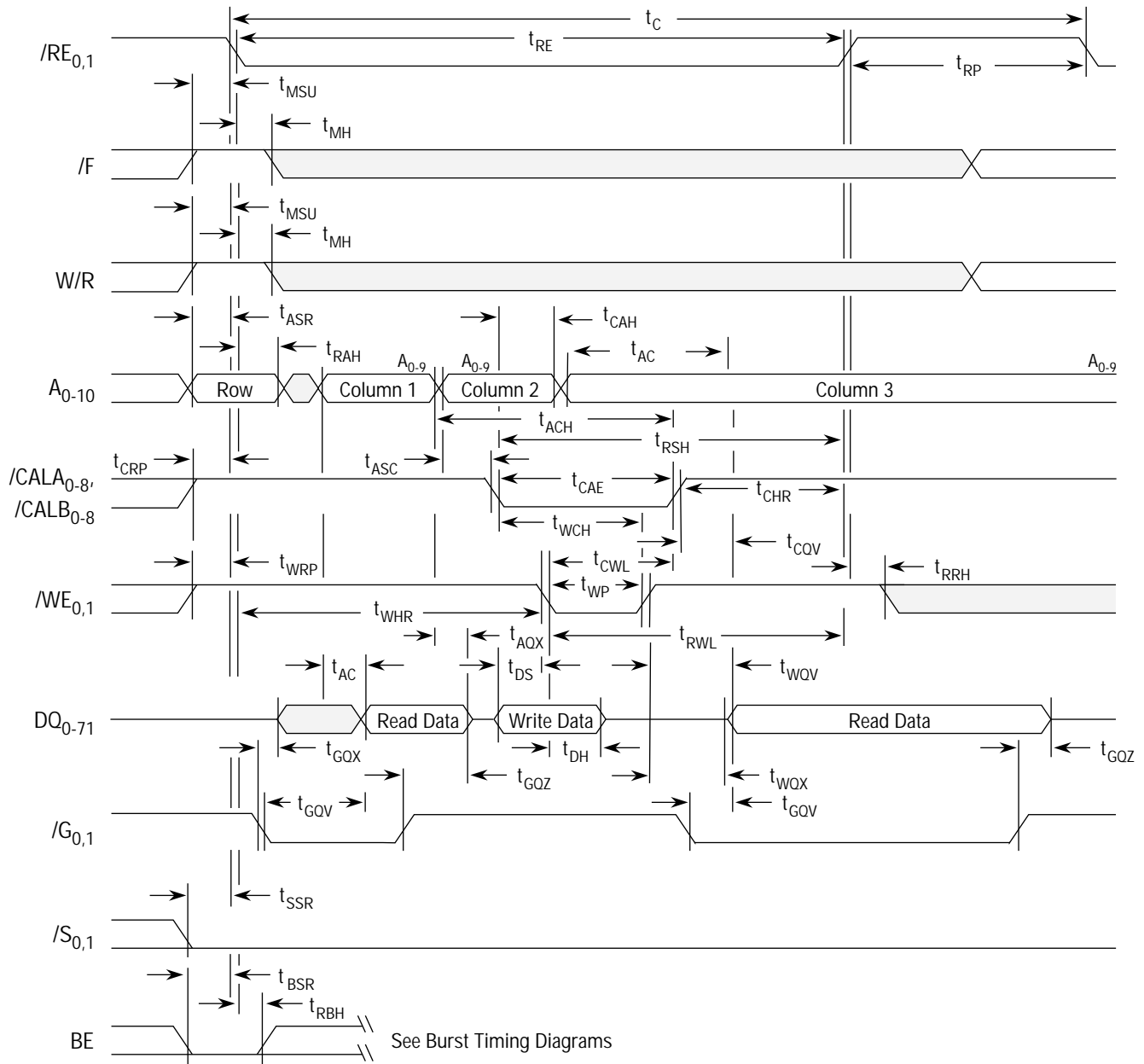
Don't Care or Indeterminate ▢

NOTES: 1. If column address one equals column address two, then a read-modify-write cycle is performed.
2. Reads and writes can occur to different banks.

Write-Per-Bit Cycle (/G=High)
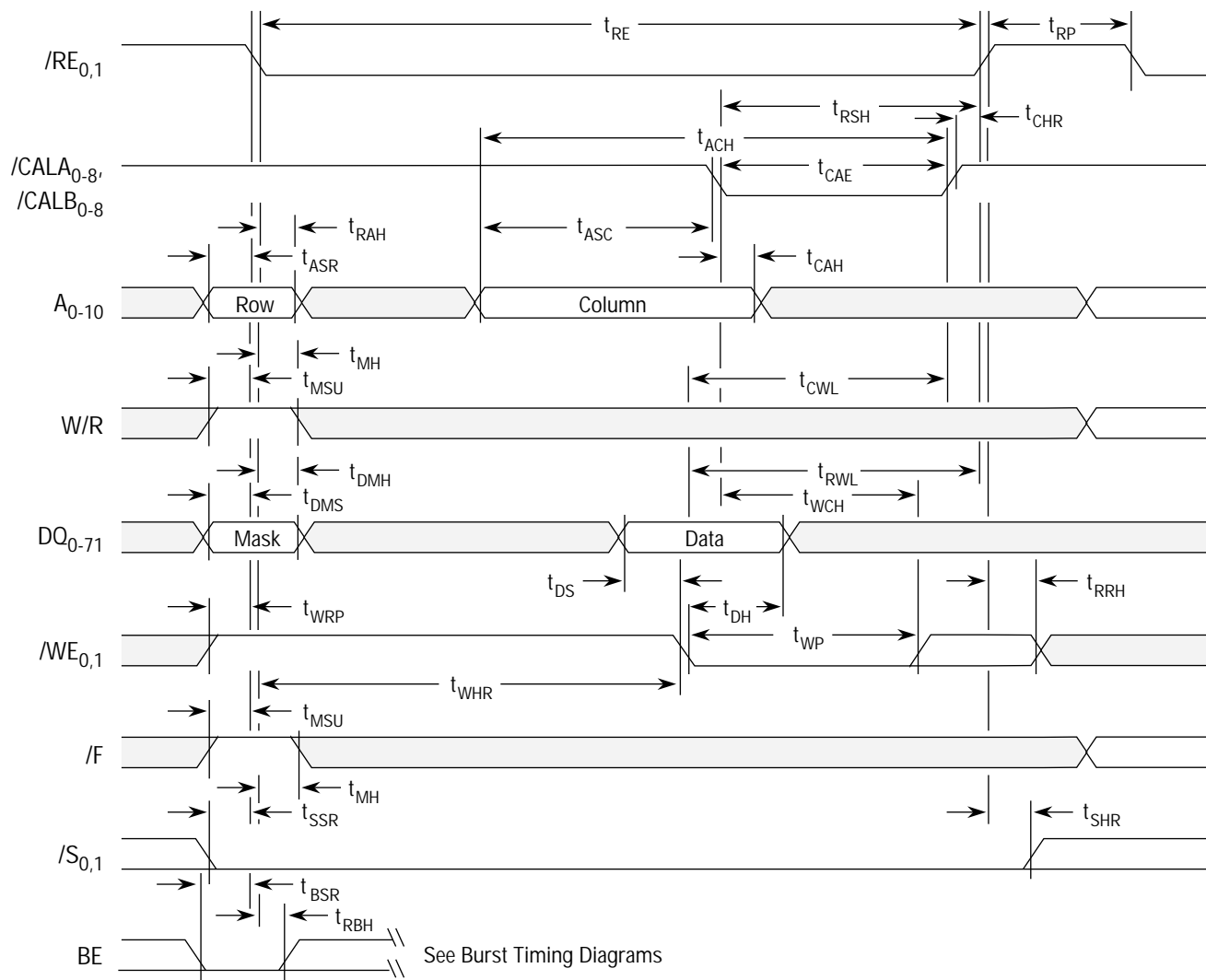
Don't Care or Indeterminate ☐

NOTES: 1. Data mask bit high (1) enables bit write; data mask bit low (0) inhibits bit write.
2. Write-per-bit cycle only valid for DM512K72.

Memory-To-Memory Transfer (Non-Pipelined)
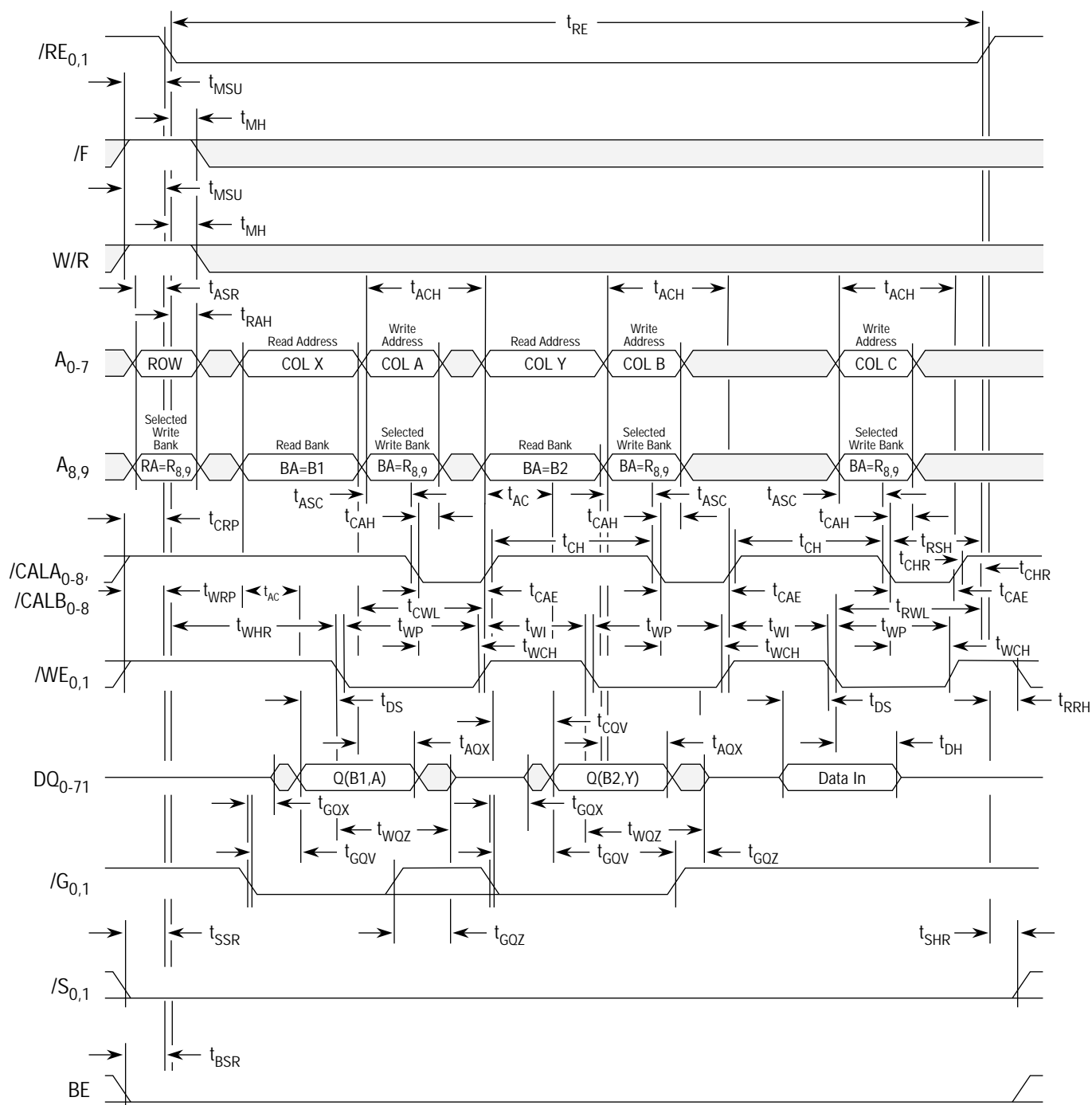
NOTES: 1. Reads may be from any of the cache banks, but writes only occur to the active row latched by /RE.
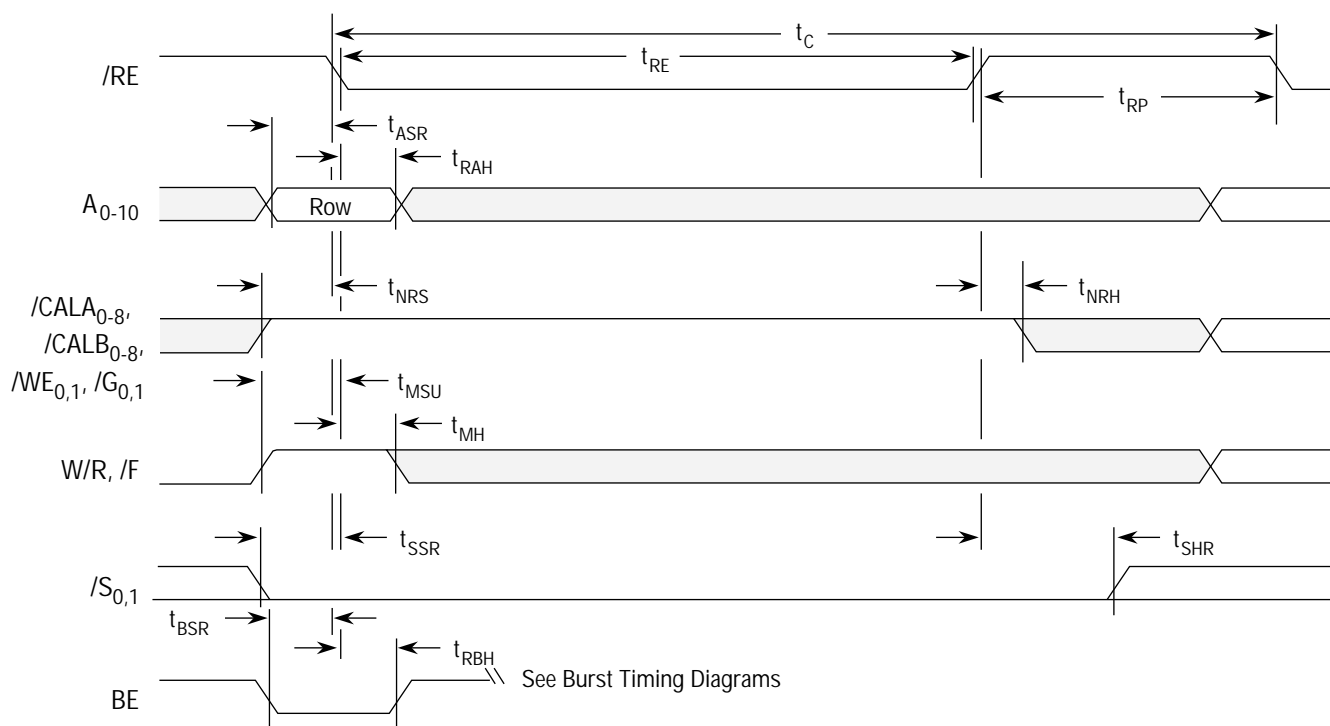2. Transfers can be within page, between pages, or between chips.

Don't Care or Indeterminate ☐

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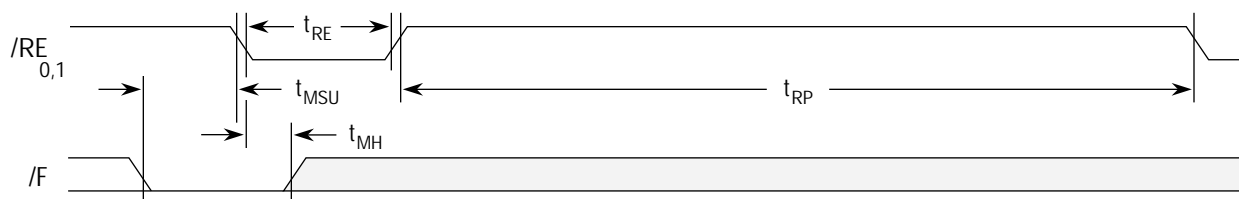
/F Refresh Cycle

Don't Care or Indeterminate ☐

NOTES: 1. During /F refresh cycles, the status of W/R, /WE, A_{0-10}, /CAL, /S, and /G is a don't care.
2. /RE inactive cache reads may be performed in parallel with /F refresh cycles.

/RE-Only Refresh

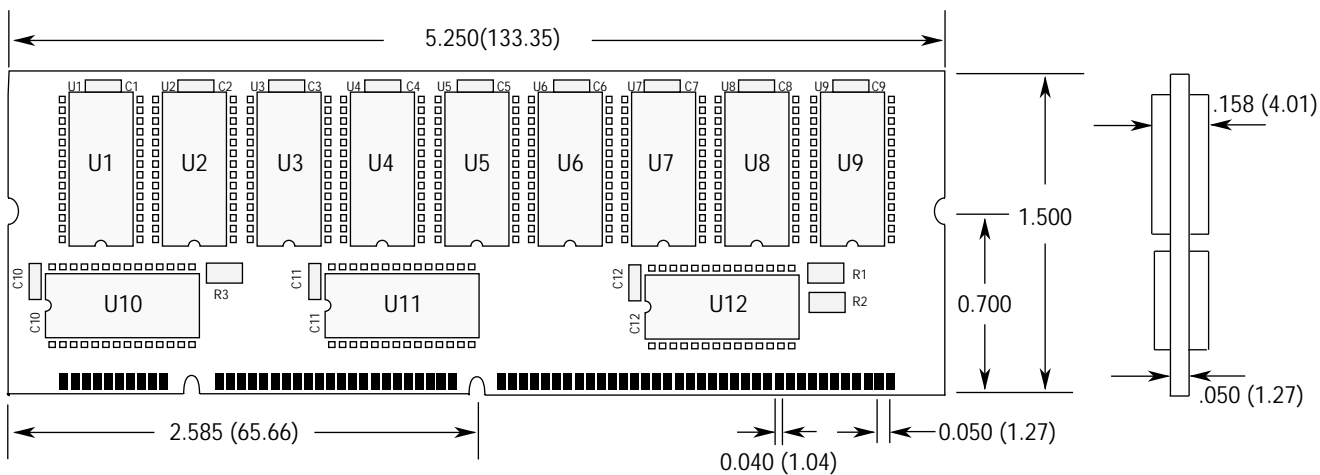See Burst Timing Diagrams

Don't Care or Indeterminate ☐

NOTES: 1. All binary combinations of A_{0-9} must be refreshed every 64ms interval. A_{10} does not have to be cycled, but must remain valid during row address setup and hold times.
2. /RE refresh is write cycle with no /CAL active cycle.

DIMM Module

Inches (mm)

5.250(133.35)

| U1 | U2 | U3 | U4 | U5 | U6 | U7 | U8 | U9 |

U10   R3   U11   U12   R1 / R2

2.585 (65.66)

0.040 (1.04)   0.050 (1.27)

.158 (4.01)

1.500

0.700

.050 (1.27)

U1-4, U6-9, U13-19, U18-21 — Enhanced DM2223T-xx, 512Kx8 EDRAM, 300 Mil TSOP
U5, U17 — Enhanced DM2233T-xx, 512Kx8 EDRAM with Write-per-bit (not present on DM512K64DT)
U10-12, U22-24 — IDT 74FCT162344ETPA CMOS Address/Clock Driver or Equivalent
C1-24 — 0.22µF Chip Capacitor
Socket — Robinson Nugent DIMS - 168BD5-TR or Equivalent

Part Numbering System

DM512K72DTE - 12N

└ **Error Check Mode (72-bit Only)**
Blank - Write-per-bit Parity
N - ECC (No write-per-bit)

Access Time from Cache in Nanoseconds
12ns
15ns

Packaging System
T = 300 Mil, Plastic TSOP - II

Memory Module Configuration
D= DIMM

I/O Width (Including Parity)
64 = 64 Bits
72 = 72 Bits

Memory Depth
512K
1M

Dynamic Memory