Enhanced Memory Systems Inc.

DM512K64DT6/DM512K72DT6 Multibank EDO EDRAM
512Kb x 64/512Kb x 72 Enhanced DRAM DIMM

Product Specification

Features

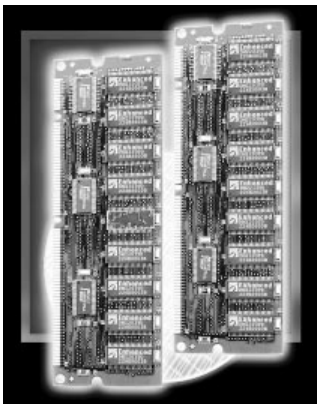
- 8Kbytes SRAM Cache Memory for 12ns Random Reads Within Four Active Pages (Multibank Cache)
- Fast 4Mbyte DRAM Array for 30ns Access to Any New Page
- Write Posting Registers for 12ns Random Writes and Burst Writes Within a Page (Hit or Miss)
- 2Kbyte Wide DRAM to SRAM Bus for 113.6 Gigabytes/Second Cache Fill Rate
- A Hit Pin Outputs Status on On-chip Page Hit/Miss Comparators to Simplify Control
- On-chip Cache Hit/Miss Comparators Automatically Maintain Cache Coherency on Writes
- Hidden Precharge & Refresh Cycles
- Extended 64ms Refresh Period for Low Standby Power
- CMOS/TTL Compatible I/O and +5 Volt Power Supply
- Output Latch Enable Allows Extended Data Output (EDO) for Faster System Operation

Description

The Enhanced Memory Systems 4MB enhanced DRAM (EDRAM)DIMM module provides a single memory module solution for the main memory or local memory of fast 64-bit embedded computers, communications switches, and other high performance systems. Due to its fast non-interleave architecture, the EDRAM DIMM module supports zero-wait-state burst read or write operation to 83MHz. The EDRAM outperforms conventional SRAM plus DRAM or synchronous DRAM memory systems by minimizing wait states on initial reads (hit or miss) and eliminating writeback delays.

Each 4Mbyte DIMM module has 8Kbytes of SRAM cache organized as four 256 x 72 row registers with 12ns initial access time. On a cache miss, the fast DRAM array reloads an entire 2Kbyte row register over a 2Kbyte-wide bus in just 18ns for an effective cache fill rate of 113.6 Gbytes/second. During write cycles, a write posting register allows the initial write to be posted as early as 5ns after column address is available. EDRAM supports direct non-interleave page writes at up to 83MHz. An on-chip hit/miss comparator automatically maintains cache coherency during writes.

Architecture

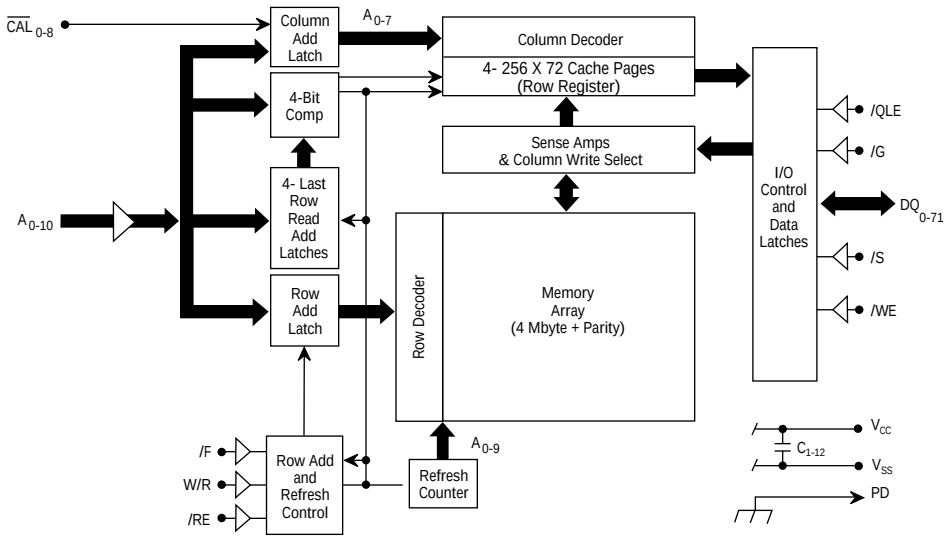


The DM512K72DT6 achieves 512Kb x 72 density by mounting nine 512Kx8 EDRAMs, packaged in low profile 44-pin TSOP-II packages on one side of the multi-layer substrate. Three high drive series terminated buffer chips buffer address and control lines. Twelve surface mount capacitors are used to decouple the power supply bus. The DM512K64DT contains eight 512Kx8 EDRAMs. The parity data component is not populated.

The EDRAM memory module architecture is very similar to two standard 2MB DRAM SIMM modules configured in a 64-bit wide, non-interleave configuration. The EDRAM module adds an integrated cache and cache control logic which allow the cache to operate much like a page mode or static column DRAM.

The EDRAM's SRAM cache is integrated into the DRAM array as tightly coupled row registers. Memory reads always occur from the 256 x 72 cache row register associated with a 1MB segment of DRAM. When the on-chip comparator detects a page hit, only the SRAM is accessed and data is available in 12ns from column address (the /HIT output is low to indicate a page hit). When a page miss is detected, the entire new DRAM row is loaded into cache and data is available at the output within 30ns from row enable (the /HIT output is high to indicate a page miss). Subsequent reads within a page (burst reads or random reads) will continue at 12ns cycle time. Since reads occur from the SRAM cache, the DRAM precharge can occur simultaneously without degrading performance. The on-chip refresh counter with independent

Functional Diagram



refresh bus allows the EDRAM to be refreshed during cache reads.

Memory writes can be posted as early as 6.5ns after row enable and are directed to the DRAM array. During a write hit, the on-chip address comparator activates a parallel write path to the SRAM cache to maintain coherency. Memory writes do not affect the contents of the cache row register except during write hits.

By integrating the SRAM cache as row registers in the DRAM array and keeping the on-chip control simple, the EDRAM is able to provide superior system performance at less cost, power, and area than systems implemented with complex synchronous SRAM cache, cache controllers, and multilevel data busses.

Functional Description

The EDRAM is designed to provide optimum memory performance with high speed microprocessors. As a result, it is possible to perform simultaneous operations to the DRAM and SRAM cache sections of the EDRAM. This feature allows the EDRAM to hide precharge and refresh operation during reads and maximize hit rate by maintaining page cache contents during write operations even if data is written to another memory page. These capabilities, in conjunction with the faster basic DRAM and cache speeds of the EDRAM, minimize processor wait states.

EDRAM Basic Operating Modes

The EDRAM operating modes are specified in the table.

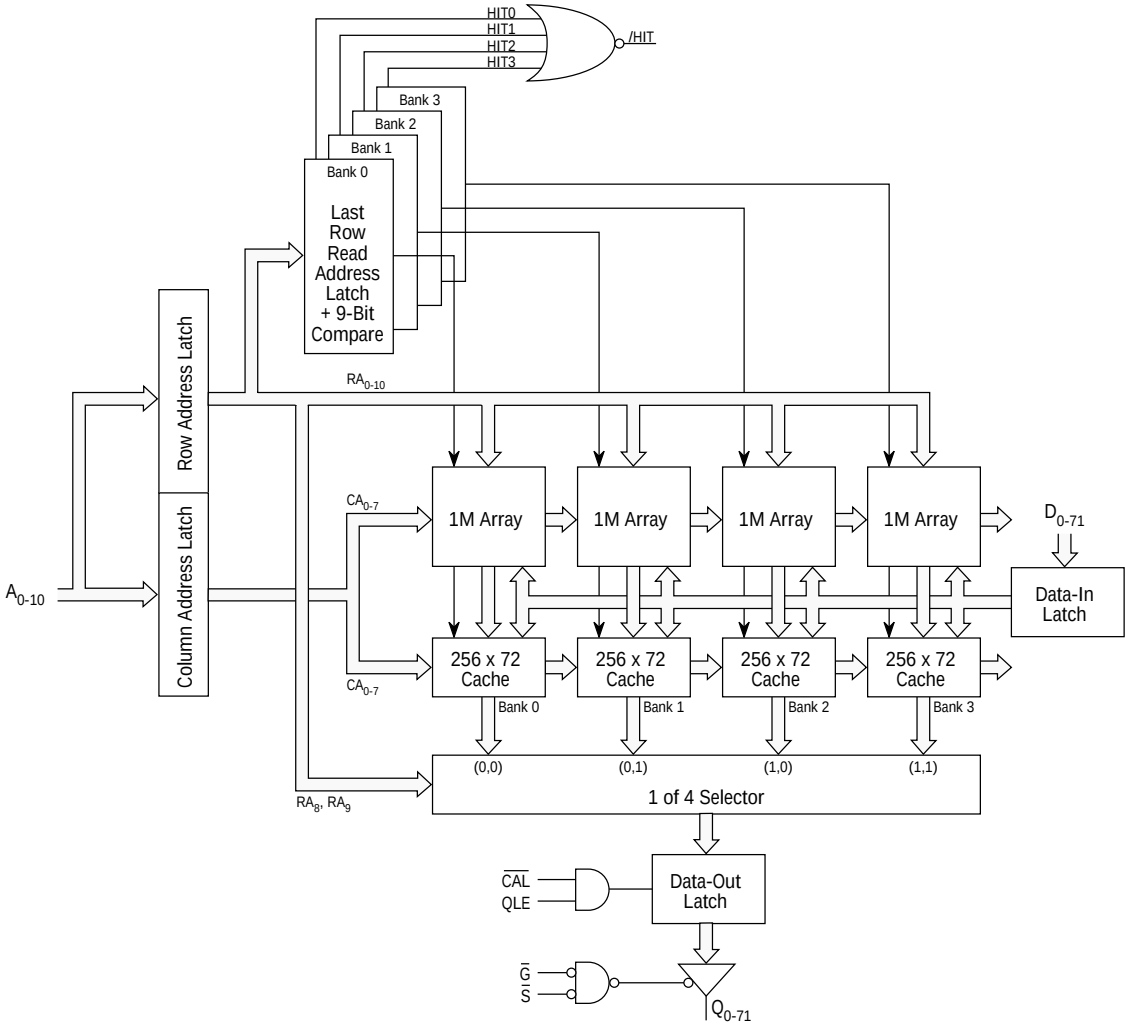
Hit and Miss Terminology

In this datasheet, "hit" and "miss" always refer to a hit or miss to any of the four pages of data contained in the SRAM cache row registers. There are four cache row registers, one for each of the four banks of DRAM. These registers are specified by the bank select row address bits A_8 and A_9. The contents of these cache row registers is always equal to the last row that was read from each of the four internal DRAM banks (as modified by any write hit data).

DRAM Read Hit

A DRAM read request is initiated by clocking /RE with W/R low and /F high. The EDRAM will compare the new row address to the last row read address latch for the bank specified by row address bits A_{8-9} (LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address matches the LRR, the requested data is already in the SRAM cache and no DRAM memory reference is initiated. The data specified by the row and column address is available at the output pins at the greater of times t_{AC} or t_{GQV}. The /HIT output is driven low at time t_{HV} after /RE to indicate the shorter access time to the

Four Bank Cache Architecture



external control logic. Since no DRAM activity is initiated, /RE can be brought high after time t_{RE1}, and a shorter precharge time, t_{RP1}, is required. Additional locations within the currently active page may be accessed concurrently with precharge by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address change in static column mode. During any read cycle, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address. In page mode, data valid time is determined by either t_{AC} and t_{CQV}.

DRAM Read Miss

A DRAM read request is initiated by clocking /RE with W/R low and /F high. The EDRAM will compare the new row address to the LRR address latch for the bank specified by row address bits A_{8-9} (LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address does not match the LRR, the requested data is not in SRAM cache and a new row is fetched from the DRAM. The EDRAM will load the new row data into the SRAM cache and update the LRR latch. The data at the specified column address is available at the output pins at the greater of times t_{RAC}, t_{AC}, and t_{GQV}. The /HIT output is driven high at time t_{HV} after /RE to indicate the longer access time to the external control logic. /RE may be brought high after time t_{RE} since the new row data is safely latched into SRAM cache. This allows the EDRAM to precharge the DRAM array while data is accessed from SRAM cache. Additional locations within the currently active page may be accessed by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address change in static column mode. During any read cycle, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address. In page mode, data valid time is determined by either t_{AC} and t_{CQV}.

DRAM Write Hit

A DRAM write request is initiated by clocking /RE while W/R, /CAL, /WE, and /F are high. The EDRAM will compare the new row address to the LRR address latch for the bank specified by row address bits A_{8-9} (LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address matches the LRR, the EDRAM will write data to both the DRAM page in the appropriate bank and its corresponding SRAM cache simultaneously to maintain coherency. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE (t_{RAH} + t_{ASC} for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. With /G enabled and /WE disabled, read operations may be performed while /RE is activated in write hit mode. This allows read-modify-write, write-verify, or random read-write sequences within the page with 12ns cycle times. During a write hit sequence, the /HIT output is driven low. At the end of any write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. Cache reads can be performed concurrently with precharge (see "/RE Inactive Operation"). When /RE is inactive, the cache reads will occur from the page accessed during the last /RE active read cycle.

DRAM Write Miss

A DRAM write request is initiated by clocking /RE while W/R, /CAL, /WE, and /F are high. The EDRAM will compare the new row address to the LRR address latch for the bank specified for row address bits A_{8-9} (LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address does not match any of the LRRs, the EDRAM will write data to the DRAM page in the appropriate bank and the contents of the current cache is not modified. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE (t_{RAH} + t_{ASC} for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. During a write miss sequence, the /HIT output is driven high, cache reads are inhibited, and the output buffers are disabled (independently of /G) until time t_{WRR} after /RE goes high. At the end of a write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. Cache reads can be performed concurrently with the precharge (see "/RE Inactive Operation"). When /RE is inactive, the cache reads will occur from the page accessed during the last /RE active read cycle.

/RE Inactive Operation

Data may be read from the SRAM cache without clocking /RE. This capability allows the EDRAM to perform cache read

EDRAM Basic Operating Modes

Function	/S	/RE	W/R	/F	A_{0-10}	Comment
Read Hit	L	↓	L	H	Row = LRR	No DRAM Reference, Data in Cache
Read Miss	L	↓	L	H	Row ≠ LRR	DRAM Row to Cache
Write Hit	L	↓	H	H	Row = LRR	Write to DRAM and Cache, Reads Enabled
Write Miss	L	↓	H	H	Row ≠ LRR	Write to DRAM, Cache Not Updated, Reads Disabled
Internal Refresh	X	↓	X	L	X	
Low Power Standby	H	H	X	X	X	Standby Current
Unallowed Mode	H	L	X	H	X	

H = High; L = Low; X = Don't Care; ↓ = High-to-Low Transition; LRR = Last Row Read

operations during precharge and refresh cycles to minimize wait states. It is only necessary to select /S and /G and provide the appropriate column address to read data as shown in the table below. In this mode of operation, the cache reads will occur from the page and bank accessed during the last /RE active read cycle. To perform a cache read in static column mode, /CAL is held high, and the cache contents at the specified column address will be valid at time t_{AC} after address is stable. To perform a cache read in page mode, /CAL is clocked to latch the column address. When /RE is inactive, the hit pin is not driven and is in a high impedance state.

This option is desirable when the external control logic is capable of fast hit/miss comparison. In this case, the controller can avoid the time required to perform row/column multiplexing on hit cycles.

Function	/S	/G	/CAL	A_{0-7}
Cache Read (Static Column)	L	L	H	Col Adr
Cache Read (Page Mode)	L	L	↕	Col Adr

EDO Mode and Output Latch Enable Operation

The QLE and /CAL inputs can be used to create extended data output (EDO) mode timings in either static column or page modes. The DM512K32DT6 has an output latch enable (QLE) that can be used to extend the data output valid time. The output latch enable operates as shown in the following table.

When QLE is low, the latch is transparent and the EDRAM operates identically to the standard EDRAMs. When /CAL is high during a static column mode read, the QLE input can be used to latch the output to extend the data output valid time. QLE can be held high during page mode reads. In this case, the data outputs are latched while /CAL is high and open when /CAL is not high.

QLE	/CAL	Comments
L	X	Output Transparent
↕	H	Output Latched When QLE=H (Static Column EDO)
H	↕	Output Latched When /CAL=H (Page Mode EDO)

Write-Per-Bit Operation

The DM512K72 DIMM offers a write-per-bit capability to selectively modify individual parity bits ($DQ_{8, 17, 26, 35, 44, 53, 62, 71}$) for byte write operations. The parity device (DM2213) is selected via $/CAL_8$. Byte write selection to non-parity bits is accomplished via $/CAL_{0-7}$. The bits to be written are determined by a bit mask data word which is placed on the parity I/O data pins prior to clocking /RE. The logic one bits in the mask data select the bits to be written. As soon as the mask is latched by /RE, the mask data is removed and write data can be placed on the data bus. The mask is only specified on the /RE transition. During page mode burst write operations, the same mask is used for all write operations.

ECC Operation

The DM512K72DT6-xxN supports error correction coding (ECC) by replacing the parity chip with a normal DM2203 device. This version does not support write-per-bit parity operation.

Internal Refresh

If /F is active (low) on the assertion of /RE, an internal refresh cycle is executed. This cycle refreshes the row address supplied by an internal refresh counter. This counter is incremented at the end of the cycle in preparation for the next /F refresh cycle. At least 1,024 /F cycles must be executed every 64ms. /F refresh cycles can be hidden because cache memory can be read under column address control throughout the entire /F cycle. /F cycles are the only active cycles where /S can be disabled.

/RE Only Refresh Operation

Although /F refresh using the internal refresh counter is the recommended method of EDRAM refresh, an /RE only refresh may be performed using an externally supplied row address. /RE refresh is performed by executing a *write cycle* (W/R, /G, and /F are high) where /CAL is not clocked. This is necessary so that the current cache contents and LRR are not modified by the refresh operation. All combinations of addresses A_{0-9} must be sequenced every 64ms refresh period. A_{10} does not need to be cycled. Read refresh cycles are not allowed because a DRAM refresh cycle does not occur when a read refresh address matches the LRR address latch.

Low Power Mode

The EDRAM enters its low power mode when /S is high. In this mode, the internal DRAM circuitry is powered down to reduce standby current.

Initialization Cycles

A minimum of eight /RE active initialization cycles (read, write, or refresh) are required before normal operation is guaranteed. Following these start-up cycles, two read cycles to different row addresses must be performed for each of the four internal banks of DRAM to initialize the internal cache logic. Row address bits A_8 and A_9 define the four internal DRAM banks.

Unallowed Mode

Read, write, or /RE only refresh operations must not be performed to unselected memory banks by clocking /RE when /S is high.

Reduced Pin Count Operation

Although it is desirable to use all EDRAM control pins to optimize system performance, the interface to the EDRAM may be simplified to reduce the number of control lines by either tying pins to ground or by tying one or more control inputs together. The /S input can be tied to ground if the low power standby mode is not required. The QLE input can be tied low if output latching is not required, or it can be tied high if "extended data out" (hyper page mode) is required. The /HIT output pin is not necessary for device operation. The W/R and /G inputs can be tied together if reads are not required during a write hit cycle. The simplified control interface still allows the fast page read/write cycle times, fast random read/write times, and hidden precharge functions available with the EDRAM.

Pin Descriptions

/RE — Row Enable

These inputs are used to initiate DRAM read and write operations and latch a row address. It is not necessary to clock /RE to read data from the EDRAM SRAM row register. On read operations, /RE can be brought high as soon as data is loaded into cache to allow early precharge.

/CAL$_{0-8}$ — Column Address Latch

These inputs are used to latch the column address and in combination with /WE to trigger write operations. When /CAL is high, the column address latch is transparent. When /CAL is low, the column address latch contains the address present at the time /CAL went low. Individual /CAL inputs are provided for each byte of EDRAM to allow byte write capability.

W/R — Write/Read

This input along with /F input specifies the type of DRAM operation initiated on the low going edge of /RE. When /F is high, W/R specifies either a write (logic high) or read operation (logic low).

/F — Refresh

This input will initiate a DRAM refresh operation using the internal refresh counter as an address source when it is low on the low going edge of /RE.

/WE — Write Enable

This input controls the latching of write data on the input data pins. A write operation is initiated when both the /CAL for the specified byte and /WE are low.

/G — Output Enable

This input controls the gating of read data to the output data pins during read operations.

/S — Chip Select

This input is used to power up the I/O and clock circuitry. When /S is high, the EDRAM remains in a powered-down condition. Read or write cycles must not be executed when /S is high. /S must remain low throughout any read or write operation. Only /F refresh operation can be executed when, /S is not enabled.

DQ$_{0-71}$ — Data Input/Output

These CMOS/TTL bidirectional data pins are used to read and write data to the EDRAM. On the DM2213 write-per-bit memory, these pins are also used to specify the bit mask used during write operations.

A$_{0-10}$ — Multiplex Address

These inputs are used to specify the row and column addresses of the EDRAM data. The 11-bit row address is latched on the falling edge of /RE. The 8-bit column address can be specified at any other time to select read data from the SRAM cache or to specify the write column address during write cycles.

QLE — Output Latch Enable

This input enables the EDRAM output latches. When QLE is low, the output latch is transparent. Data is latched when both /CAL and QLE are high. This allows output data to be extended during either static column or page mode read cycles.

/HIT — Hit Pin

This output pin will be driven during /RE active read or write cycles to indicate the hit/miss status of the cycle.

PD — Presence Detect

This output will indicate if the DIMM module is inserted in a socket. When a DIMM is inserted, this pin is grounded. When no DIMM is present, the pin is open.

V_{CC} Power Supply

These inputs are connected to the +5 volt power supply.

V_{SS} Ground

These inputs are connected to the power supply ground connection.

Pinout

Pin No.	Function	Interconnect (Component Pin)	Organization
1	Vss		Ground
2	DQ_0	U1-4	Byte 0, I/O 0
3	DQ_1	U1-6	Byte 0, I/O 1
4	DQ_2	U1-7	Byte 0, I/O 2
5	DQ_3	U1-9	Byte 0, I/O 3
6	V_{DD}		+5 Volts
7	DQ_4	U1-13	Byte 0, I/O 4
8	DQ_5	U1-15	Byte 0, I/O 5
9	DQ_6	U1-16	Byte 0, I/O 6
10	DQ_7	U1-18	Byte 0, I/O 7
11	DQ_8	U5-4	Parity, I/O 0
12	V_{SS}		Ground
13	DQ_9	U3-4	Byte 1, I/O 0
14	DQ_{10}	U3-6	Byte 1, I/O 1
15	DQ_{11}	U3-7	Byte 1, I/O 2
16	DQ_{12}	U3-9	Byte 1, I/O 3
17	DQ_{13}	U3-13	Byte 1, I/O 4
18	V_{DD}		+5 Volts
19	DQ_{14}	U3-15	Byte 1, I/O 5
20	DQ_{15}	U3-16	Byte 1 I/O 6
21	DQ_{16}	U3-18	Byte 1 I/O 7
22	DQ_{17}	U5-6	Parity, I/O 1
23	V_{SS}		Ground
24	V_{SS}		Ground
25	V_{DD}		+5 Volts
26	V_{DD}		+5 Volts
27	/WE	U10A-8	Write Enable
28	/CAL0	U1-32	Byte 0 /CAL
29	/CAL2	U6-32	Byte 2 /CAL
30	/S	U10A-14	Chip Select
31	/G	U10B-15	Output Enable
32	V_{SS}		Ground
33	A_0	U10B-21	Address 0
34	A_2	U11A-8	Address 2
35	A_4	U11A-14	Address 4
36	A_6	U11B-15	Address 6
37	A_8	U11B-21	Address 8
38	A_{10}	U11C-36	Address 10
39	N.C.		
40	V_{DD}		+5 Volts
41	V_{DD}		+5 Volts
42	QLE	U12A-8	Output Latch Enable

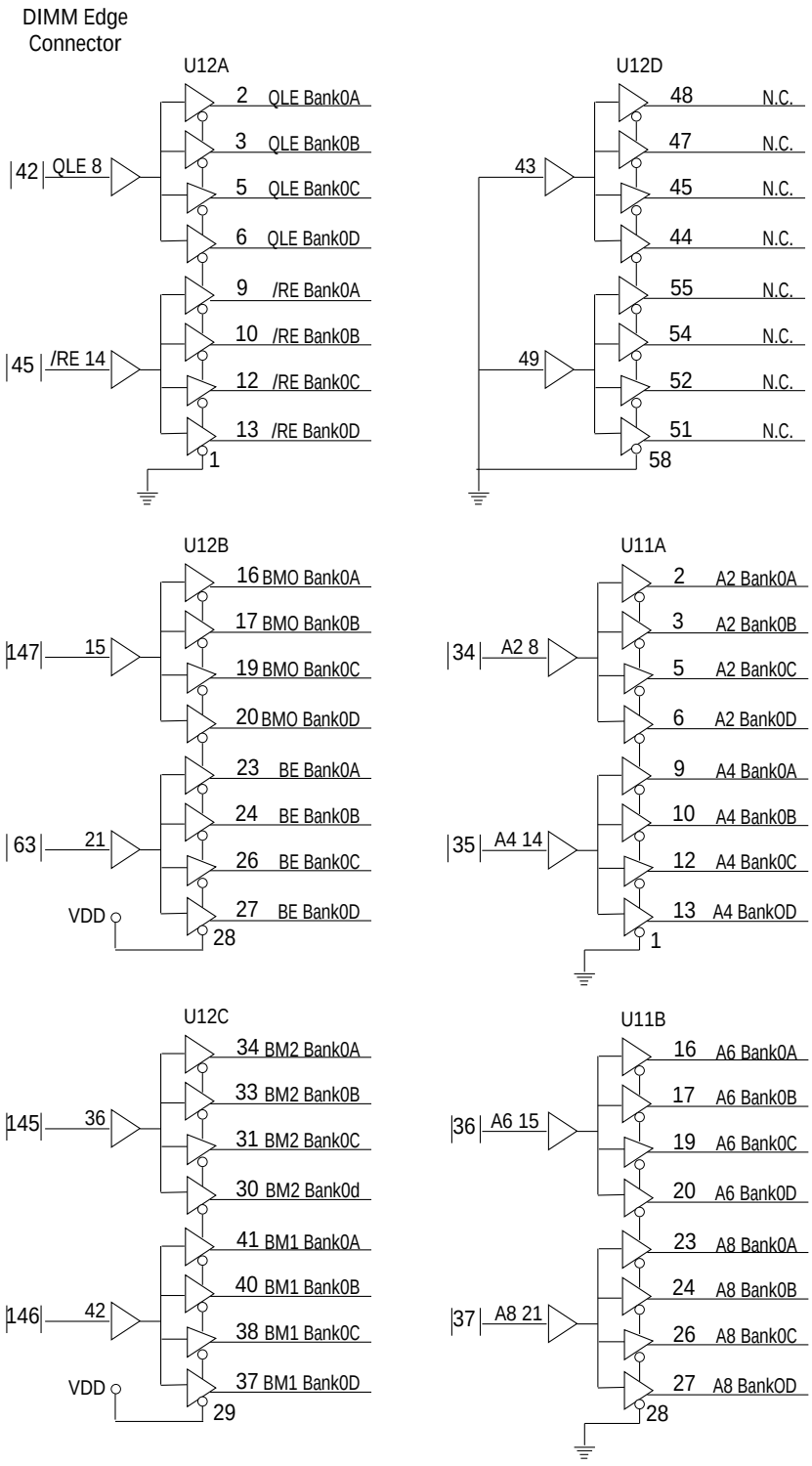
Pin No.	Function	Interconnect (Component Pin)	Organization
85	V_{SS}		Ground
86	DQ_{36}	U2-4	Byte 4, I/O 0
87	DQ_{37}	U2-6	Byte 4, I/O 1
88	DQ_{38}	U2-7	Byte 4, I/O 2
89	DQ_{39}	U2-9	Byte 4 I/O 3
90	V_{DD}		+5 Volts
91	DQ_{40}	U2-13	Byte 4 I/O 4
92	DQ_{41}	U2-15	Byte 4 I/O 5
93	DQ_{42}	U2-16	Byte 4, I/O 6
94	DQ_{43}	U2-18	Byte 4, I/O 7
95	DQ_{44}	U5-13	Parity, I/O 4
96	V_{SS}		Ground
97	DQ_{45}	U4-4	Byte 5, I/O 0
98	DQ_{46}	U4-6	Byte 5, I/O 1
99	DQ_{47}	U4-7	Byte 5, I/O 2
100	DQ_{48}	U4-9	Byte 5, I/O 3
101	DQ_{49}	U4-13	Byte 5, I/O 4
102	V_{DD}		+5 Volts
103	DQ_{50}	U4-15	Byte 5, I/O 5
104	DQ_{51}	U4-16	Byte 5, I/O 6
105	DQ_{52}	U4-18	Byte 5, I/O 7
106	DQ_{53}	U5-15	Parity, I/O 5
107	V_{SS}		Ground
108	V_{SS}		Ground
109	V_{DD}		+5 Volts
110	V_{DD}		+5 Volts
111	/F	U10D-49	Refresh Pin
112	/CAL1	U3-32	Byte 1 /CAL
113	/CAL3	U8-32	Byte 3 /CAL
114	N.C.	N.C.	
115	W/R	U10D-43	Write/Read Mode
116	V_{SS}		Ground
117	A_1	U10C-42	Address 1
118	A_3	U10C-36	Address 3
119	A_5	U11D-49	Address 5
120	A_7	U11D-43	Address 7
121	A_9	U11C-42	Address 9
122	N.C.		
123	N.C.		
124	V_{DD}		+5 Volts
125	N.C.	N.C.	
126	N.C.	N.C.	

Pinout

Pin No.	Function	Interconnect (Component Pin)	Organization
43	V_{SS}		Ground
44	N.C.	N.C.	
45	/RE	U12A-14	Row Enable
46	/CAL4	U2-32	Byte 4 /CAL
47	/CAL6	U7-32	Byte 6 /CAL
48	N.C.	N.C.	
49	V_{DD}		+5 Volts
50	V_{DD}		+5 Volts
51	V_{SS}		Ground
52	DQ_{18}	U6-4	Byte 2, I/O 0
53	DQ_{19}	U6-6	Byte 2, I/O 1
54	V_{SS}		Ground
55	DQ_{20}	U6-7	Byte 2, I/O 2
56	DQ_{21}	U6-9	Byte 2, I/O 3
57	DQ_{22}	U6-13	Byte 2, I/O 4
58	DQ_{23}	U6-15	Byte 2, I/O 5
59	V_{DD}		+5 Volts
60	DQ_{24}	U6-16	Byte 2, I/O 6
61	PD		Ground
62	N.C.	N.C.	
63	N.C.	U12B-21	
64	V_{SS}		Ground
65	DQ_{25}	U6-18	Byte 2, I/O 7
66	DQ_{26}	U5-7	Parity, I/O 2
67	DQ_{27}	U8-4	Byte 3, I/O 0
68	V_{SS}		Ground
69	DQ_{28}	U8-6	Byte 3, I/O 1
70	DQ_{29}	U8-7	Byte 3, I/O 2
71	DQ_{30}	U8-9	Byte 3, I/O 3
72	DQ_{31}	U8-13	Byte 3, I/O 4
73	V_{DD}		+5 Volts
74	DQ_{32}	U8-15	Byte 3, I/O 5
75	DQ_{33}	U8-16	Byte 3, I/O 6
76	DQ_{34}	U8-18	Byte 3, I/O 7
77	DQ_{35}	U5-9	Parity, I/O 3
78	V_{SS}		Ground
79	N.C.	N.C.	
80	N.C.	N.C.	
81	N.C.	N.C.	
82	N.C.	N.C.	
83	V_{DD}		+5 Volts
84	V_{DD}		+5 Volts

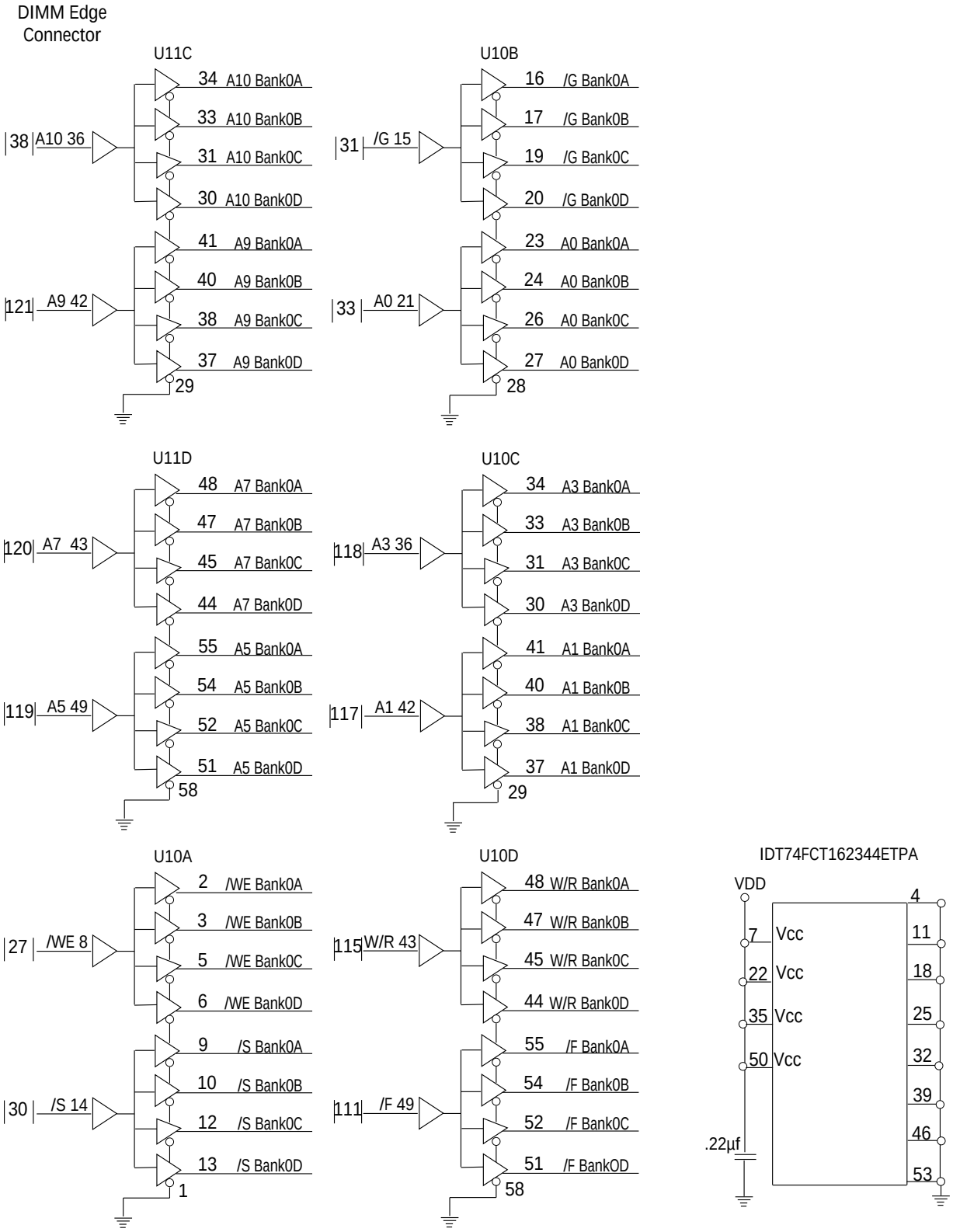
Pin No.	Function	Interconnect (Component Pin)	Organization
127	V_{SS}		Ground
128	V_{SS}		Ground
129	N.C.	N.C.	
130	/CAL5	U4-32	Byte 5
131	/CAL7	U9-32	Byte 7
132	/CAL8	U5-32	Parity
133	V_{DD}		+5 Volts
134	V_{DD}		+5 Volts
135	V_{SS}		Ground
136	DQ_{54}	U7-4	Byte 6, I/O 0
137	DQ_{55}	U7-6	Byte 6, I/O 1
138	V_{SS}		Ground
139	DQ_{56}	U7-7	Byte 6, I/O 2
140	DQ_{57}	U7-9	Byte 6, I/O 3
141	DQ_{58}	U7-13	Byte 6, I/O 4
142	DQ_{59}	U7-15	Byte 6, I/O 5
143	V_{DD}		+5 Volts
144	DQ_{60}	U7-16	Byte 6, I/O 6
145	/Hit	U12C-36	Hit Output
146	N.C.	U12C-42	
147	N.C.	U12B-15	
148	V_{SS}		Ground
149	DQ_{61}	U7-18	Byte 6, I/O 7
150	DQ_{62}	U5-16	Parity, I/O 6
151	DQ_{63}	U9-4	Byte 7, I/O 0
152	V_{SS}		Ground
153	DQ_{64}	U9-6	Byte 7, I/O 1
154	DQ_{65}	U9-7	Byte 7, I/O 2
155	DQ_{66}	U9-9	Byte 7, I/O 3
156	DQ_{67}	U9-13	Byte 7, I/O 4
157	V_{SS}		+5 Volts
158	DQ_{68}	U9-15	Byte 7, I/O 5
159	DQ_{69}	U9-16	Byte 7, I/O 6
160	DQ_{70}	U9-18	Byte 7, I/O 7
161	DQ_{71}	U5-18	Parity, I/O 7
162	V_{SS}		Ground
163	N.C.	N.C.	
164	N.C.	N.C.	
165	N.C.	N.C.	
166	N.C.	N.C.	
167	V_{DD}		+5 Volts
168	V_{DD}		+5 Volts

Buffer Diagrams



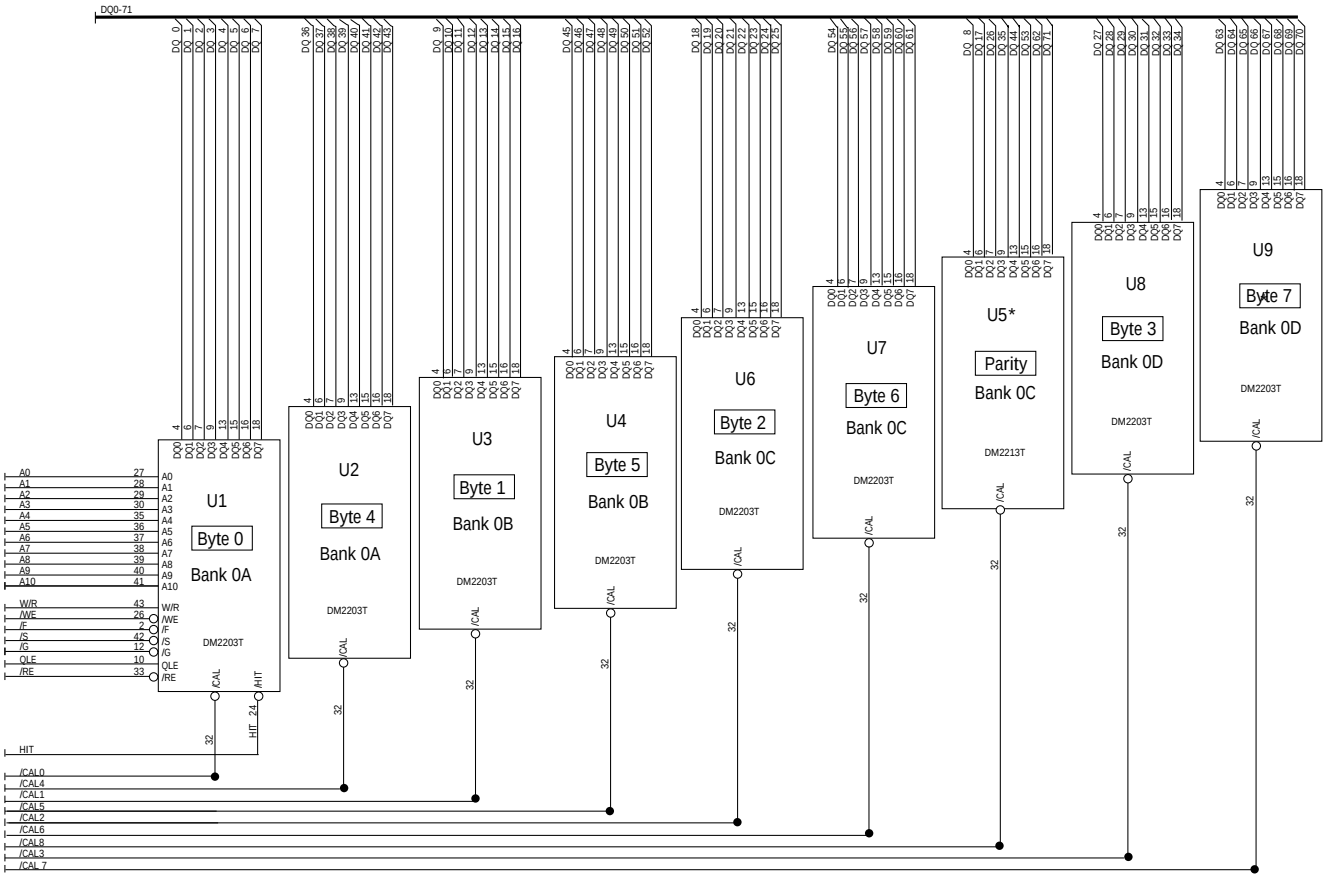
Note: Address and control buffers add a minimum of 1.5ns and a maximum of 3.8ns delay to each signal path.

Buffer Diagrams



Note: Address and control buffers add a minimum of 1.5ns and a maximum of 3.8ns delay to each signal path.

Interconnect Diagram



Note: For reference to buffer connection, append bank name to address or clock name, i.e., A10 + Bank 0A = A10BANK0A. Refer to Buffer Interconnect Diagram for detailed buffer connections. DQ0-71 and /CAL0-8 are directly connected to pins.

* Not Present on DM512K64

Pin Names

Pin Names	Function
A_{0-10}	Address Inputs
/RE	Row Enable
DQ_{0-71}	Data In/Data Out
$/CAL_{0-8}$	Column Address Latch
W/R	Write/Read Control
V_{CC}	Power (+5V)
V_{SS}	Ground

Pin Names	Function
/WE	Write Enable
/G	Output Enable
/F	Refresh Control
/S	Chip Select
/HIT	Hit Output
QLE	Output Latch Enable
NC	Not Connected

Absolute Maximum Ratings

(Beyond Which Permanent Damage Could Result)

Description	Ratings
Input Voltage (V_{IN})	- 1 ~ V_{CC}+1
Output Voltage (V_{OUT})	- 1 ~ V_{CC}+1
Power Supply Voltage (V_{CC})	- 1 ~ 7v
Ambient Operating Temperature (T_A)	-40 ~ +70°C
Storage Temperature (T_S)	-55 ~ 150°C
Static Discharge Voltage (Per MIL-STD-883 Method 3015)	Class 1
Short Circuit O/P Current (I_{OUT})	50mA*

*One output at a time; short duration.

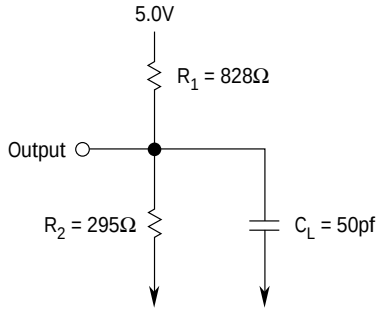
Capacitance

Description	Max	Pins
Input Capacitance	14pf	A_{0-10}
Input Capacitance	14pf	$/CAL_{0-8}$
Input Capacitance	10pf	/G, QLE
Input Capacitance	14pf	W/R, /F
I/O Capacitance	15pf	DQ_{0-71}
Input Capacitance	12pf	/RE, /S
Input Capacitance	12pf	/HIT

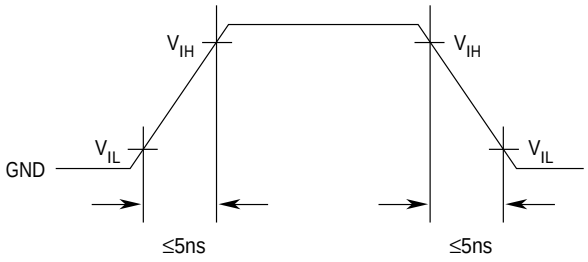
AC Test Load and Waveforms

V_{IN} Timing Reference Point at V_{IL} and V_{IH}

V_{OUT} Timing Referenced to 1.5 Volts



Load Circuit



Input Waveforms

Electrical Characteristics

T_A = 0 - 70°C (Commercial)

Symbol	*Parameters*	*Min*	*Max*	*Test Conditions*
V_{CC}	Supply Voltage	4.75V	5.25V	All Voltages Referenced to V_{SS}
V_{IH}	Input High Voltage	2.4V	V_{CC}+1	
V_{IL}	Input Low Voltage	-1.0V	0.8V	
V_{OH}	Output High Level	2.4V	—	I_{OUT} = - 5mA
V_{OL}	Output Low Level	—	0.4V	I_{OUT} = 4.2mA
$V_{i(L)}$	Input Leakage Current	-90µA	90µA	0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V
$V_{0(L)}$	Output Leakage Current	-90µA	90µA	0V ≤ V_{IN}, 0V ≤ V_{OUT} ≤ 5.5V

DM512K72DT6

Symbol	*Operating Current*	*33MHz Typ(1)*	*-12 Max*	*-15 Max*	*Test Condition*	*Notes*
I_{CC1}	Random Read	1166mA	2465mA	1970mA	/RE, /CAL, /G and Addresses Cycling: t_C = t_C Minimum	2, 3
I_{CC2}	Fast Page Mode Read	761mA	1745mA	1385mA	/CAL, /G and Addresses Cycling: t_{PC} = t_{PC} Minimum	2, 4
I_{CC3}	Static Column Read	671mA	1430mA	1160mA	/G and Addresses Cycling: t_{AC} = t_{AC} Minimum	2, 4
I_{CC4}	Random Write	1391mA	2150mA	1700mA	/RE, /CAL, /WE and Addresses Cycling: t_C = t_C Minimum	2, 3
I_{CC5}	Fast Page Mode Write	626mA	1655mA	1295mA	/CAL, /WE and Addresses Cycling: t_{PC} = t_{PC} Minimum	2, 4
I_{CC6}	Standby	11mA	11mA	11mA	All Control Inputs Stable ≥ V_{CC} - 0.2V, Outputs Driven	
I_{CCT}	Average Typical Operating Current	446mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

DM512K64DT6

Symbol	*Operating Current*	*33MHz Typ(1)*	*-12 Max*	*-15 Max*	*Test Condition*	*Notes*
I_{CC1}	Random Read	1056mA	2240mA	1790mA	/RE, /CAL, /G and Addresses Cycling: t_C = t_C Minimum	2, 3
I_{CC2}	Fast Page Mode Read	696mA	1600mA	1270mA	/CAL, /G and Addresses Cycling: t_{PC} = t_{PC} Minimum	2, 4
I_{CC3}	Static Column Read	616mA	1320mA	1070mA	/G and Addresses Cycling: t_{AC} = t_{AC} Minimum	2, 4
I_{CC4}	Random Write	1256mA	1960mA	1550mA	/RE, /CAL, /WE and Addresses Cycling: t_C = t_C Minimum	2, 3
I_{CC5}	Fast Page Mode Write	576mA	1520mA	1190mA	/CAL, /WE and Addresses Cycling: t_{PC} = t_{PC} Minimum	2, 4
I_{CC6}	Standby	10mA	10mA	10mA	All Control Inputs Stable ≥ V_{CC} - 0.2V, Outputs Driven	
I_{CCT}	Average Typical Operating Current	416mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

(1) "33MHz Typ" refers to worst case I_{CC} expected in a system operating with a 33MHz memory bus. See power applications note for further details. This parameter is not 100% tested or guaranteed.

(2) I_{CC} is dependent on cycle rates and is measured with CMOS levels and the outputs open.

(3) I_{CC} is measured with a maximum of one address change while /RE = V_{IL}

(4) I_{CC} is measured with a maximum of one address change while /CAL = V_{IH}

Switching Characteristics Note: These parameters do not include buffer delays. See pages 2-144-5 for derating factors.V_{CC} = 5V ± 5%, T_A = 0 to 70°C, C_L = 50pf

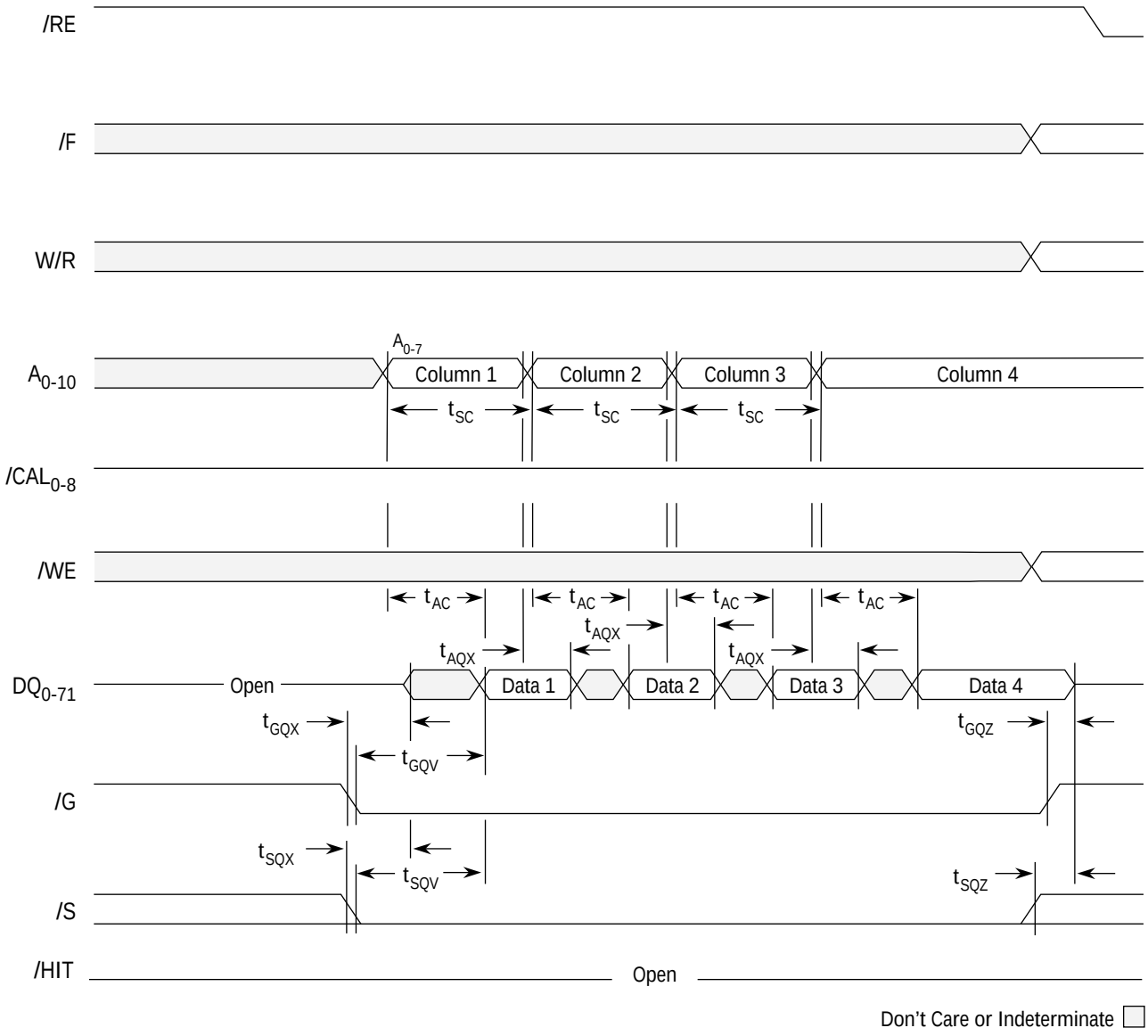
Symbol	Description	-12		-15		Units
		Min	Max	Min	Max	
t_{AC}(1)	Column Address Access Time		12		15	ns
t_{ACH}	Column Address Valid to /CAL Inactive (Write Cycle)	12		15		ns
t_{ACI}	Address Valid to /CAL Inactive (QLE High)	12		15		ns
t_{AHQ}	Column Address Hold From QLE High (/CAL=H)	0		0		ns
t_{AQH}	Address Valid to QLE High	12		15		ns
t_{AQX}	Column Address Change to Output Data Invalid	5		5		ns
t_{ASC}	Column Address Setup Time	5		5		ns
t_{ASR}	Row Address Setup Time	5		5		ns
t_C	Row Enable Cycle Time	55		65		ns
t_{C1}	Row Enable Cycle Time, Cache Hit (Row=LRR), Read Cycle Only	20		25		ns
t_{CAE}	Column Address Latch Active Time	5		6		ns
t_{CAH}	Column Address Hold Time	0		0		ns
t_{CH}	Column Address Latch High Time (Latch Transparent)	5		5		ns
t_{CHR}	/CAL Inactive Lead Time to /RE Inactive (Write Cycles Only)	-2		-2		ns
t_{CHW}	Column Address Latch High to Write Enable Low (Multiple Writes)	0		0		ns
t_{CLV}	Column Address Latch Low to Data Valid (QLE High)		7		7	ns
t_{CQH}	Column Address Latch Low to Data Invalid (QLE High)	0		0		ns
t_{CQV}	Column Address Latch High to Data Valid		15		15	ns
t_{CQX}	Column Address Latch Inactive to Data Invalid	5		5		ns
t_{CRP}	Column Address Latch Setup Time to Row Enable	5		5		ns
t_{CWL}	/WE Low to /CAL Inactive	5		5		ns
t_{DH}	Data Input Hold Time	0		0		ns
t_{DMH}	Mask Hold Time From Row Enable (Write-Per-Bit)	1		1.5		ns
t_{DMS}	Mask Setup Time to Row Enable (Write-Per-Bit)	5		5		ns
t_{DS}	Data Input Setup Time	5		5		ns
t_{GQV}(1)	Output Enable Access Time		5		5	ns
t_{GQX}(2,3)	Output Enable to Output Drive Time	0	5	0	5	ns
t_{GQZ}(4,5)	Output Turn-Off Delay From Output Disabled (/G↑)	0	5	0	5	ns
t_{HV}	Hit Valid From Row Enable		5		5	ns
t_{HZ}	Hit Turn-Off From Row Enable Going High	0		0		ns
t_{MH}	/F and W/R Mode Select Hold Time	0		0		ns
t_{MSU}	/F and W/R Mode Select Setup Time	5		5		ns
t_{NRH}	/CAL, /G, and /WE Hold Time For /RE-Only Refresh	0		0		ns
t_{NRS}	/CAL, /G, and /WE Setup Time For /RE-Only Refresh	5		5		ns
t_{PC}	Column Address Latch Cycle Time	12		15		ns
t_{QCI}	QLE High to /CAL Inactive	0		0		ns
t_{QH}	QLE High Time	5		5		ns

Switching Characteristics Note: These parameters do not include buffer delays. See pages 2-144-5 for derating factors.V_{CC} = 5V ± 5%, T_A = 0 to 70°C, C_L = 50pf

Symbol	Description	-12		-15		Units
		Min	Max	Min	Max	
t_{QL}	QLE Low Time	5		5		ns
t_{QQH}	Data Hold From QLE Inactive	2		2		ns
t_{QQV}	Data Valid From QLE Low		7.5		7.5	ns
t_{RAC}(1)	Row Enable Access Time, On a Cache Miss		30		35	ns
t_{RAC1}(1)	Row Enable Access Time, On a Cache Hit (Limit Becomes t_{AC})		15		17	ns
t_{RAH}	Row Address Hold Time	1		1.5		ns
t_{RE}	Row Enable Active Time	30	100000	35	100000	ns
t_{RE1}	Row Enable Active Time, Cache Hit (Row=LRR) Read Cycle	8		10		ns
t_{REF}	Refresh Period		64		64	ms
t_{RGX}	Output Enable Don't Care From Row Enable (Write, Cache Miss), DQ = Hi-Z	9		10		ns
t_{RQX1}(2,5)	Row Enable High to Output Turn-On After Write Miss	0	12		15	ns
t_{RP}	Row Precharge Time	20		25		ns
t_{RP1}	Row Precharge Time, Cache Hit (Row=LRR) Read Cycle	8		10		ns
t_{RRH}	Write Enable Don't Care From Row Enable (Write Only)	0		0		ns
t_{RSH}	Last Write Address Latch to End of Write	12		15		ns
t_{RSW}	Row Enable to Column Address Latch Low For Second Write	35		40		ns
t_{RWL}	Last Write Enable to End of Write	12		15		ns
t_{SC}	Column Address Cycle Time	12		15		ns
t_{SHR}	Select Hold From Row Enable	0		0		ns
t_{SQV}(1)	Chip Select Access Time		12		15	ns
t_{SQX}(2,3)	Output Turn-On From Select Low	0	12	0	15	ns
t_{SQZ}(4,5)	Output Turn-Off From Chip Select	0	8	0	10	ns
t_{SSR}	Select Setup Time to Row Enable	5		5		ns
t_T	Transition Time (Rise and Fall)	1	10	1	10	ns
t_{WC}	Write Enable Cycle Time	12		15		ns
t_{WCH}	Column Address Latch Low to Write Enable Inactive Time	5		5		ns
t_{WHR}(6)	Write Enable Hold After /RE	0		0		ns
t_{WI}	Write Enable Inactive Time	5		5		ns
t_{WP}	Write Enable Active Time	5		5		ns
t_{WQV}(1)	Data Valid From Write Enable High		12		15	ns
t_{WQX}(2,5)	Data Output Turn-On From Write Enable High	0	12	0	15	ns
t_{WQZ}(3,4)	Data Turn-Off From Write Enable Low	0	12	0	15	ns
t_{WRP}	Write Enable Setup Time to Row Enable	5		5		ns
t_{WRR}	Write to Read Recovery (Following Write Miss)		12		15	ns

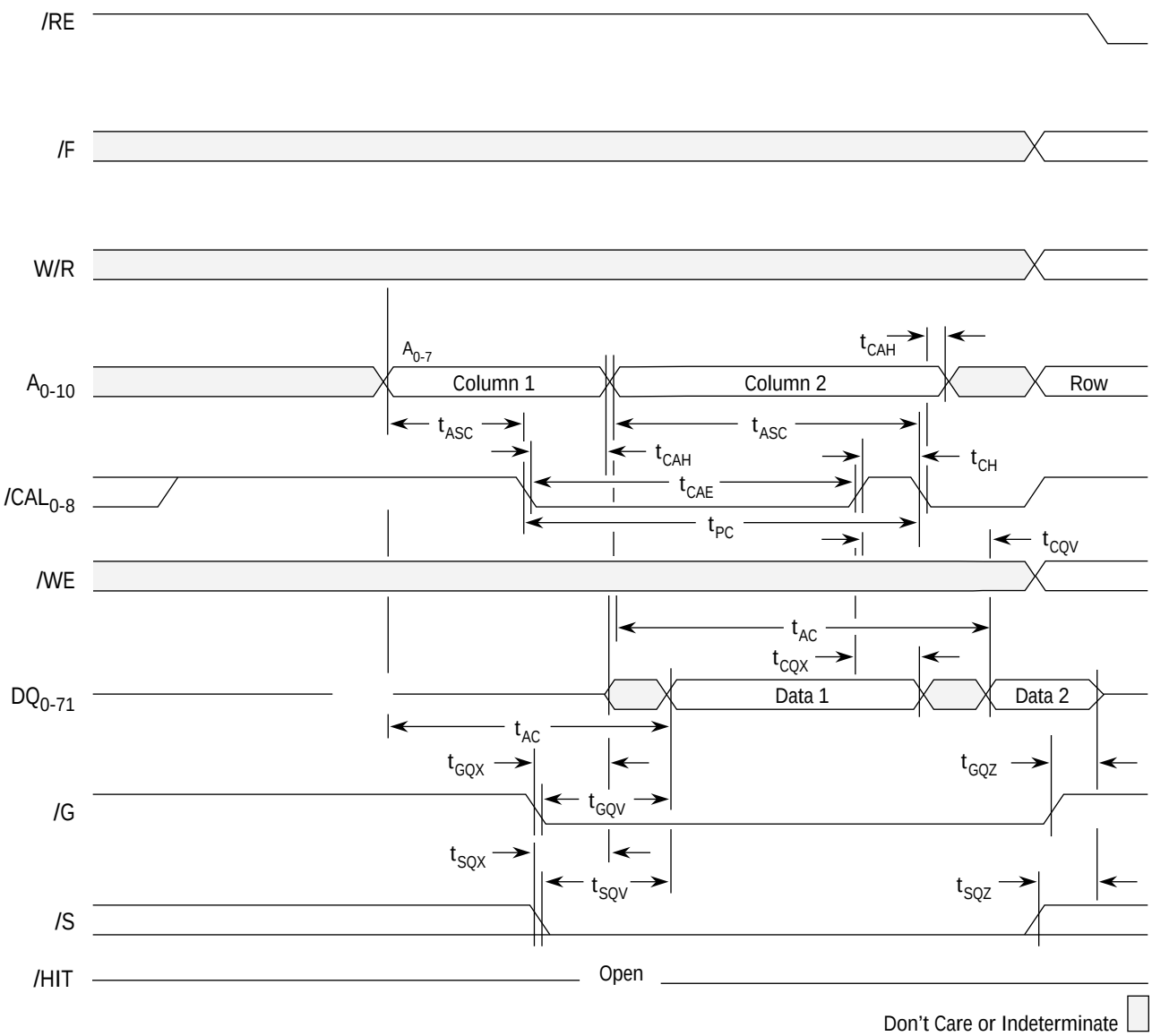
(1) V_{OUT} Timing Reference Point at 1.5V; (2) Parameter Defines Time When Output is Enabled (Sourcing or Sinking Current) and is Not Referenced to V_{OH} or V_{OL}; (3) Minimum Specification is Referenced from V_{IH} and Maximum Specification is Referenced from V_{IL} on Input Control Signal; (4) Parameter Defines Time When Output Achieves Open-Circuit Condition and is Not Referenced to V_{OH} or V_{OL}; (5) Minimum Specification is Referenced from V_{IL} and Maximum Specification is Referenced from V_{IH} on Input Control Signal; (6) On DM2213, t_{WHR} Minimum is t_{DS}

/RE Inactive Cache Read Hit (Static Column Mode)



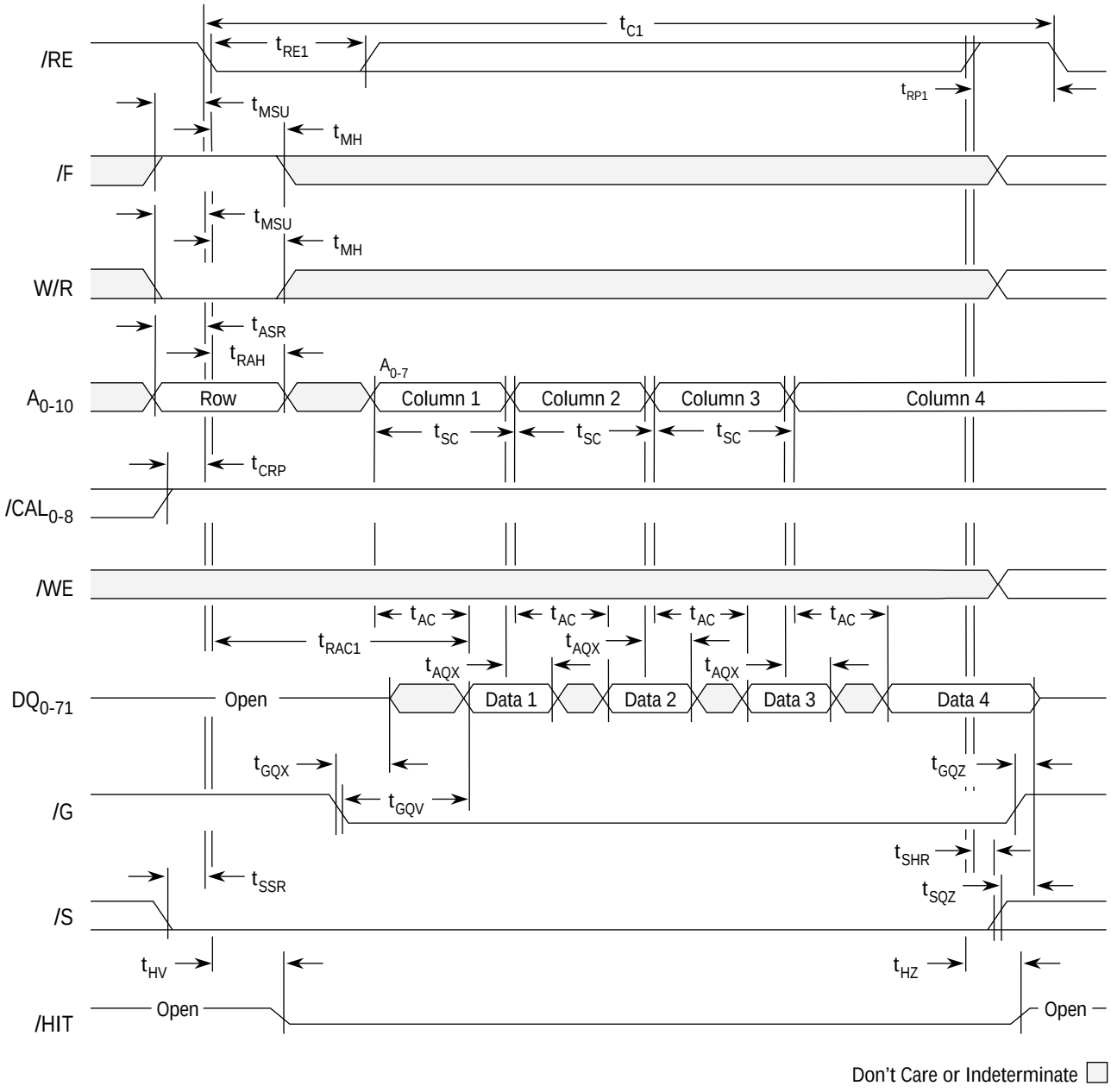
NOTES: 1. Data accessed during /RE inactive read is from the row address specified during the last /RE active read cycle.

/RE Inactive Cache Read Hit (Page Mode)



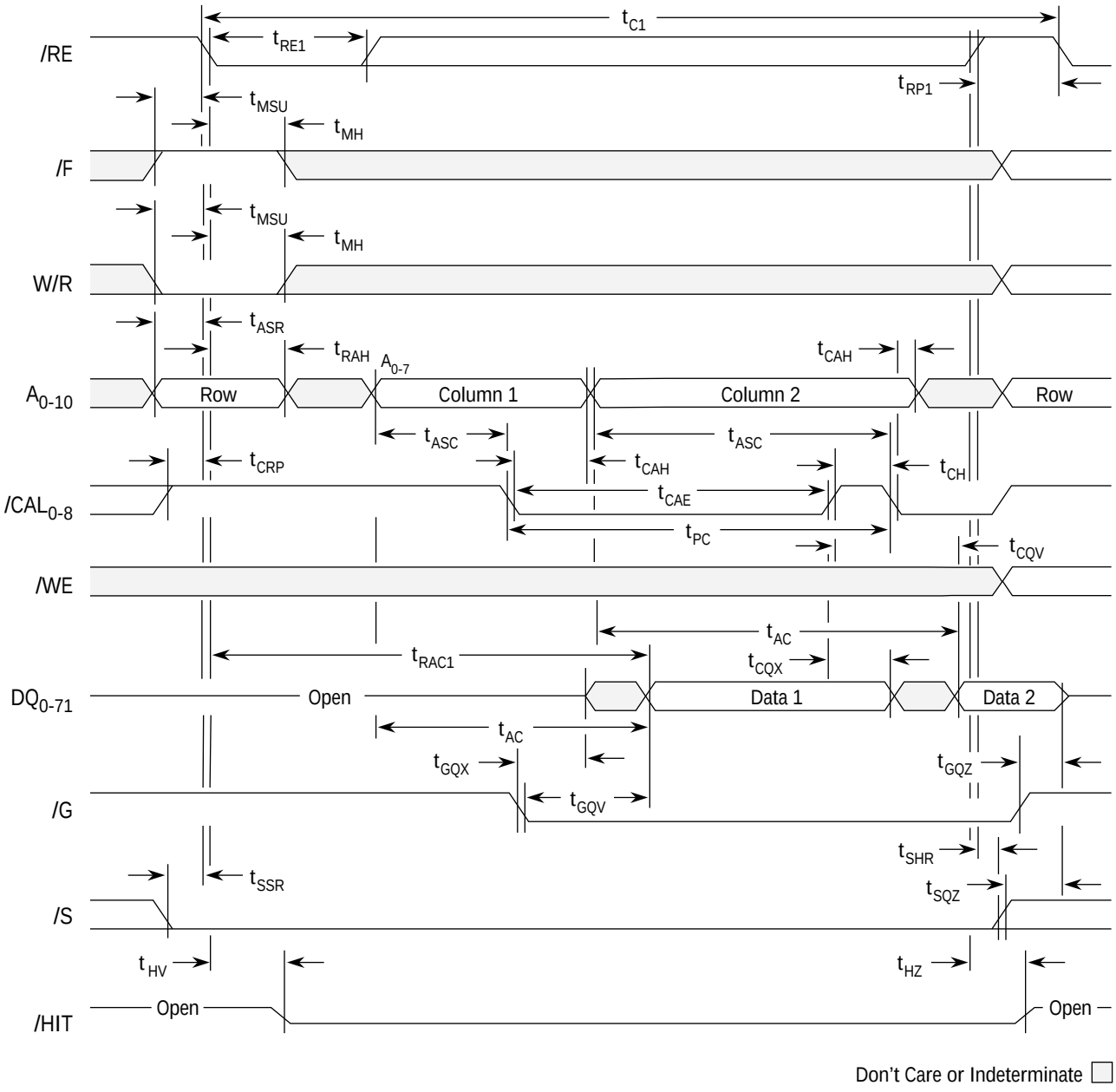
NOTES: 1. Data accessed during /RE inactive read is from the row address specified during the last /RE active read cycle.

/RE Active Cache Read Hit (Static Column Mode)

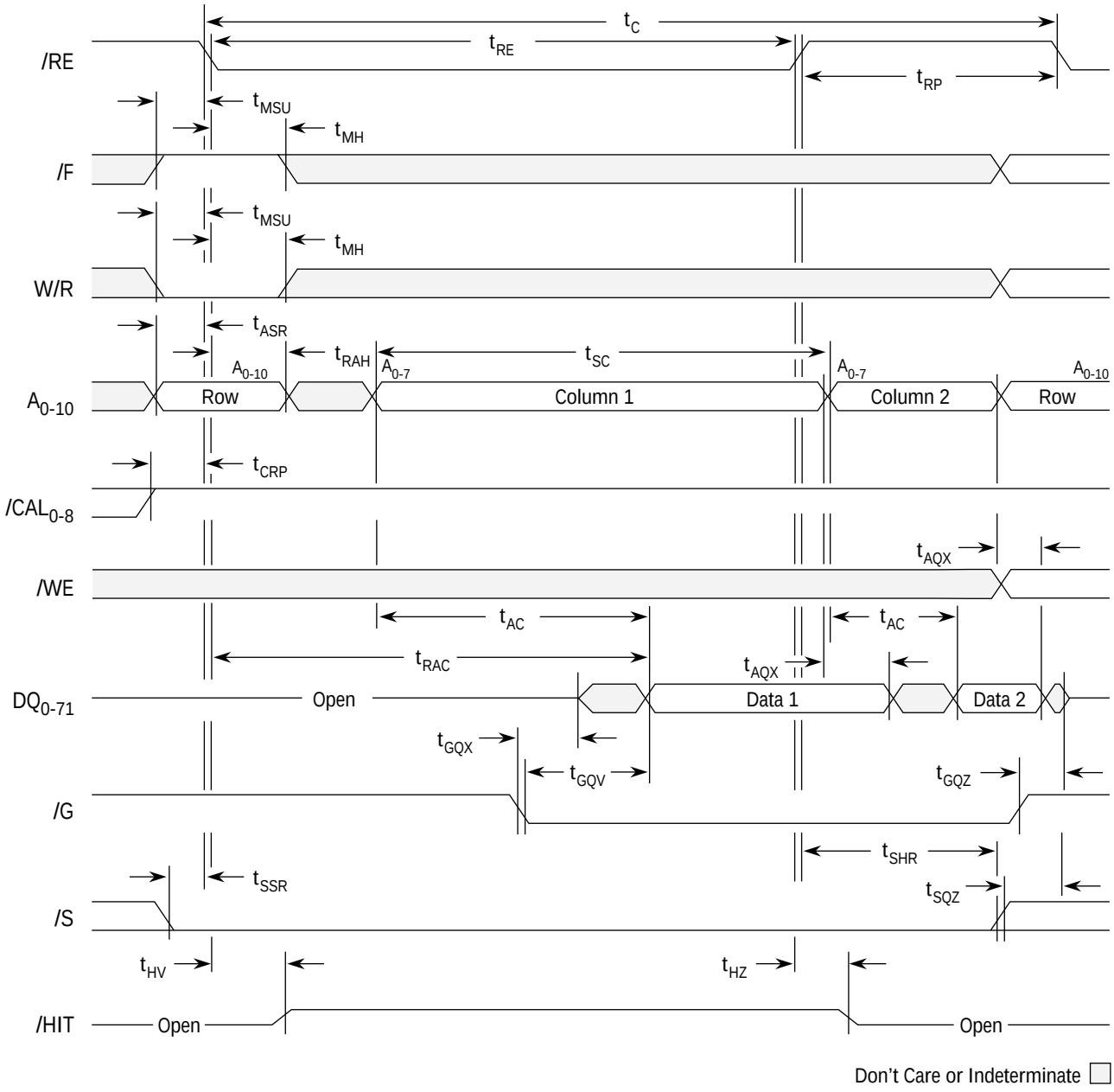


Don't Care or Indeterminate

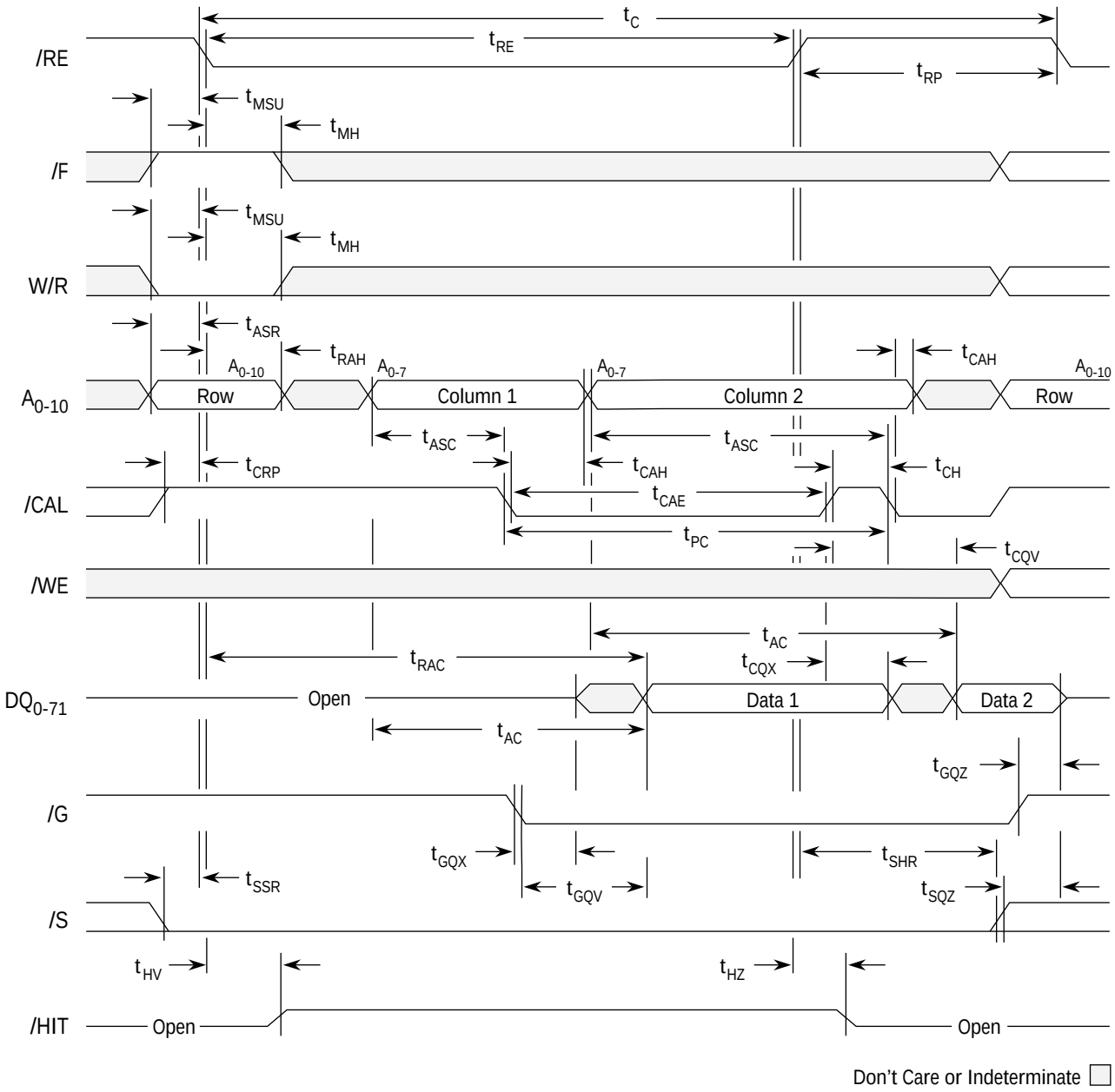
/RE Active Cache Read Hit (Page Mode)



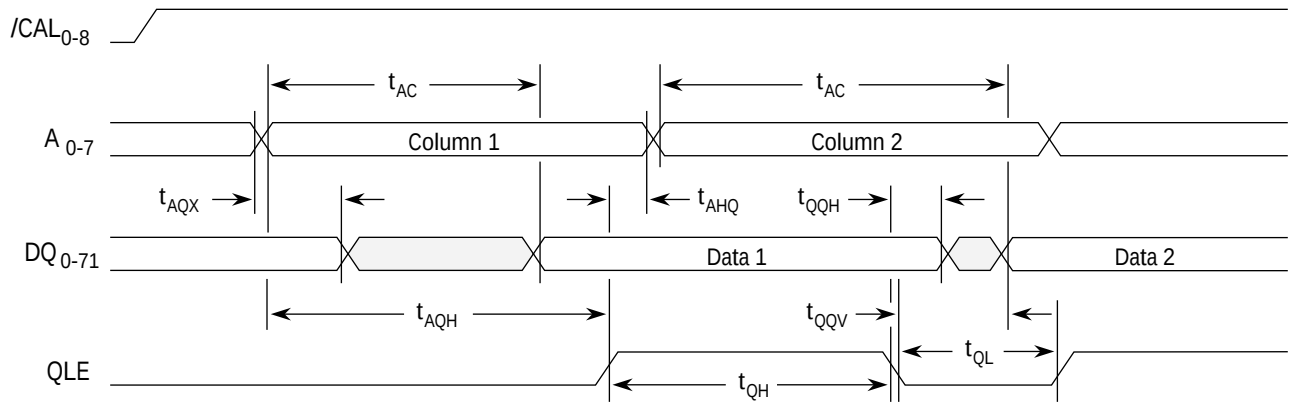
/RE Active Cache Read Miss (Static Column Mode)



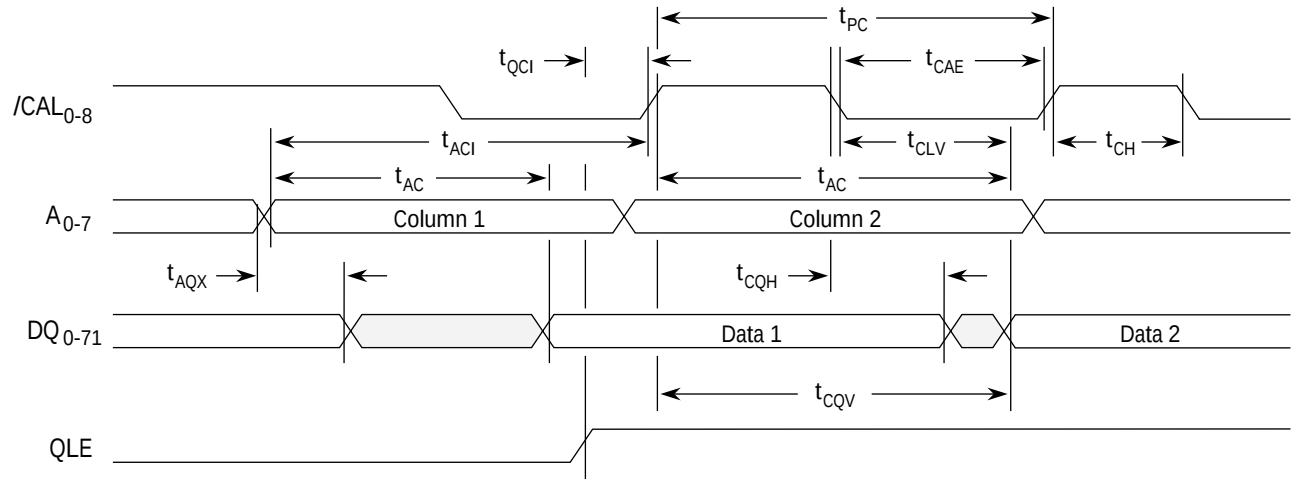
/RE Active Cache Read Miss (Page Mode)



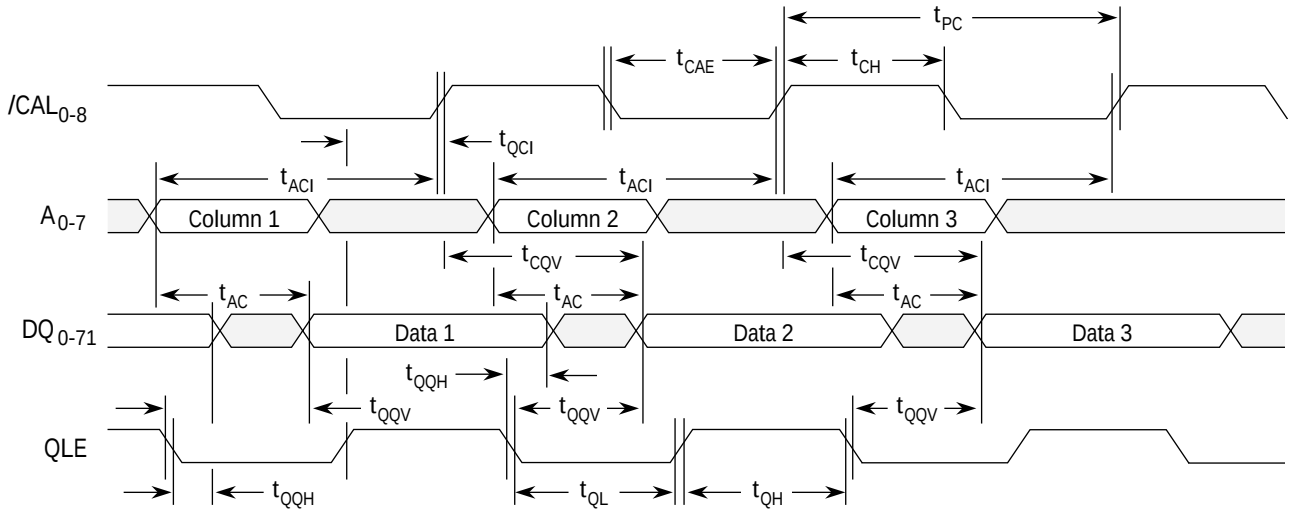
Output Latch Enable Operation (Static Column EDO Mode Read)



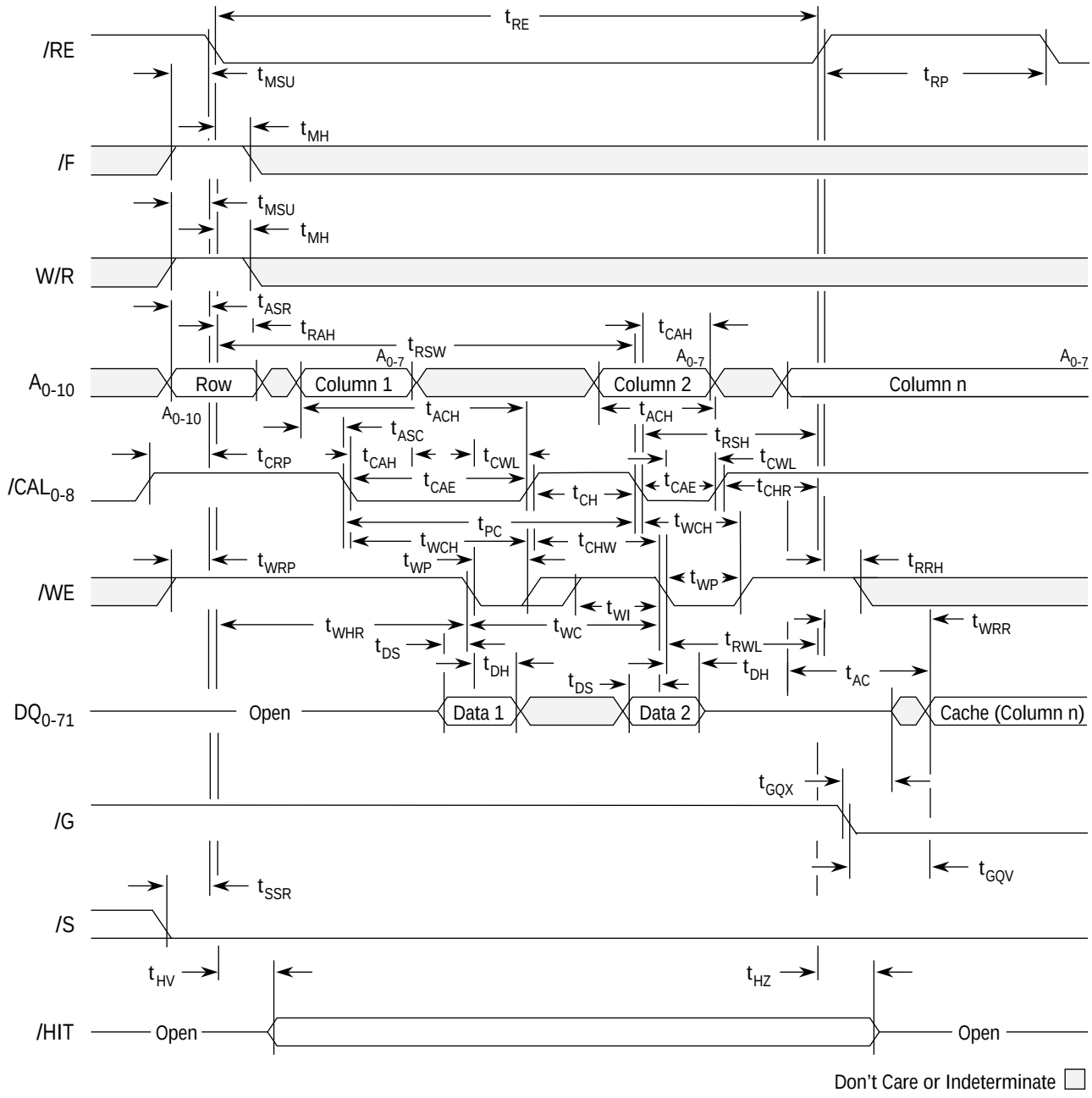
Output Latch Enable Operation (Page Mode EDO Read)



Output Latch Enable Operation (Asynchronous Access)

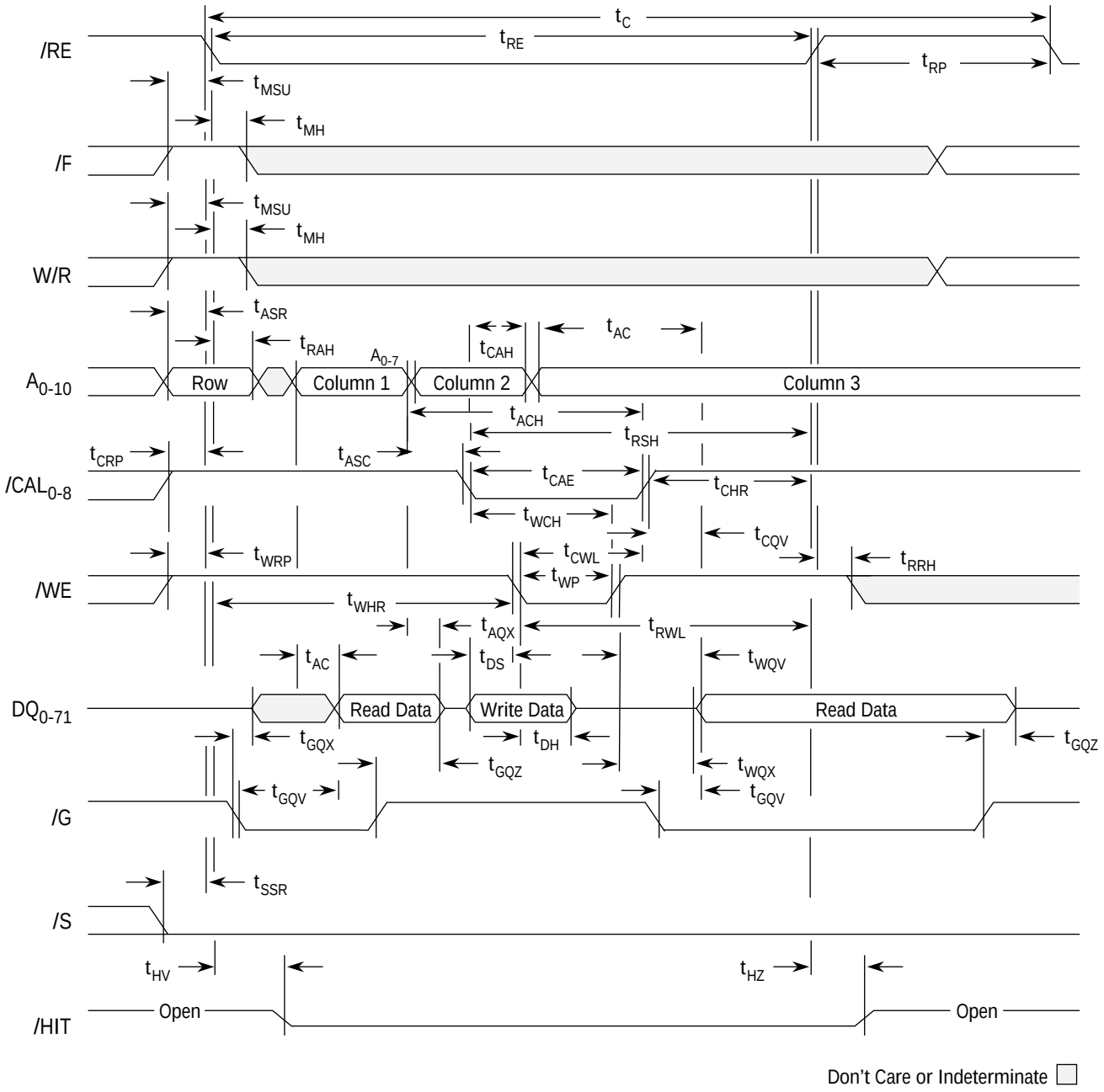


Burst Write (Hit or Miss) Followed By /RE Inactive Cache Reads



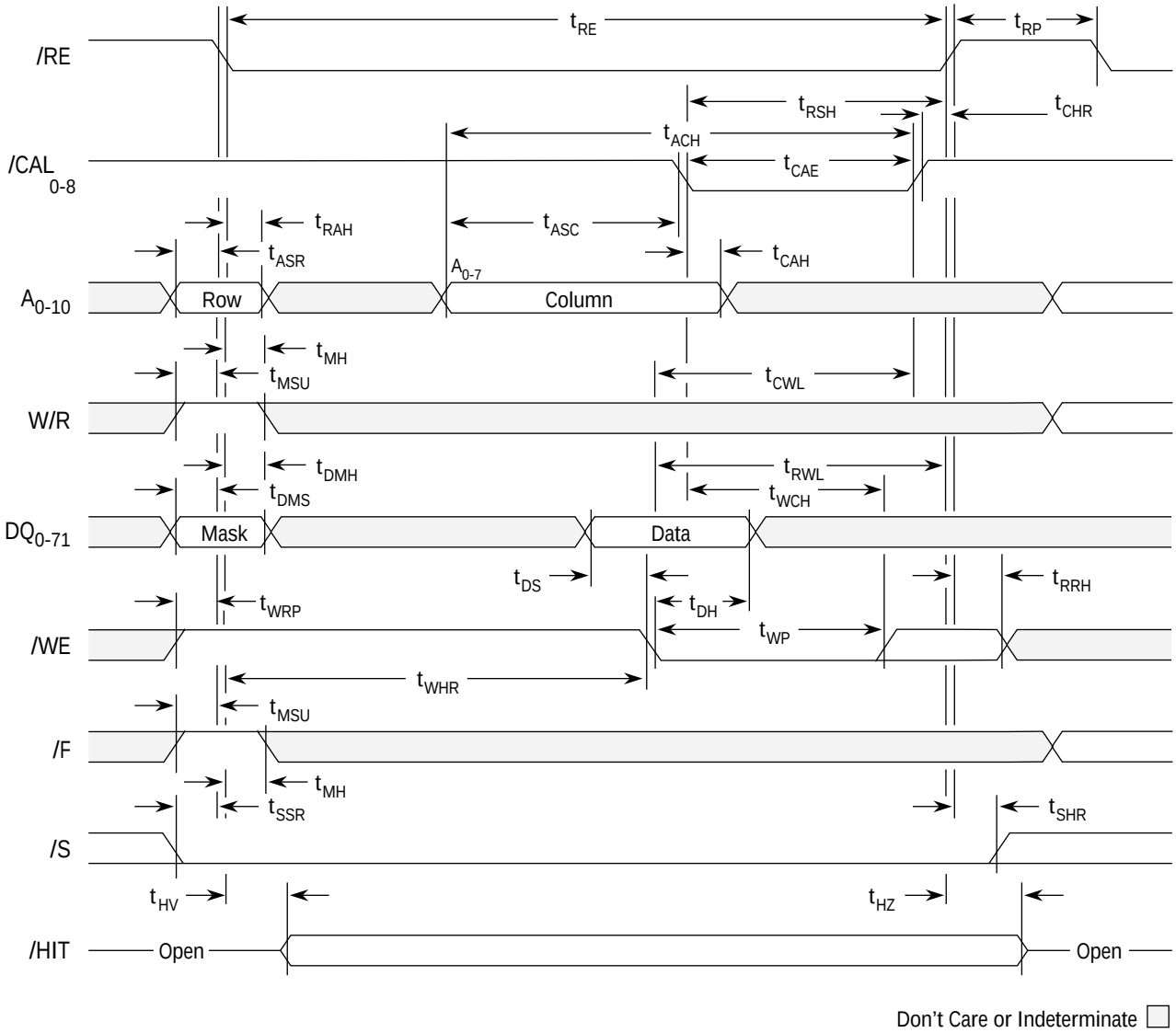
NOTES: 1. /G becomes a don't care after t_{RGX} during a write miss.

Read/Write During Write Hit Cycle (Can Include Read-Modify-Write)



NOTES: 1. If column address one equals column address two, then a read-modify-write cycle is performed.

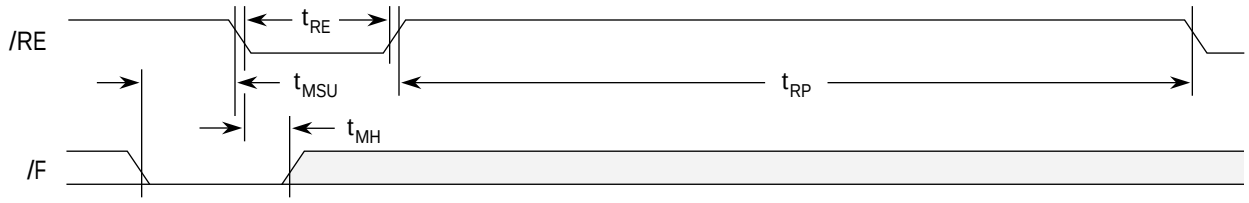
Write-Per-Bit Cycle (/G=High)



NOTES: 1. Data mask bit high (1) enables bit write; data mask bit low (0) inhibits bit write.

2. Write-per-bit cycle valid only for DM512K72DT6.

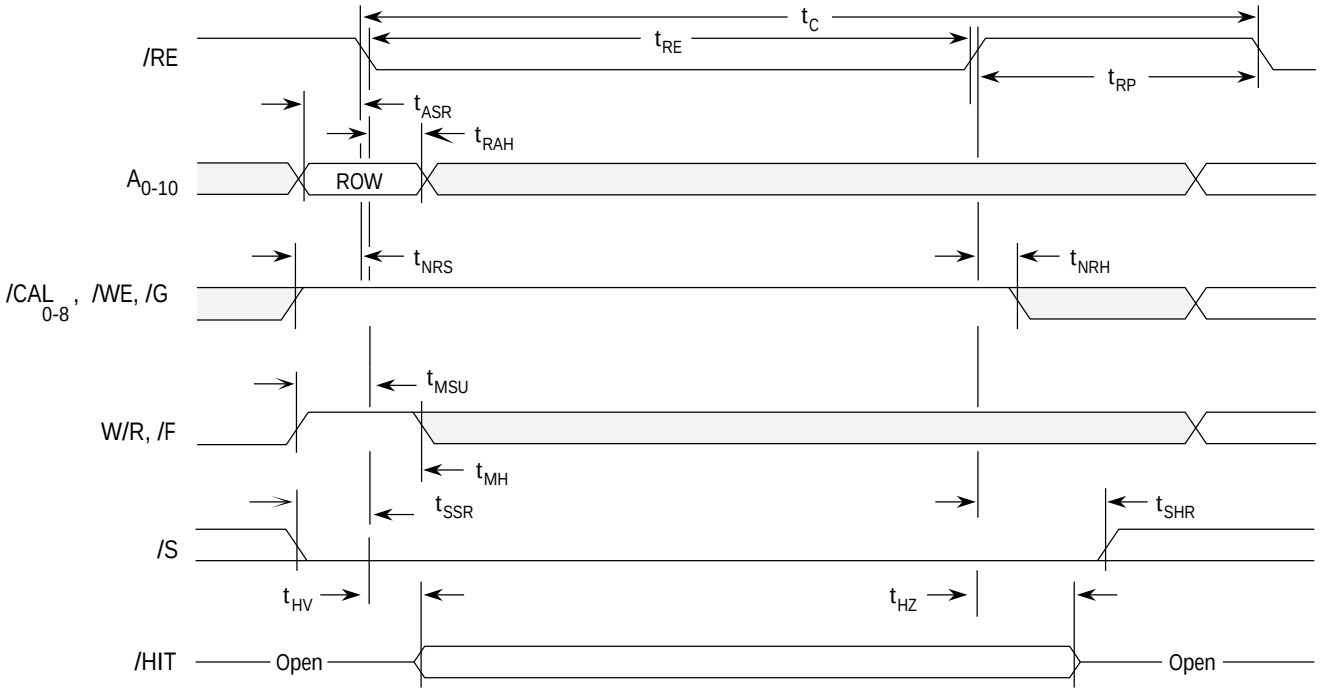
/F Refresh Cycle



Don't Care or Indeterminate ☐

NOTES: 1. During /F refresh cycles, the status of W/R, /WE, $A_{0\text{-}10}$, /CAL, /S, and /G is a don't care.
2. /RE inactive cache reads may be performed in parallel with /F refresh cycles.

/RE-Only Refresh

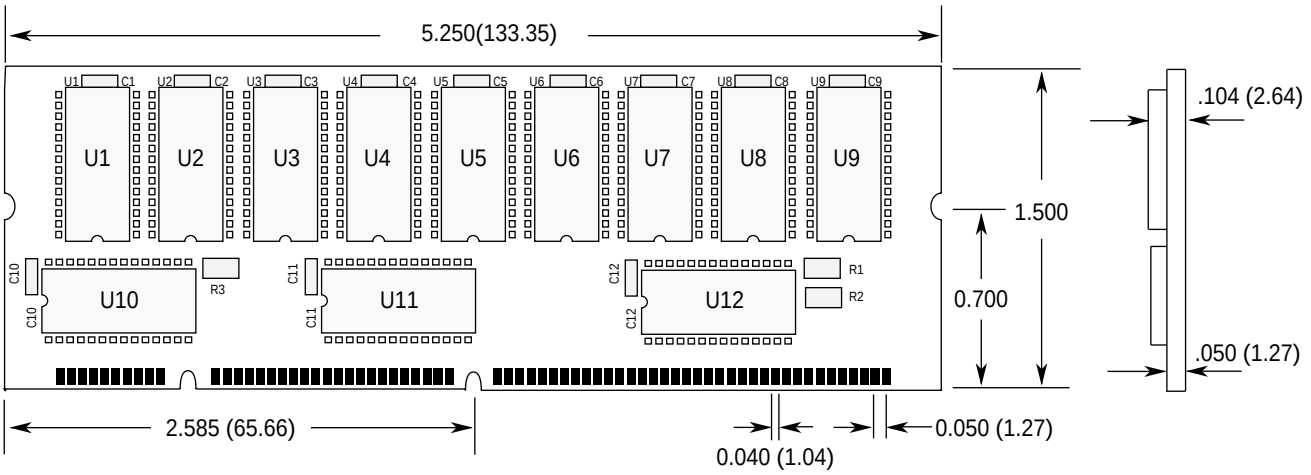


Don't Care or Indeterminate ☐

NOTES: 1. All binary combinations of $A_{0\text{-}9}$ must be refreshed every 64ms interval. A_{10} does not have to be cycled, but must remain valid during row address setup and hold times.
2. /RE refresh is write cycle with no /CAL active cycle.

Mechanical Data
168 Pin DIMM Module Configuration

Inches (mm)



U1-4, U6-9 — Enhanced DM2203T-xx, 512Kx8 EDRAM, 300 Mil TSOP
U5 — Enhanced DM2213T-xx, 512Kx8 EDRAM with Write-per-bit (not present on DM512K64DT)
U10-12 — IDT 74FCT162344ETPA Address/Clock Driver or Equivalent
C1-12 — 0.22µF Chip Capacitor
Socket — Robinson Nugent DIMS - 168BD5-TR or Equivalent

Part Numbering System

DM512K72DT 6- 12 N

Error Check Mode (72-bit Only)
Blank - Write-per-bit Parity
N - ECC (No Write-per-bit)

Access Time from Cache in Nanoseconds
12ns
15ns

Packaging System
T = 300 Mil, Plastic TSOP - II

Memory Module Configuration
D= DIMM

I/O Width
64 = 64 Bits
72 = 72 Bits

Memory Depth
512K
1M

Dynamic Memory