Enhanced Memory Systems Inc.

DM512K32ST/DM512K36ST
512Kb x 32/512Kb x 36 EDRAM SIMM

Product Specification

Features

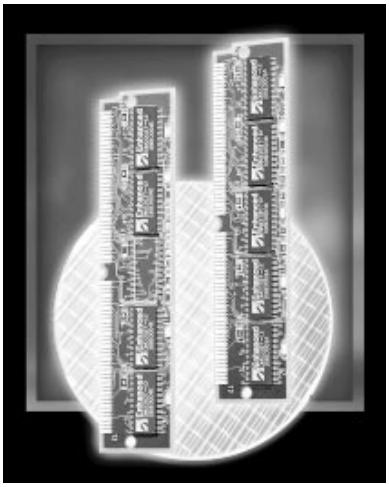
- 4KByte SRAM Cache Memory for 12ns Random Reads Within Four Actives Pages (Multibank Cache)
- Fast DRAM Array for 30ns Access to Any New Page
- Write Posting Register for 12ns Random Writes and Burst Writes Within a Page (Hit or Miss)
- 1KByte Wide DRAM to SRAM Bus for 56.8 Gigabytes/Sec Cache Fill
- On-chip Cache Hit/Miss Comparators Maintain Cache Coherency on Writes
- Hidden Precharge and Refresh Cycles
- Extended 64ms Refresh Period for Low Standby Power
- Standard CMOS/TTL Compatible I/O Levels and +5 Volt Supply
- Compatibility with JEDEC 512K x 32/36 DRAM SIMM Configuration Allows Performance Upgrade in System
- Industrial Temperature Range Option

Description

The Enhanced Memory Systems 2MB EDRAM SIMM module provides a single memory module solution for the main memory or local memory of fast embedded control, DSP, and other high performance systems. Due to its fast 12ns cache row register, the EDRAM memory module supports zero-wait-state burst read operations at up to 50MHz bus rates in a non-interleave configuration and 100MHz bus rates with a two-way interleave configuration.

On-chip write posting and fast page mode operation supports 12ns write and burst write operations. On a cache miss, the fast DRAM array reloads the entire 1KByte cache over a 1KByte-wide bus in 18ns for an effective bandwidth of 56.8 Gbytes/sec. This means very low latency and fewer wait states on a cache miss than a non-integrated cache/DRAM solution. The JEDEC compatible 72-bit SIMM configuration allows a single memory controller to be designed to support either JEDEC slow DRAMs or high speed EDRAMs to provide a simple upgrade path to higher system performance.

Architecture



The DM512K36ST achieves 512K x 36 density by mounting five 512K x 8 EDRAMs, packaged in 44-pin plastic TSOP-II packages, on a multi-layer substrate. Four 2203 devices and one DM2213 device provide data and parity storage. The DM512K32 contains four 2203 devices for data only.

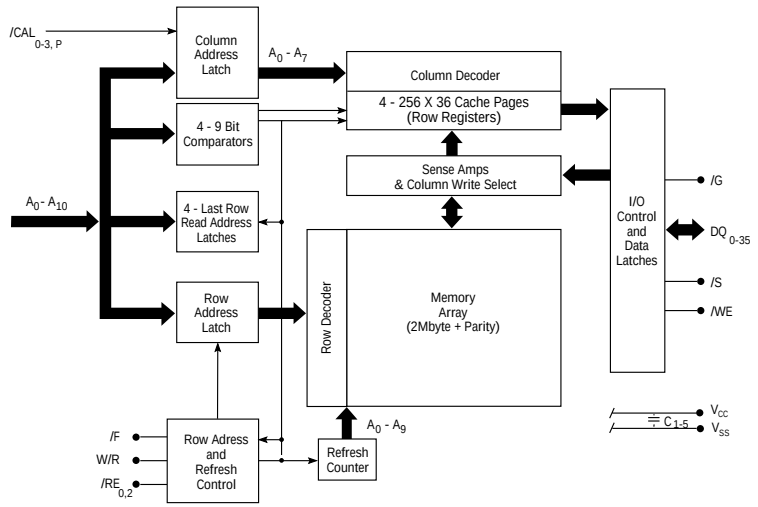
The EDRAM memory module architecture is very similar to a standard 2MB DRAM module with the addition of an integrated cache and on-chip control which allows it to operate much like a page mode or static column DRAM.

The EDRAM's SRAM cache is integrated into the DRAM array as tightly coupled row registers. The 512K x 32/36 EDRAM SIMM has a total of four independent DRAM memory banks each with its own 256 x 32/36 SRAM row register. Memory reads always occur from the cache row register of one of these banks as specified by row address bits A_8 and A_9 (bank select). When the internal comparator detects that the row address matches the last row read from any of the four DRAM banks (page hit), the SRAM is accessed and data is available on the output pins in 12ns from column address input. Subsequent reads within the page (burst reads or random reads) can continue at 12ns cycle time. When the row address does not match the last row read from any of the four DRAM banks (page miss), the new DRAM row is accessed and loaded into the appropriate SRAM row register and data is available on the output pins all within 30ns from row enable. Subsequent reads within the page (burst reads or random reads) can continue at 12ns cycle time.

Since reads occur from the SRAM cache, the DRAM precharge can occur during burst reads. This eliminates the precharge time delay suffered by other DRAMs and SDRAMs when accessing a new page. The EDRAM has an independent on-chip refresh counter and dedicated refresh control pin to allow the DRAM array to be refreshed concurrently with cache read operations (hidden refresh).

During EDRAM read accesses, data can be accessed in either static column

Functional Diagram



or page mode depending upon the operation of the /CAL input. If /CAL is held high, new data is accessed with each new column address (static column mode). If /CAL is brought low during a read access, the column address is latched and new data will not be accessed until both the column address is changed and /CAL is brought high (page mode). A dedicated output enable (/G) with 5ns access time allows high speed two-way interleave without an external multiplexer.

Memory writes are posted to the input data latch and directed to the DRAM array. During a write hit, the on-chip address comparator activates a parallel write path to the SRAM cache to maintain coherency. Random or page mode writes can be posted 5ns after column address and data are available. The EDRAM allows 12ns page mode cycle time for both write hits and write misses. Memory writes do not affect the contents of the cache row register except during a cache hit. Since the DRAM array can be written to at SRAM speeds, there is no need for complex writeback schemes.

By integrating the SRAM cache as row registers in the DRAM array and keeping the on-chip control simple, the EDRAM is able to provide superior performance over standard slow 4Mb DRAMs. By eliminating the need for SRAMs and cache controllers, system cost, board space, and power can all be reduced.

Functional Description

The EDRAM is designed to provide optimum memory performance with high speed microprocessors. As a result, it is possible to perform simultaneous operations to the DRAM and SRAM cache sections of the EDRAM. This feature allows the EDRAM to hide precharge and refresh operation during reads and maximize hit rate by maintaining page cache contents during write operations even if data is written to another memory page. These capabilities, in conjunction with the faster basic DRAM and cache speeds of the EDRAM, minimize processor wait states.

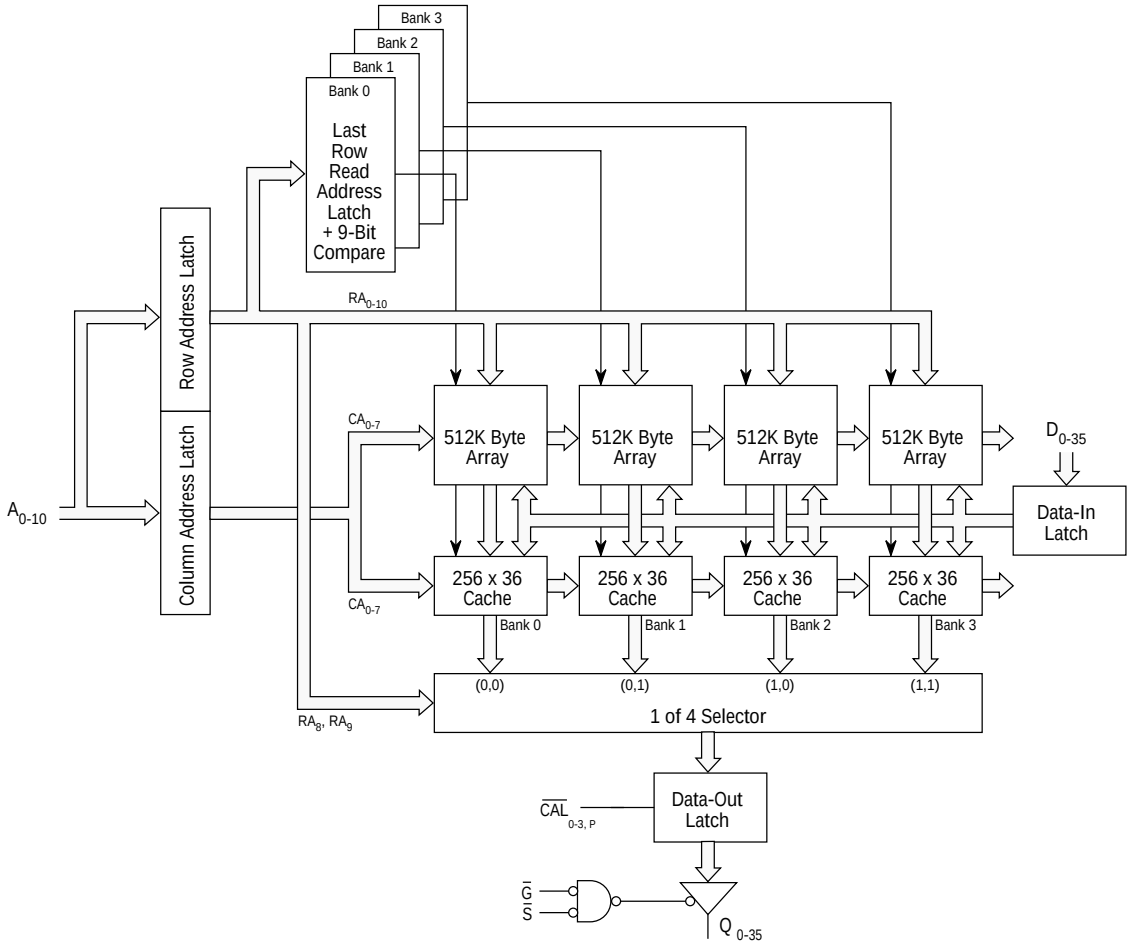
EDRAM Basic Operating Modes

The EDRAM operating modes are specified in the table to follow.

Hit and Miss Terminology

In this datasheet, “hit” and “miss” always refer to a hit or miss to any of the four pages of data contained in the SRAM cache row

Four Bank Cache Architecture



registers. There are four cache row registers, one for each of the four banks of DRAM. These registers are specified by the bank select row address bits A_8 and A_9. The contents of these cache row registers is always equal to the last row that was read from each of the four internal DRAM banks (as modified by any write hit data).

DRAM Read Hit

A DRAM read request is initiated by clocking /RE with W/R low and /F high. The EDRAM will compare the new row address to the last row read address latch for the bank specified by row address bits $A_{8\text{-}9}$ (LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address matches the LRR, the requested data is already in the SRAM cache and no DRAM memory reference is initiated. The data specified by the row and column address is available at the output pins at the greater of times t_{AC} or t_{GQV}. Since no DRAM activity is initiated, /RE can be brought high after time t_{RE1}, and a shorter precharge time, t_{RP1}, is required. Additional locations within the currently active page may be accessed concurrently with precharge by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address change in static column mode. During any read cycle, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address. In page mode, data valid time is determined by either t_{AC} or t_{CQV}.

DRAM Read Miss

A DRAM read request is initiated by clocking /RE with W/R low and /F high. The EDRAM will compare the new row address to the LRR address latch for the bank specified by row address bits $A_{8\text{-}9}$ (LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address does not match the LRR, the requested data is not in SRAM cache and a new row is fetched from the DRAM. The EDRAM will load the new row data into the SRAM cache and update the LRR latch. The data at the specified column address is available at the output pins at the greater of times t_{RAC}, t_{AC}, and t_{GQV}. /RE may be brought high after time t_{RE} since the new row data is safely latched into SRAM cache. This allows the EDRAM to precharge the DRAM array while data is accessed from SRAM cache. Additional locations within the currently active page may be accessed by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address change in static column mode. During any read cycle, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address. In page mode, data valid time is determined by either t_{AC} or t_{CQV}.

DRAM Write Hit

A DRAM write request is initiated by clocking /RE while W/R, /WE, and /F are high. The EDRAM will compare the new row address to the LRR address latch for the bank specified by row address bits $A_{8\text{-}9}$ (LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address matches the LRR, the EDRAM will write data to both the DRAM page in the appropriate bank and its corresponding SRAM cache simultaneously to maintain coherency. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE (t_{RAH} + t_{ASC} for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. With /G enabled and /WE disabled, read operations may be performed while /RE is activated in write hit mode. This allows read-modify-write, write-verify, or random read-write sequences within the page with 12ns cycle times. At the end of any write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. Cache reads can be performed concurrently with precharge (see "/RE Inactive Operation"). When /RE is inactive, the cache reads will occur from the page accessed during the last /RE active read cycle. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, the /CAL input can be used as a byte write select in multi-chip systems.

DRAM Write Miss

A DRAM write request is initiated by clocking /RE while W/R, /WE, and /F are high. The EDRAM will compare the new row address to the LRR address latch for the bank specified for row address bits $A_{8\text{-}9}$ (LRR: a 9-bit row address latch for each internal

EDRAM Basic Operating Modes

Function	/S	/RE	W/R	/F	$A_{0\text{-}10}$	Comment
Read Hit	L	↓	L	H	Row = LRR	No DRAM Reference, Data in Cache
Read Miss	L	↓	L	H	Row ≠ LRR	DRAM Row to Cache
Write Hit	L	↓	H	H	Row = LRR	Write to DRAM and Cache, Reads Enabled
Write Miss	L	↓	H	H	Row ≠ LRR	Write to DRAM, Cache Not Updated, Reads Disabled
Internal Refresh	X	↓	X	L	X	Cache Reads Enabled
Low Power Standby	H	H	X	X	X	Standby Current
Unallowed Mode	H	L	X	H	X	

H = High; L = Low; X = Don't Care; ↓ = High-to-Low Transition; LRR = Last Row Read

DRAM bank which is reloaded on each /RE active read miss cycle). If the row address does not match any of the LRRs, the EDRAM will write data to the DRAM page in the appropriate bank and the contents of the current cache is not modified. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE (t_{RAH} + t_{ASC} for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. During a write miss sequence cache reads are inhibited and the output buffers are disabled (independently of /G) until time t_{WRR} after /RE goes high. At the end of a write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. Cache reads can be performed concurrently with the precharge (see "/RE Inactive Operation"). When /RE is inactive, the cache reads will occur from the page accessed during the last /RE active read cycle. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, /CAL can be used as a byte write select in multi-chip systems.

/RE Inactive Operation

Data may be read from the SRAM cache without clocking /RE. This capability allows the EDRAM to perform cache read operations during precharge and refresh cycles to minimize wait states. It is only necessary to select /S and /G and provide the appropriate column address to read data as shown in the table below. In this mode of operation, the cache reads will occur from the page accessed during the last /RE active read cycle. To perform a cache read in static column mode, /CAL is held high, and the cache contents at the specified column address will be valid at time t_{AC} after address is stable. To perform a cache read in page mode, /CAL is clocked to latch the column address and data.

This option is desirable when the external control logic is capable of fast hit/miss comparison. In this case, the controller can avoid the time required to perform row/column multiplexing on hit cycles.

Function	/S	/G	/CAL	A_{0-7}
Cache Read (Static Column)	L	L	H	Column Address
Cache Read (Page Mode)	L	L	↕	Column Address

H = High; L = Low; X = Don't Care; ↕ = Transitioning

Write-Per-Bit Operation

The DM512K36ST SIMM provides a write-per-bit capability to selectively modify individual parity bits ($DQ_{8, 17, 26, 35}$) for byte write operations. The parity device (DM2213) is selected via $/CAL_P$. Byte write selection to non-parity bits is accomplished via CAL_{0-3}. The bits to be written are determined by a bit mask data word which is placed on the parity I/O data pins prior to clocking /RE. The logic one bits in the mask data select the bits to be written. As soon as the mask is latched by /RE, the mask data is removed and write data can be placed on the databus. The mask is only specified on the /RE transition. During page mode write operations, the same mask is used for all write operations.

Internal Refresh

If /F is active (low) on the assertion of /RE, an internal refresh cycle is executed. This cycle refreshes the row address supplied by an internal refresh counter. This counter is incremented at the end of the cycle in preparation for the next /F refresh cycle. At least 1,024 /F cycles must be executed every 64ms. /F refresh cycles can be hidden because cache memory can be read under column address control throughout the entire /F cycle. /F cycles are the only active cycles where /S can be disabled.

/RE Only Refresh Operation

Although /F refresh using the internal refresh counter is the recommended method of EDRAM refresh, it is possible to perform an /RE only refresh using an externally supplied row address. /RE refresh is performed by executing a *write cycle* (W/R and /F are high) where /CAL is not clocked. This is necessary so that the current cache contents and LRR are not modified by the refresh operation. All combinations of addresses A_{0-9} must be sequenced every 64ms refresh period. A_{10} does not need to be cycled. Read refresh cycles are not allowed because a DRAM refresh cycle does not occur when a read refresh address matches the LRR address latch.

Low Power Mode

The EDRAM enters its low power mode when /S is high. In this mode, the internal DRAM circuitry is powered down to reduce standby current.

Initialization Cycles

A minimum of eight /RE active initialization cycles (read, write, or refresh) are required before normal operation is guaranteed. Following these start-up cycles, two read cycles to different row addresses must be performed for each of the four internal banks of DRAM to initialize the internal cache logic. Row address bits A_8 and A_9. define the four internal DRAM banks.

Unallowed Mode

Read, write, or /RE only refresh operations must not be initiated to unselected memory banks by clocking /RE when /S is high.

Reduced Pin Count Operation

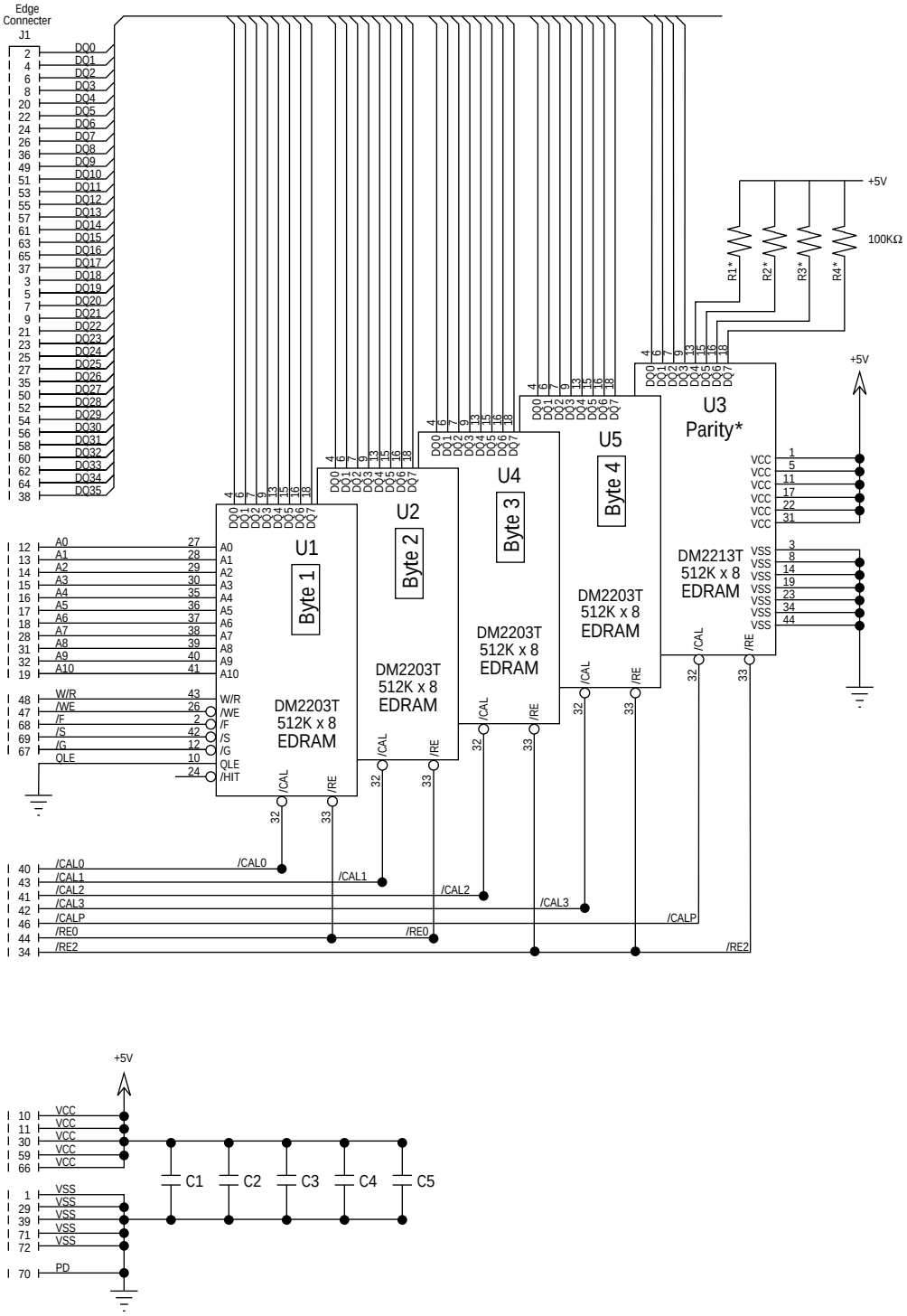
It is possible to simplify the interface to the 2MByte SIMM to reduce the number of control lines. $/RE_0$ and $/RE_2$ could be tied together externally to provide a single row enable. W/R and /G can be tied together if reads are not performed during write hit cycles. This external wiring simplifies the interface without any performance impact.

Pin Descriptions

$/RE_{0,2}$ — Row Enable

These inputs are used to initiate DRAM read and write operations and latch a row address and the states of W/R and /F. It is not necessary to clock /RE to read data from the EDRAM SRAM row registers. On read operations, /RE can be brought high as soon as data is loaded into cache to allow early precharge.

Interconnect Diagram



*DM2213 and R_{1-4} are not present on the DM512K32ST.

Pinout

Pin No.	*Function*	*Interconnect (Component Pin)*	*Organization*
1	GND	C (3, 8, 14, 19, 23, 34, 44)	Ground
2	DQ_0	U1 (4)	Byte 1 I/O 1
3	DQ_{18}	U4 (4)	Byte 3 I/O 1
4	DQ_1	U1 (6)	Byte 1 I/O 2
5	DQ_{19}	U4 (6)	Byte 3 I/O 2
6	DQ_2	U1 (7)	Byte 1 I/O 3
7	DQ_{20}	U4 (7)	Byte 3 I/O 3
8	DQ_3	U1 (9)	Byte 1 I/O 4
9	DQ_{21}	U4 (9)	Byte 3 I/O 4
10	+5 Volts	C (1, 5,11, 17, 22, 31)	V_{CC}
11	+5 Volts	C (1, 5, 11, 17, 22, 31)	V_{CC}
12	A_0	C (27)	Address
13	A_1	C (28)	Address
14	A_2	C (29)	Address
15	A_3	C (30)	Address
16	A_4	C (35)	Address
17	A_5	C (36)	Address
18	A_6	C (37)	Address
19	A_{10}	C (41)	Address
20	DQ_4	U1 (13)	Byte 1 I/O 5
21	DQ_{22}	U4 (13)	Byte 3 I/O 5
22	DQ_5	U1 (15)	Byte 1 I/O 6
23	DQ_{23}	U4 (15)	Byte 3 I/O 6
24	DQ_6	U1 (16)	Byte 1 I/O 7
25	DQ_{24}	U4 (164	Byte 3 I/O 7
26	DQ_7	U1 (18)	Byte 1 I/O 8
27	DQ_{25}	U4 (18)	Byte 3 I/O 8
28	A_7	C (38)	Address
29	GND	C (3, 8, 14, 19, 23, 34, 44)	Ground
30	+5 Volts	C (1, 5, 11, 17, 22, 31)	V_{CC}
31	A_8	C (39)	Address
32	A_9	C (40)	Address
33	NC		Reserved for 2Mb x 36
34	$/RE_2$	U3, 4, 5 (33)	Row Enable (Bytes 3,4, Parity)
35	DQ_{26}*	U3 (7)	Parity I/O for Byte 3
36	DQ_8*	U3 (4)	Parity I/O for Byte 1

Pin No.	*Function*	*Interconnect (Component Pin)*	*Organization*
37	DQ_{17}*	U3 (6)	Parity I/O for Byte 2
38	DQ_{35}*	U3 (9)	Parity I/O for Byte 4
39	GND	C (3, 8, 14, 19, 23, 34, 44)	Ground
40	$/CAL_0$	U1 (32)	Byte 1 Column Address Latch
41	$/CAL_2$	U4 (32)	Byte 3 Column Address Latch
42	$/CAL_3$	U5 (32)	Byte 4 Column Address Latch
43	$/CAL_1$	U2 (32)	Byte 2 Column Address Latch
44	$/RE_0$	U1, 2 (33)	Row Enable (Bytes 1,2)
45	NC		Reserved for 2Mb x 36
46	$/CAL_P$*	U3 (32)	Parity Column Address Latch
47	/WE	C (26)	Write Enable
48	W/R	C (43)	W/R Mode Control
49	DQ_9	U2 (4)	Byte 2 I/O 1
50	DQ_{27}	U5 (4)	Byte 4 I/O 1
51	DQ_{10}	U2 (6)	Byte 2 I/O 2
52	DQ_{28}	U5 (6)	Byte 4 I/O 2
53	DQ_{11}	U2 (7)	Byte 2 I/O 3
54	DQ_{29}	U5 (7)	Byte 4 I/O 3
55	DQ_{12}	U2 (9)	Byte 2 I/O 4
56	DQ_{30}	U5 (9)	Byte 4 I/O 4
57	DQ_{13}	U2 (13)	Byte 2 I/O 5
58	DQ_{31}	U5 (13)	Byte 4 I/O 5
59	+5 Volts	C (1, 5, 11, 17, 22, 31)	V_{CC}
60	DQ_{32}	U5 (15)	Byte 4 I/O 6
61	DQ_{14}	U2 (15)	Byte 2 I/O 6
62	DQ_{33}	U5 (16)	Byte 4 I/O 7
63	DQ_{15}	U2 (16)	Byte 2 I/O 7
64	DQ_{34}	U5 (18)	Byte 4 I/O 8
65	DQ_{16}	U2 (18)	Byte 2 I/O 8
66	+5 Volts	C (1, 5, 11, 17, 22, 31)	V_{CC}
67	/G	C (12)	Output Enable
68	/F	C (2)	Refresh Mode Control
69	/S	C (42)	Chip Select
70	PD	Signal GND	Presence Detect
71	GND	C (3, 8, 14, 19, 23, 34, 44)	Ground
72	GND	C (3, 8, 14, 19 33, 34, 44)	Ground

C = Common to All Memory Chips, U1 = Chip 1, etc.

*No Connect for DM512K32ST

/CAL $_{0-3, P}$ — Column Address Latch

These inputs are used to latch the column address and in combination with /WE to trigger write operations. When /CAL is high, the column address latch is transparent. When /CAL is low, the column address is closed and the output of the latch contains the address present while /CAL was high. /CAL can be toggled when /RE is low or high. However, /CAL must be high during the high-to-low transition of /RE except for /F refresh cycles.

W/R — Write/Read

This input along with /F specifies the type of DRAM operation initiated on the low going edge of /RE. When /F is high, W/R specifies either a write (logic high) or read operation (logic low).

/F — Refresh

This input will initiate a DRAM refresh operation using the internal refresh counter as an address source when /F is low on the low going edge of /RE.

/WE — Write Enable

This input controls the latching of write data on the input data pins. A write operation is initiated when both /CAL and /WE are low.

/G — Output Enable

This input controls the gating of read data to the output data pins during read operations.

/S — Chip Select

This input is used to power up the I/O and clock circuitry. When /S is high, the EDRAM remains in its low power mode. /S must remain active throughout any read or write operation. With the exception of /F refresh cycles, /RE should never be clocked when /S is inactive.

DQ_{0-35} — Data Input/Output

These bidirectional data pins are used to read and write data to the EDRAM. On the DM512K36 SIMM, the parity pins are also used to specify the bit mask used during parity write operations.

A_{0-10} — Multiplex Address

These inputs are used to specify the row and column addresses of the EDRAM data. The 11-bit row address is latched on the falling edge of /RE. The 8-bit column address can be specified at any other time to select read data from the SRAM cache or to specify the write column address during write cycles.

V_{CC} Power Supply

These inputs are connected to the +5 volt power supply.

V_{SS} Ground

These inputs are connected to the power supply ground connection.

Absolute Maximum Ratings

(Beyond Which Permanent Damage Could Result)

Description	Ratings
Input Voltage (V_{IN})	- 1 ~ 7v
Output Voltage (V_{OUT})	- 1 ~ 7v
Power Supply Voltage (V_{CC})	- 1 ~ 7v
Ambient Operating Temperature (T_A)	-40 ~ 85°C
Storage Temperature (T_S)	-55 ~ 150°C
Static Discharge Voltage (Per MIL-STD-883 Method 3015)	Class 1
Short Circuit O/P Current (I_{OUT})	50mA*

* One output at a time per device; short duration

Capacitance

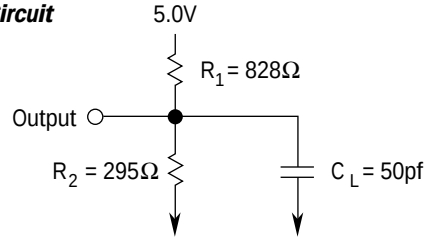
Description	Max*	Pins
Input Capacitance	22/24pf	A_{0-10}
Input Capacitance	16pf	$/RE_0$
Input Capacitance	14/18pf	$/RE_2$
Input Capacitance	17pf	/G
I/O Capacitance	9pf	DQ_{0-35}
Input Capacitance	10pf	$/CAL_{0-3, P}$
Input Capacitance	24/27pf	W/R, /WE, /F, /S

* DM512K32ST/DM512K36ST, respectively

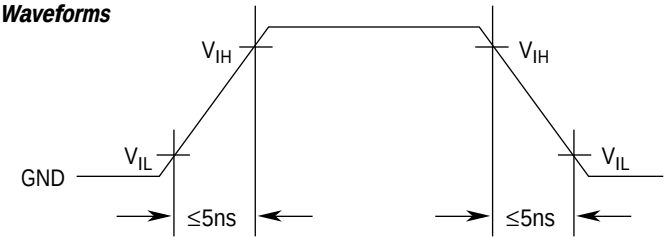
AC Test Load and Waveforms

V_{IN} Timing Reference Point at V_{IL} and V_{IH}
V_{OUT} Timing Referenced to 1.5 Volts

Load Circuit



Input Waveforms



Electrical Characteristics

(T_A = 0 to 70°C, Commercial; -40 to 85°C, Industrial)

Symbol	*Parameters*	*Min*	*Max*	*Test Conditions*
V_{CC}	Supply Voltage	4.75V	5.25V	All Voltages Referenced to V_{SS}
V_{IH}	Input High Voltage	2.4V	6.5V	
V_{IL}	Input Low Voltage	-1.0V	0.8V	
V_{OH}	Output High Level	2.4V	—	I_{OUT} = - 5mA
V_{OL}	Output Low Level	—	0.4V	I_{OUT} = 4.2mA
$I_{i(L)}$	Input Leakage Current	-50µA	50µA	$OV \le V_{IN} \le 6.5V$, All Other Pins Not Under Test = 0V
$I_{O(L)}$	Output Leakage Current	-50µA	50µA	$OV \le V_{IN}$, $OV \le V_{OUT} \le 5.5V$

Operating Current — DM512K32ST

Symbol	*Operating Current*	*33MHz Typ*(1)	*-12 Max*	*-15 Max*	*Test Condition*	*Notes*
I_{CC1}	Random Read	440mA	900mA	720mA	/RE, /CAL, /G and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC2}	Fast Page Mode Read	260mA	580mA	460mA	/CAL, /G and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC3}	Static Column Read	220mA	440mA	360mA	/G and Addresses Cycling: $t_{SC} = t_{SC}$ Minimum	2, 4
I_{CC4}	Random Write	540mA	760mA	600mA	/RE, /CAL, /WE and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC5}	Fast Page Mode Write	200mA	540mA	420mA	/CAL, /WE and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC6}	Standby	4mA	4mA	4mA	All Control Inputs Stable $\ge V_{CC}$ - 0.2V, Outputs Driven	
I_{CCT}	Average Typical Operating Current	120mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

Operating Current — DM512K36ST

Symbol	*Operating Current*	*33MHz Typ*(1)	*-12 Max*	*-15 Max*	*Test Condition*	*Notes*
I_{CC1}	Random Read	550mA	1125mA	900mA	/RE, /CAL, /G and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC2}	Fast Page Mode Read	325mA	725mA	575mA	/CAL, /G and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC3}	Static Column Read	275mA	550mA	450mA	/G and Addresses Cycling: $t_{SC} = t_{SC}$ Minimum	2, 4
I_{CC4}	Random Write	675mA	950mA	750mA	/RE, /CAL, /WE and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC5}	Fast Page Mode Write	250mA	675mA	525mA	/CAL, /WE and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC6}	Standby	5mA	5mA	5mA	All Control Inputs Stable $\ge V_{CC}$ - 0.2V, Outputs Driven	
I_{CCT}	Average Typical Operating Current	150mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

(1) "33MHz Typ" refers to worst case I_{CC} expected in a system operating with a 33MHz memory bus. See power applications note for further details. This parameter is not 100% tested or guaranteed.

(2) I_{CC} is dependent on cycle rates and is measured with CMOS levels and the outputs open.

(3) I_{CC} is measured with a maximum of one address change while /RE = V_{IL}.

(4) I_{CC} is measured with a maximum of one address change while /CAL = V_{IH}.

Switching Characteristics

(V_{CC} = 5V ± 5%, T_A = 0 to 70°C, Commercial; -40 to 85°C, Industrial; C_L = 50pF)

Symbol	*Description*	*-12*		*-15*		*Units*
		Min	*Max*	*Min*	*Max*	
t_{AC}(1)	Column Address Access Time		12		15	ns
t_{ACH}	Column Address Valid to /CAL Inactive (Write Cycle)	12		15		ns
t_{ACi}	Address Valid to /CAL Inactive	12		15		ns
t_{AQX}	Column Address Change to Output Data Invalid	5		5		ns
t_{ASC}	Column Address Setup Time	5		5		ns
t_{ASR}	Row Address Setup Time	5		5		ns
t_{C}	Row Enable Cycle Time	55		65		ns
t_{C1}	Row Enable Cycle Time, Cache Hit (Row=LRR), Read Cycle Only	20		25		ns
t_{CAE}	Column Address Latch Active Time	5		6		ns
t_{CAH}	Column Address Hold Time	0		0		ns
t_{CH}	Column Address Latch High Time (Latch Transparent)	5		5		ns
t_{CHR}	/CAL Inactive Lead Time to /RE Inactive (Write Cycles Only)	-2		-2		ns
t_{CHW}	Column Address Latch High to Write Enable Low (Multiple Writes)	0		0		ns
t_{CQV}	Column Address Latch High to Data Valid		15		15	ns
t_{CQX}	Column Address Latch Inactive to Data Invalid	5		5		ns
t_{CRP}	Column Address Latch Setup Time to Row Enable	5		5		ns
t_{CWL}	/WE Low to /CAL Inactive	5		5		ns
t_{DH}	Data Input Hold Time	0		0		ns
t_{DMH}	Mask Hold Time From Row Enable (Write-Per-Bit)	1		1.5		ns
t_{DMS}	Mask Setup Time to Row Enable (Write-Per-Bit)	5		5		ns
t_{DS}	Data Input Setup Time	5		5		ns
t_{GQV}(1)	Output Enable Access Time		5		5	ns
t_{GQX}(2,3)	Output Enable to Output Drive Time	0	5	0	5	ns
t_{GQZ}(4,5)	Output Turn-Off Delay From Output Disabled (/G↑)	0	5	0	5	ns
t_{MH}	/F and W/R Mode Select Hold Time	0		0		ns
t_{MSU}	/F and W/R Mode Select Setup Time	5		5		ns
t_{NRH}	/CAL, /G, and /WE Hold Time For /RE-Only Refresh	0		0		ns
t_{NRS}	/CAL, /G, and /WE Setup Time For /RE-Only Refresh	5		5		ns
t_{PC}	Column Address Latch Cycle Time	12		15		ns
t_{RAC}(1)	Row Enable Access Time, On a Cache Miss		30		35	ns
t_{RAC1}(1)	Row Enable Access Time, On a Cache Hit (Limit Becomes t_{AC})		15		17	ns
t_{RAC2}(1,6)	Row Enable Access Time for a Cache Write Hit		30		35	ns
t_{RAH}	Row Address Hold Time	1		1.5		ns
t_{RE}	Row Enable Active Time	30	100000	35	100000	ns

Switching Characteristics (continued)

(V_{CC} = 5V ± 5%, T_A = 0 to 70°C, Commercial; -40 to 85°C, Industrial; C_L = 50pF)

Symbol	Description	-12		-15		Units
		Min	Max	Min	Max	
t_{RE1}	Row Enable Active Time, Cache Hit (Row=LRR) Read Cycle	8		10		ns
t_{REF}	Refresh Period		64		64	ms
t_{RGX}	Output Enable Don't Care From Row Enable (Write, Cache Miss), O/P Hi Z	9		10		ns
t_{RQX1}(2,6)	Row Enable High to Output Turn-On After Write Miss	0	12	0	15	ns
t_{RP}(7)	Row Precharge Time	20		25		ns
t_{RP1}	Row Precharge Time, Cache Hit (Row=LRR) Read Cycle	8		10		ns
t_{RRH}	Read Hold Time From Row Enable (Write Only)	0		0		ns
t_{RSH}	Last Write Address Latch to End of Write	12		15		ns
t_{RSW}	Row Enable to Column Address Latch Low For Second Write	35		40		ns
t_{RWL}	Last Write Enable to End of Write	12		15		ns
t_{SC}	Column Address Cycle Time	12		15		ns
t_{SHR}	Select Hold From Row Enable	0		0		ns
t_{SQV}(1)	Chip Select Access Time		12		15	ns
t_{SQX}(2,3)	Output Turn-On From Select Low	0	12	0	15	ns
t_{SQZ}(4,5)	Output Turn-Off From Chip Select	0	8	0	10	ns
t_{SSR}	Select Setup Time to Row Enable	5		5		ns
t_T	Transition Time (Rise and Fall)	1	10	1	10	ns
t_{WC}	Write Enable Cycle Time	12		15		ns
t_{WCH}	Column Address Latch Low to Write Enable Inactive Time	5		5		ns
t_{WHR}(7)	Write Enable Hold After /RE	0		0		ns
t_{WI}	Write Enable Inactive Time	5		5		ns
t_{WP}	Write Enable Active Time	5		5		ns
t_{WQV}(1)	Data Valid From Write Enable High		12		15	ns
t_{WQX}(2,5)	Data Output Turn-On From Write Enable High	0	12	0	15	ns
t_{WQZ}(3,4)	Data Turn-Off From Write Enable Low	0	12	0	15	ns
t_{WRP}	Write Enable Setup Time to Row Enable	5		5		ns
t_{WRR}	Write to Read Recovery (Following Write Miss)		12		15	ns

(1) V_{OUT} Timing Reference Point at 1.5V

(2) Parameter Defines Time When Output is Enabled (Sourcing or Sinking Current) and is Not Referenced to V_{OH} or V_{OL}

(3) Minimum Specification is Referenced from V_{IH} and Maximum Specification is Referenced from V_{IL} on Input Control Signal

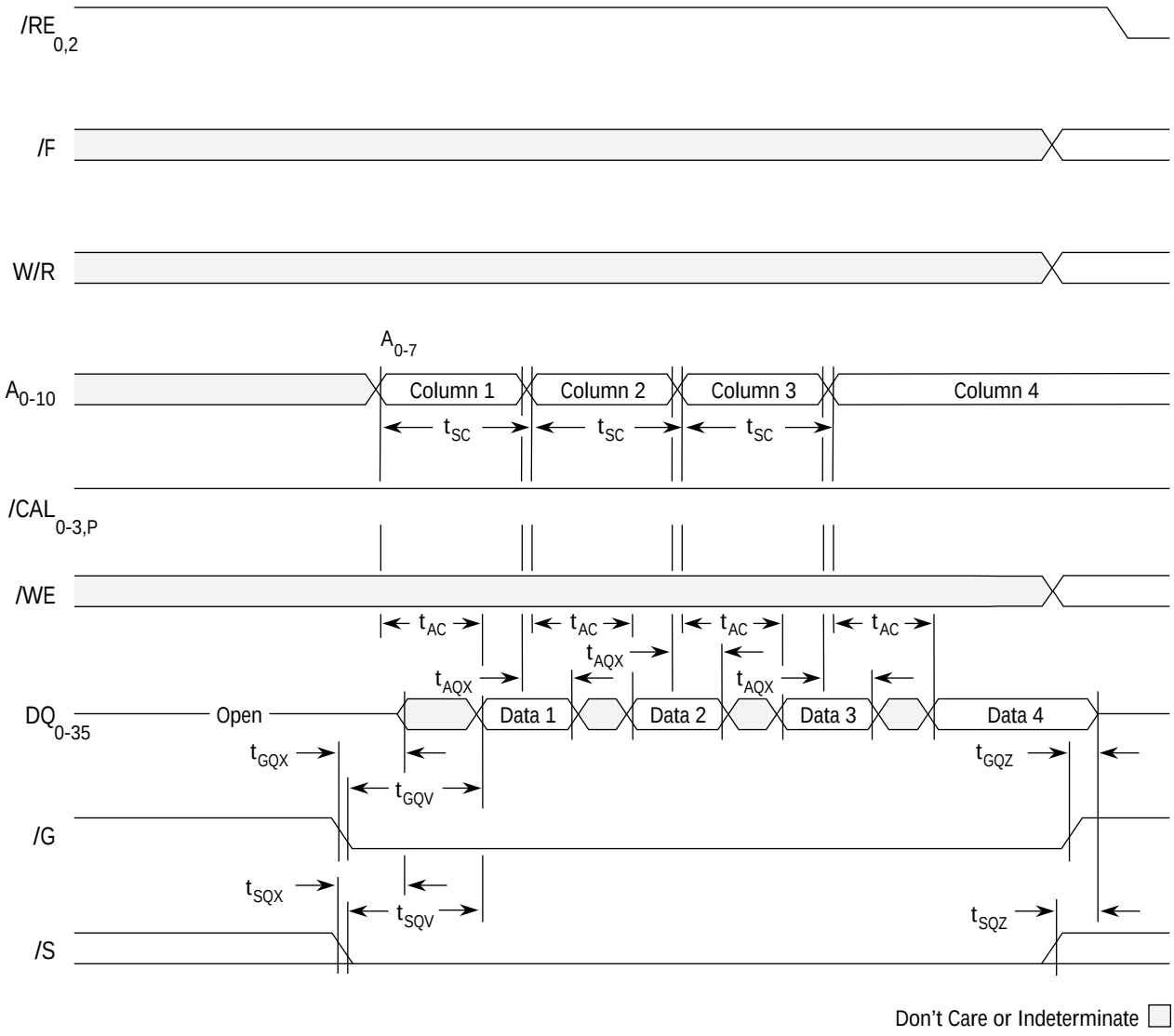
(4) Parameter Defines Time When Output Achieves Open-Circuit Condition and is Not Referenced to V_{OH} or V_{OL}

(5) Minimum Specification is Referenced from V_{IL} and Maximum Specification is Referenced from V_{IH} on Input Control Signal

(6) Access Parameter Applies When /CAL Has Not Been Asserted Prior to t_{RAC2}

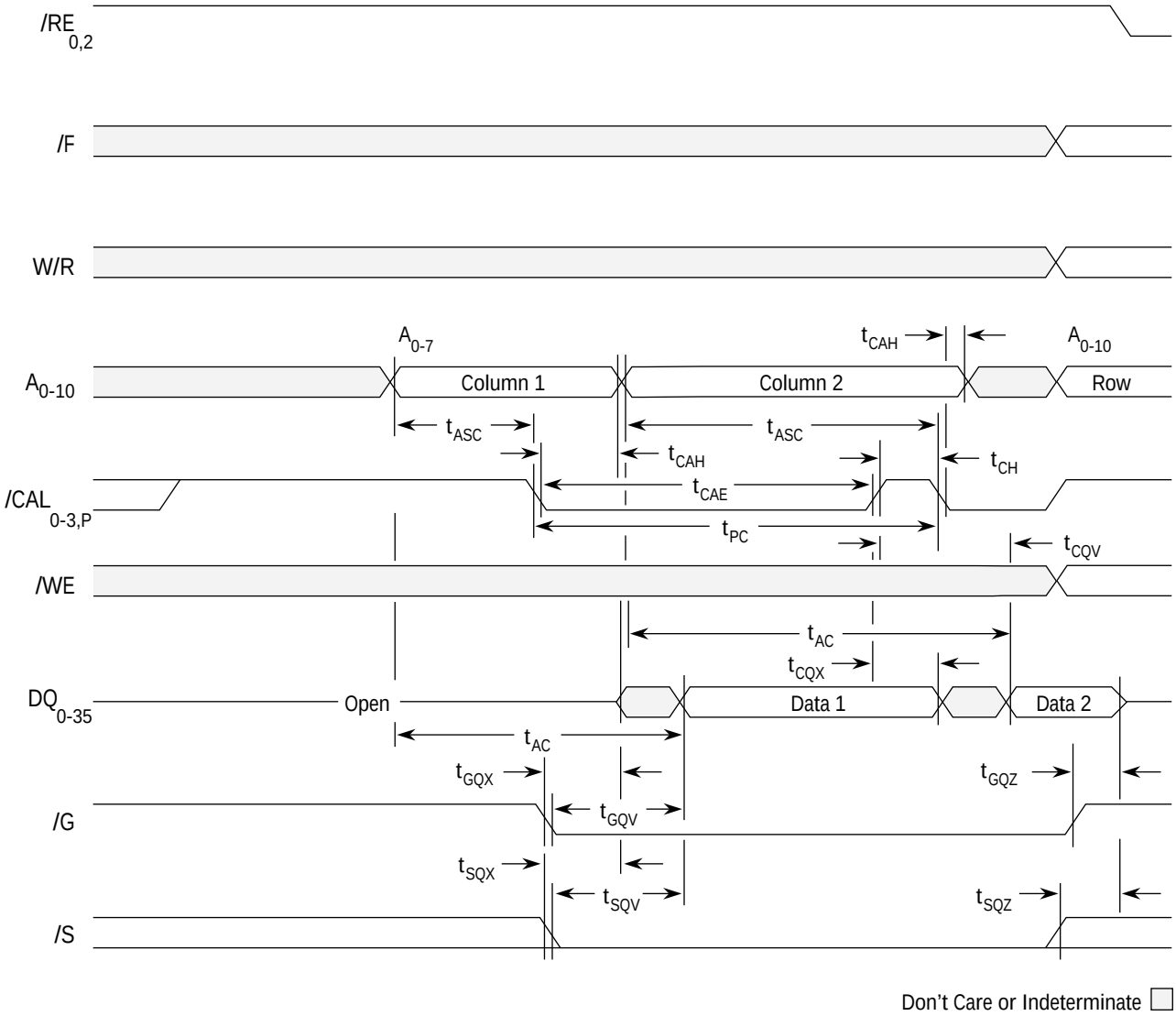
(7) For Write-Per-Bit Devices, t_{WHR} is Limited By Data Input Setup Time, t_{DS}

/RE Inactive Cache Read Hit (Static Column Mode)



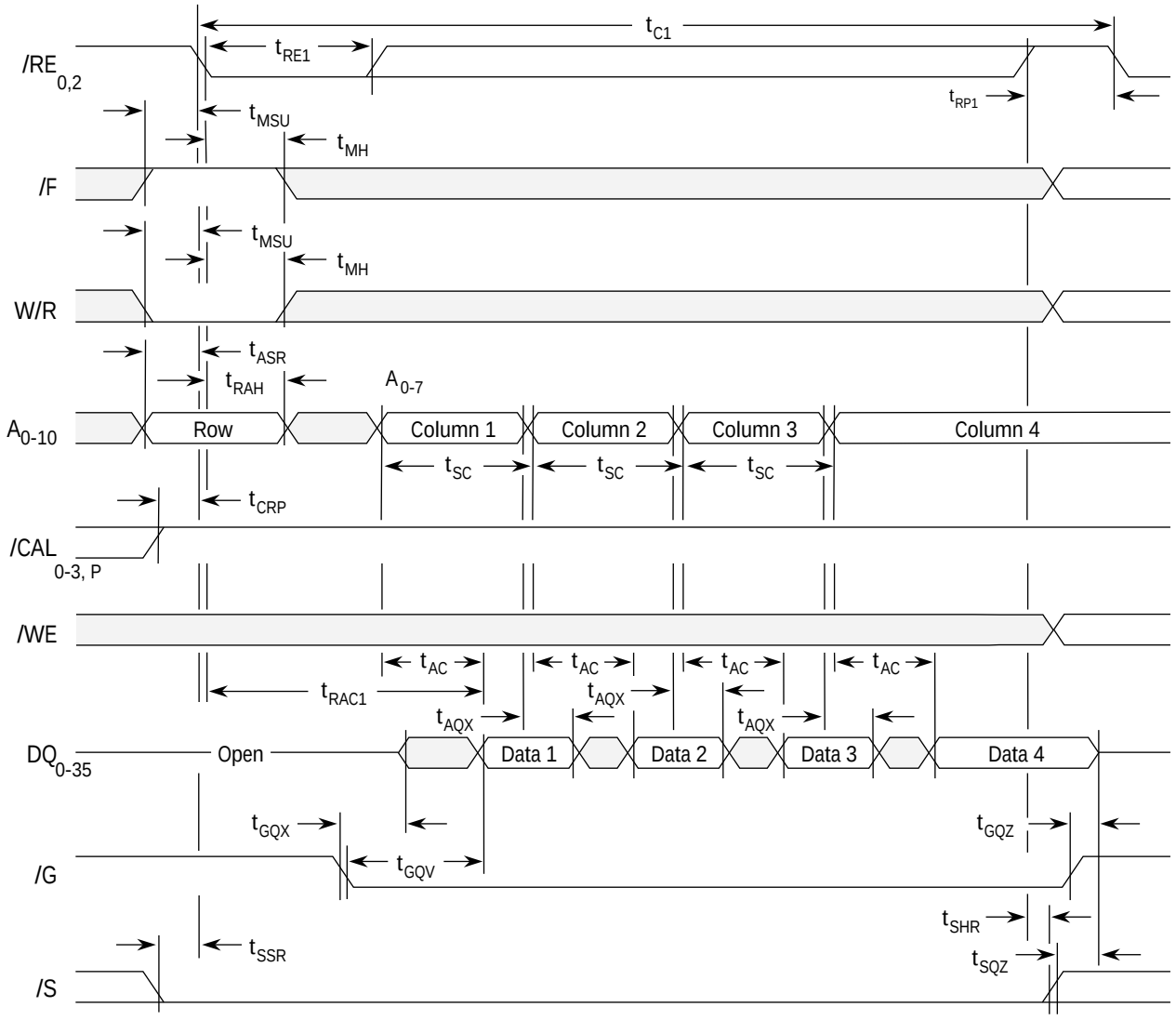
NOTES: 1. Data accessed during /RE inactive read is from the row address specified during the last /RE active read cycle.

/RE Inactive Cache Read Hit (Page Mode)

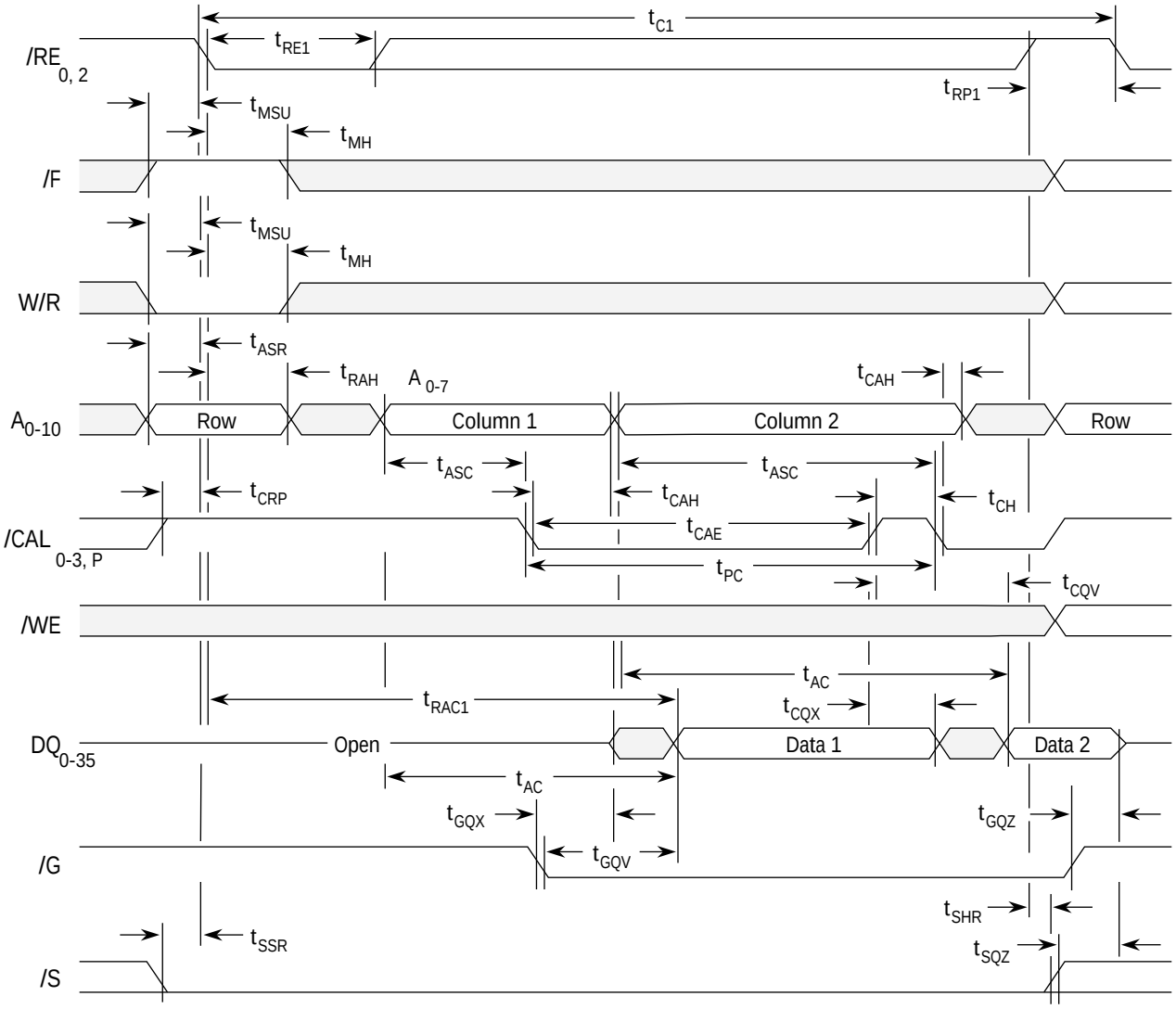


NOTES: 1. Data accessed during /RE inactive read is from the row address specified during the last /RE active read cycle.

/RE Active Cache Read Hit (Static Column Mode)

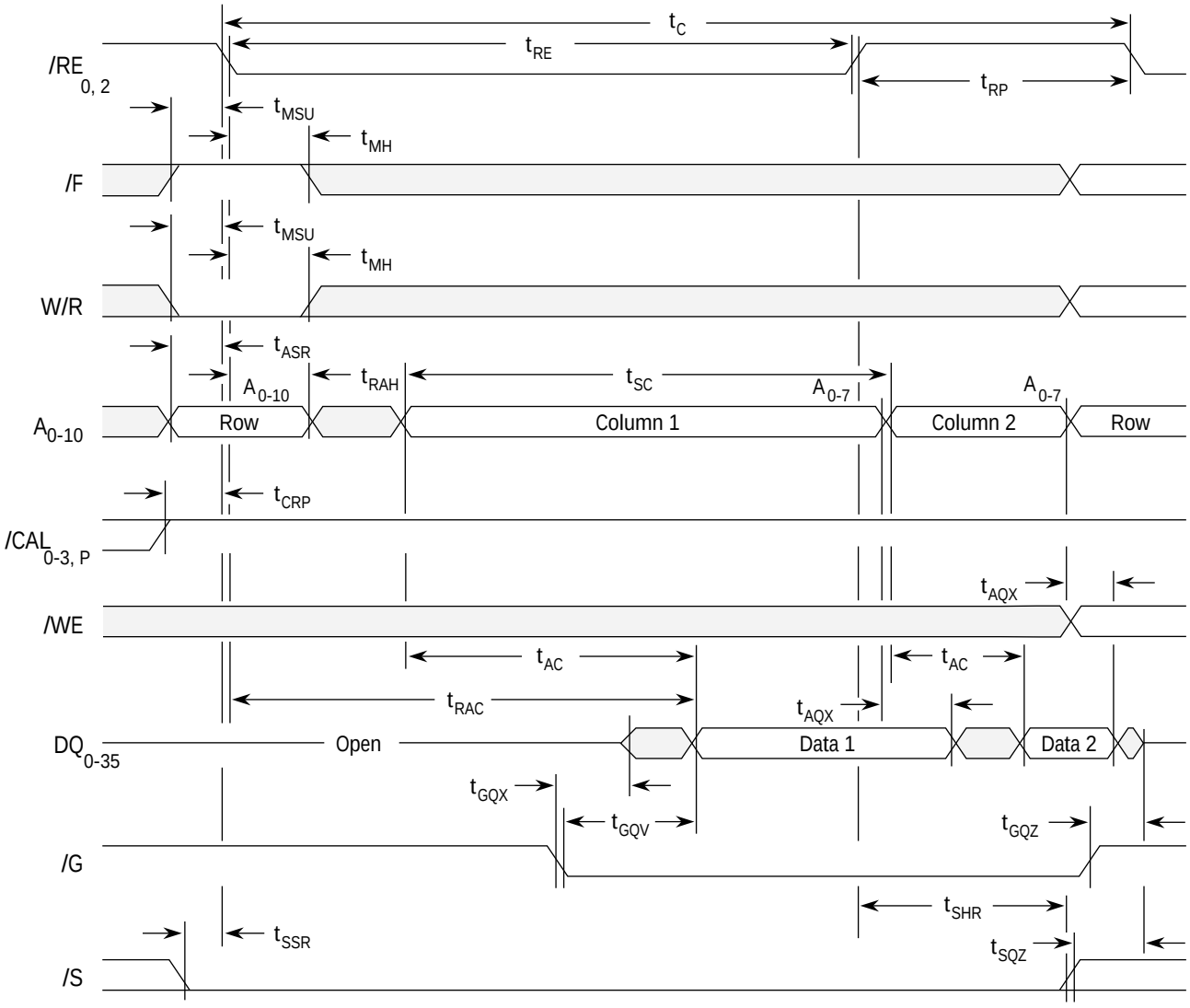


/RE Active Cache Read Hit (Page Mode)

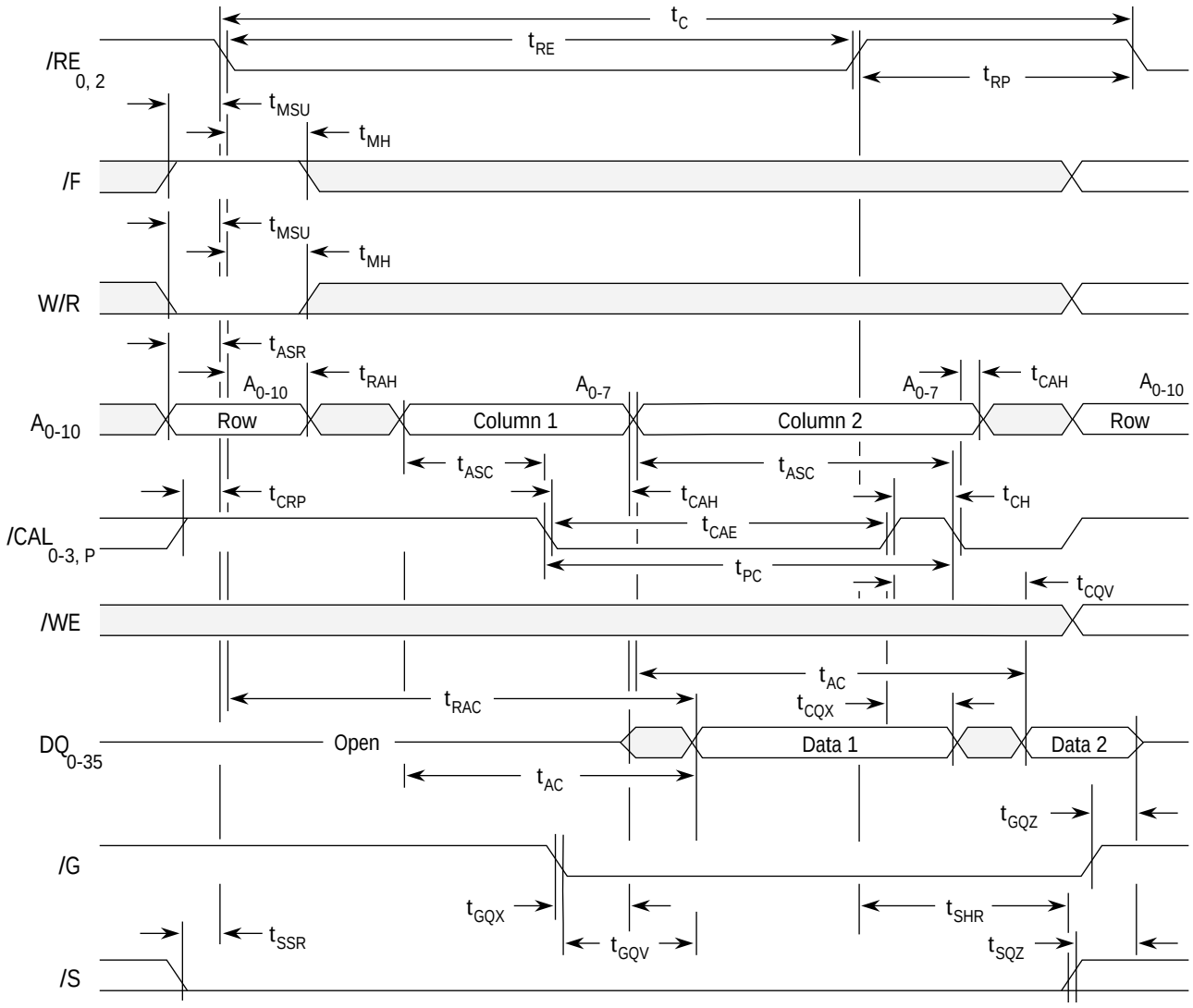


Don't Care or Indeterminate

/RE Active Cache Read Miss (Static Column Mode)

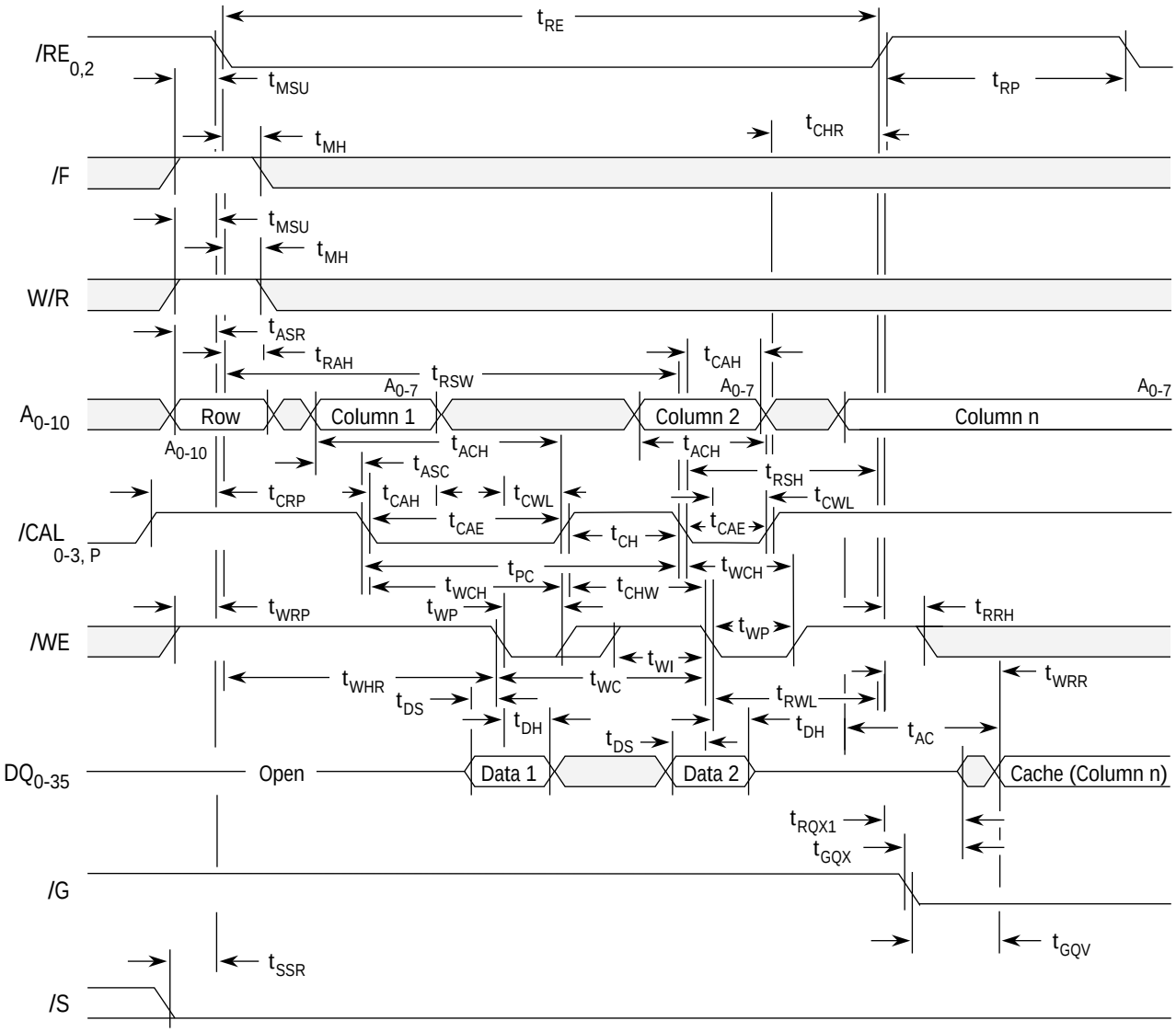


/RE Active Cache Read Miss (Page Mode)



Don't Care or Indeterminate

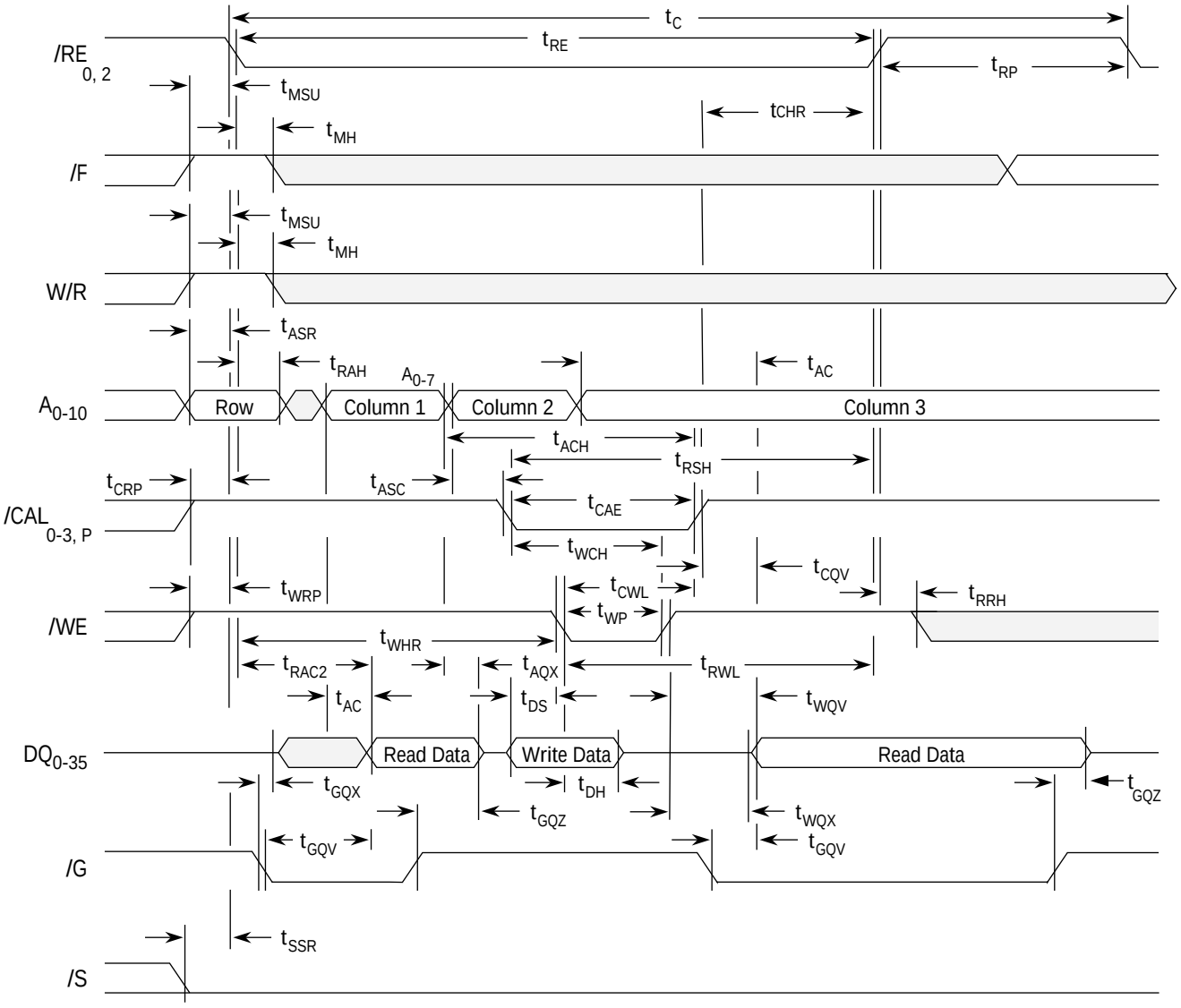
Burst Write (Hit or Miss) Followed By /RE Inactive Cache Reads



Don't Care or Indeterminate □

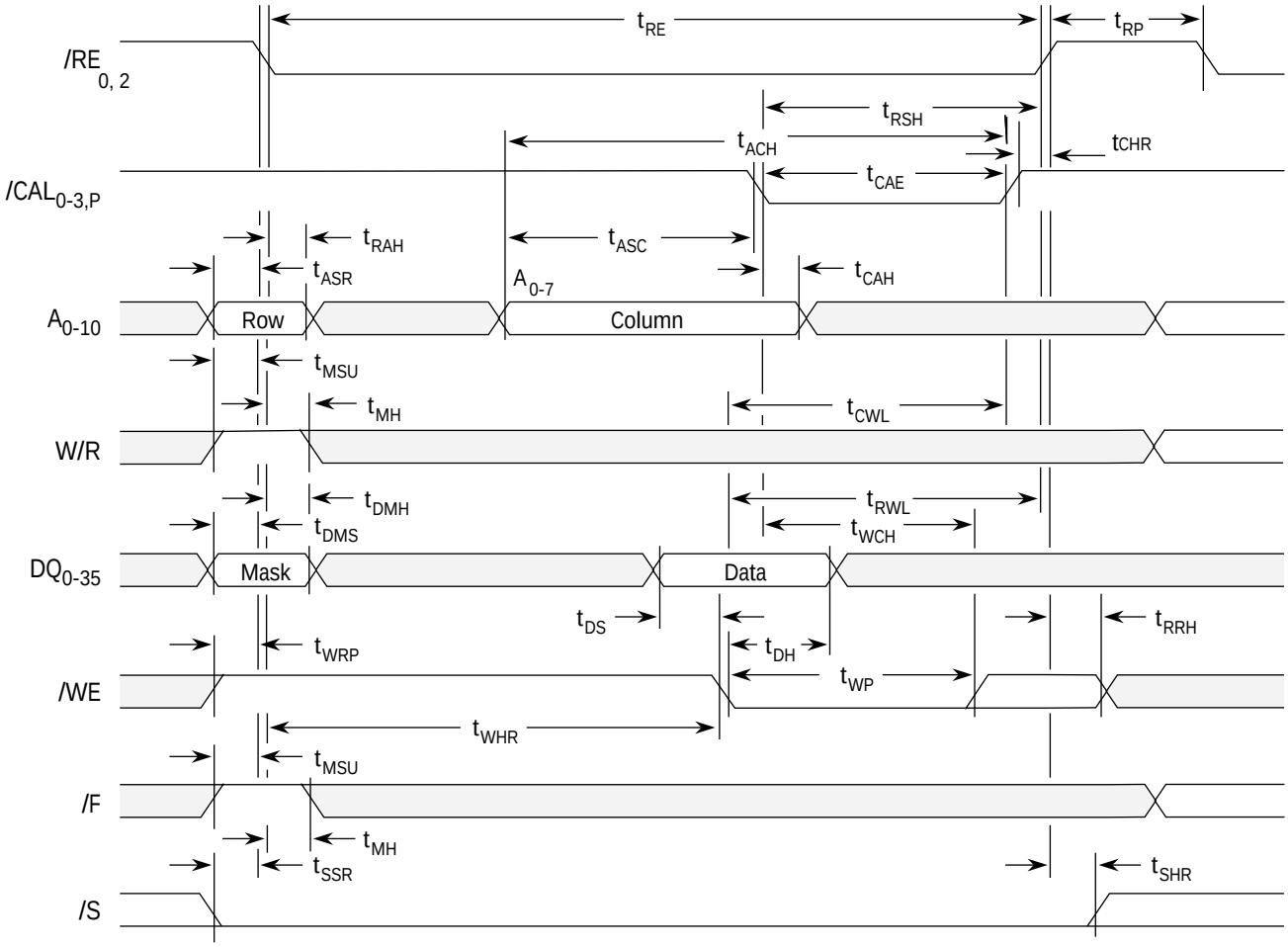
NOTES: 1. /G becomes a don't care after t_{RGX} during a write miss.

Read/Write During Write Hit Cycle (Can Include Read-Modify-Write)



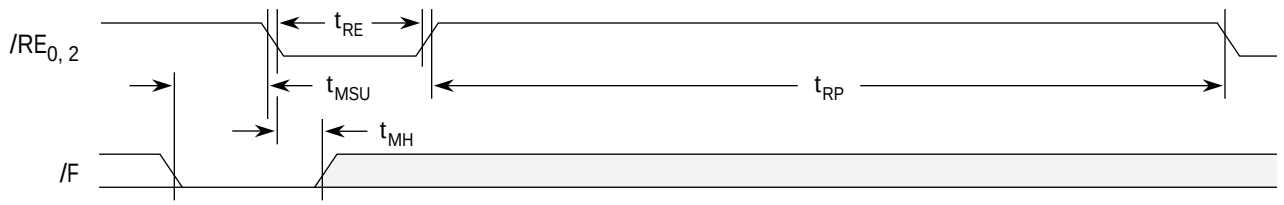
NOTES: 1. If column address one equals column address two, then a read-modify-write cycle is performed.

Write-Per-Bit Cycle (/G=High)



NOTES: 1. Data mask bit high (1) enables bit write; data mask bit low (0) inhibits bit write.
2. Write-per-bit cycle valid only for DM512K36 ST.
3. Write-per-bit waveform applies to parity bits only (DQ 8, 17, 26, 35).

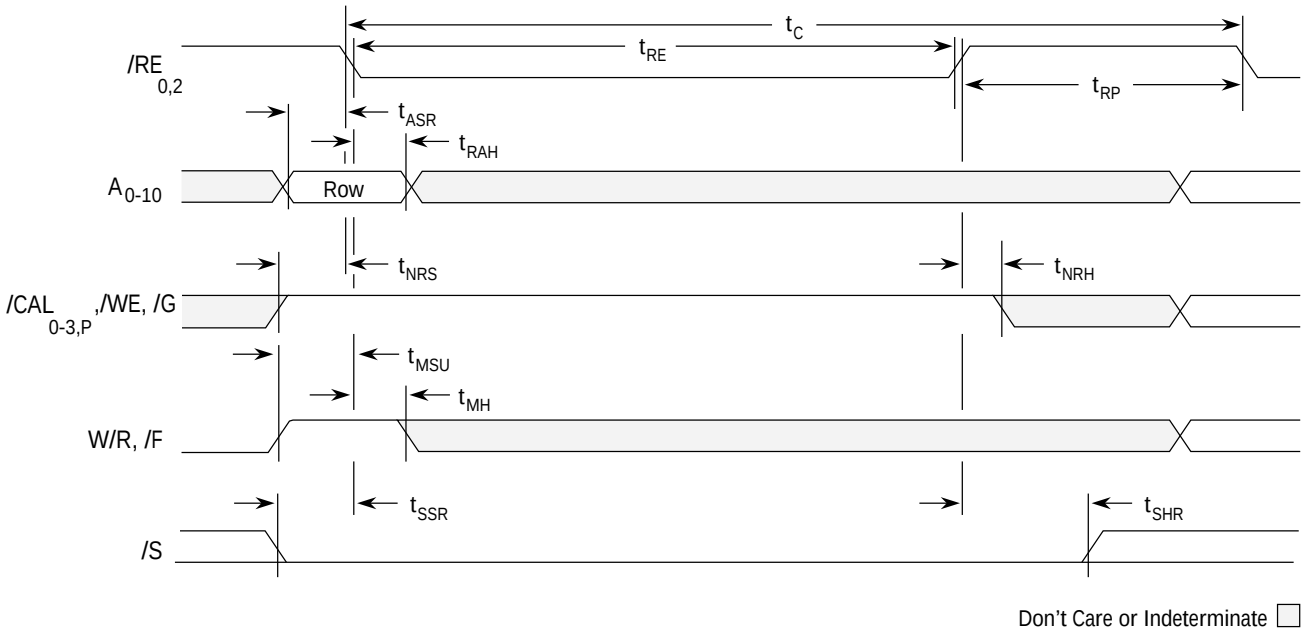
/F Refresh Cycle



NOTES: 1. During /F refresh cycles, the status of W/R, /WE, $A_{0\text{-}10}$, /CAL, /S, and /G is a don't care.

2. /RE inactive cache reads may be performed in parallel with /F refresh cycles.

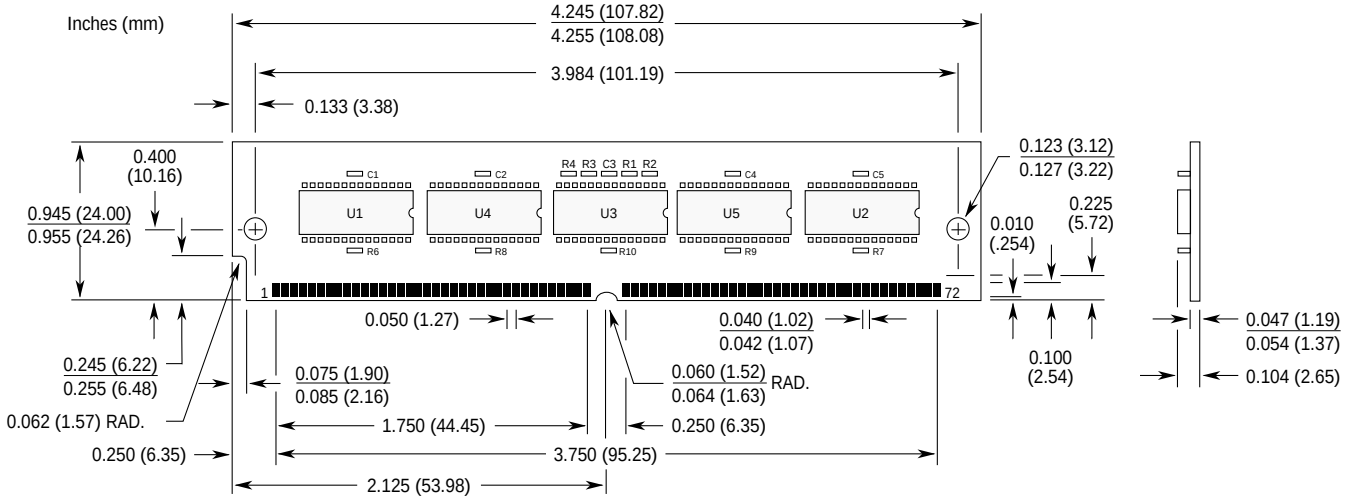
/RE-Only Refresh



NOTES: 1. All binary combinations of $A_{0\text{-}9}$ must be refreshed every 64ms interval. A_{10} does not have to be cycled, but must remain valid during row address setup and hold times.

2. /RE refresh is write cycle with no /CAL active cycle.

Mechanical Data
72 Pin SIMM Module



U1-2, U4-5 — Enhanced DM2203T-XX, 512K x 8 EDRAMs, 300 Mil TSOP
U3 — Enhanced DM2213T-XX, 512K x 8 EDRAM with write-per-bit (not present on DM512K32ST)
C1-C5 — 0.22µF Chip Capacitors
R1-R4, R6-R10 — 100KΩ Chip Resistors
Socket — AMP 822030-3 or Equivalent

Part Numbering System

DM512K36ST - 12I

Temperature Range
No Designator = 0^0 to 70^0C (Commerical)
I = 40^0 to 85^0C (Industrial)

Access Time from Cache in Nanoseconds
12ns
15ns

Packaging System
T = 300 Mil, Plastic TSOP-II

Memory Module Configuration
S = SIMM

I/O Width
32 = 32 Bits
36 = 36 Bits

Memory Depth (Kilobits)

Dynamic Memory