

DESCRIPTION:

The DPS512X16Cn3/DPS512X16Bn3 High Speed SRAM "STACK" modules are a revolutionary new memory subsystem using Dense-Pac Microsystems' ceramic Stackable Leadless Chip Carriers (SLCC). Available in straight leaded, "J" leaded or gullwing leaded packages, or mounted on a 50-pin PGA co-fired ceramic substrate. The module packs 8-Megabits of low-power CMOS static RAM in an area as small as 0.463 in², while maintaining a total height as low as 0.705 inches.

The DPS512X16Cn3/DPS512X16Bn3 STACK modules contain eight individual 128K x 8 SRAMs, each packaged in a hermetically sealed SLCC, making the modules suitable for commercial, industrial and military applications.

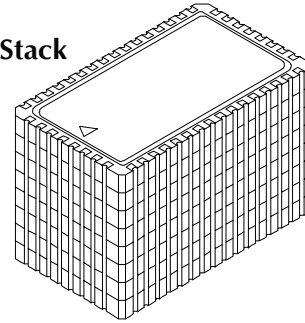
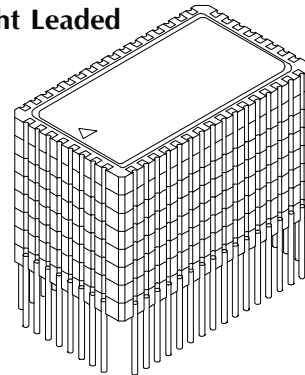
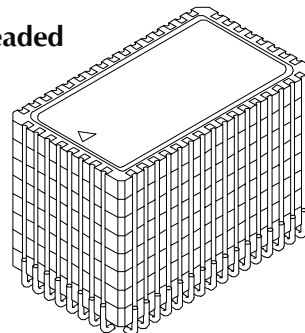
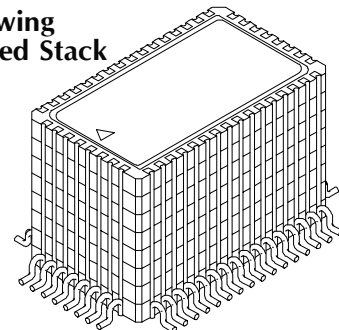
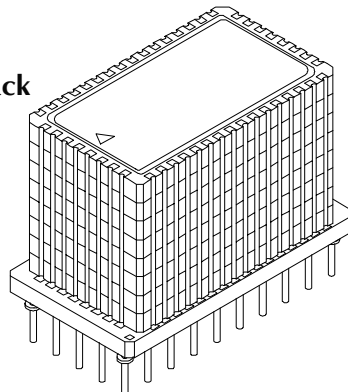
The DPS512X16Bn3 has one active low Chip Enable ($\overline{CE}$) and while the DPS512X16Cn3 an active low Chip Enable ($\overline{CE}$) and an active high Select Line (SEL).

By using SLCCs, the "Stack" family of modules offer a higher board density of memory than available with conventional through-hole, surface mount or hybrid techniques.

FEATURES:

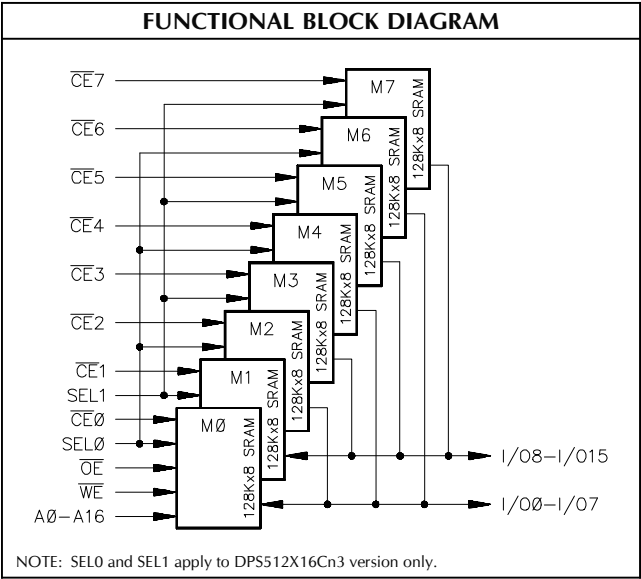
- Organizations Available: 512Kx16 or 1024Kx8
- Access Times: 20*, 25, 30, 35, 45ns
- Fully Static Operation - No clock or refresh required
- Single +5V Power Supply, $\pm 10\%$ Tolerance
- TTL Compatible
- Common Data Inputs and Outputs
- Low Data Retention Voltage: 2.0V min.
- Packages Available:
 - 48 - Pin SLCC Stack
 - 48 - Pin Straight Leaded Stack
 - 48 - Pin "J" Leaded Stack
 - 48 - Pin Gullwing Leaded Stack
 - 50 - Pin PGA Dense-Stack

* Commercial only.

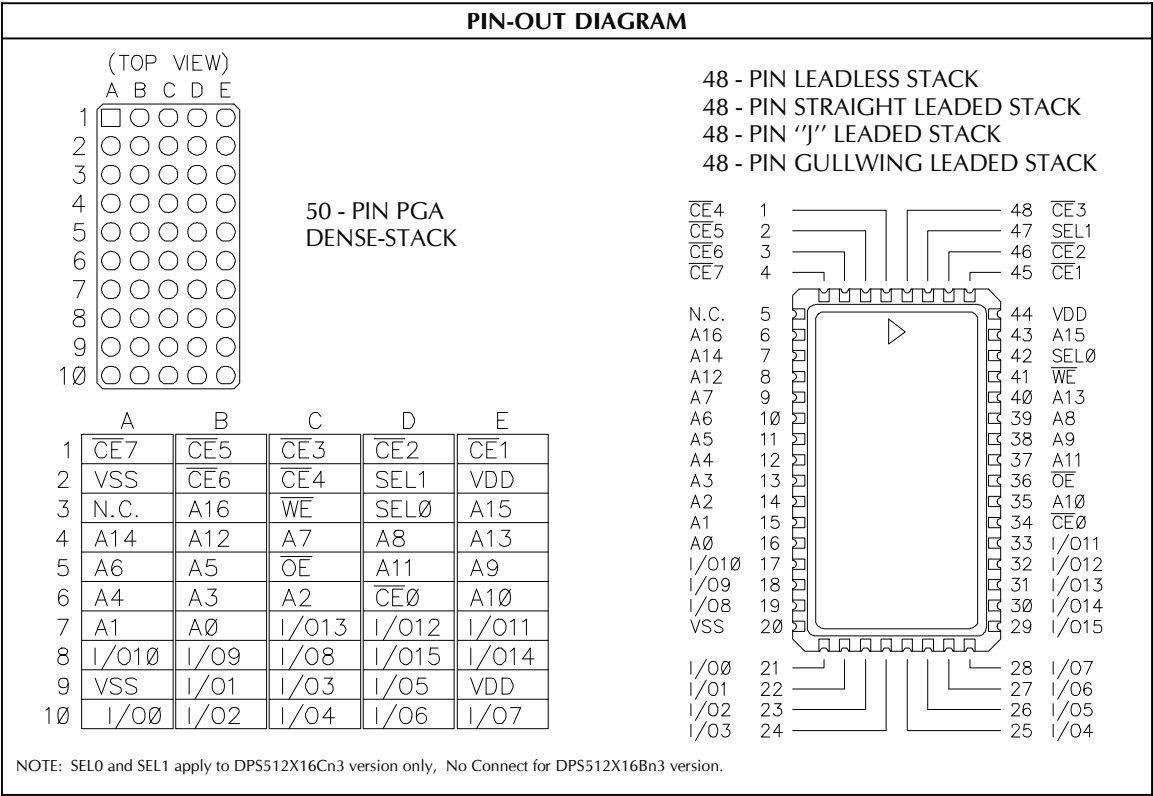
SLCC Stack**Straight Leaded Stack****"J" Leaded Stack****Gullwing Leaded Stack****Dense-Stack**

DPS512X16Cn3/DPS512X16Bn3

Dense-Pac Microsystems, Inc.



PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O15	Data Input/Output
$\overline{CE}0 - \overline{CE}7$	Low Chip Enables
SEL0, SEL1	High Chip Enables
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VDD	Power (+ 5V)
VSS	Ground
N.C.	No Connect



RECOMMENDED OPERATING RANGE ³						
Symbol	Characteristic		Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		4.5	5.0	5.5	V
V _{IH}	Input HIGH Voltage		2.2		V _{DD} +0.3	V
V _{IL}	Input LOW Voltage		-0.5 ²		0.8	V
T _A	Operating Temperature	M/B	-55	+25	+125	°C
		I	-40	+25	+85	
		C	0	+25	+70	

TRUTH TABLE						
Mode	SEL	CE	WE	OE	I/O Pin	Supply Current
Not Selected	L	X	X	X	High-Z	Standby
Not Selected	X	H	X	X	High-Z	Standby
DOUT Disable	H	L	H	H	High-Z	Active
Read	H	L	H	L	D _{OUT}	Active
Write	H	L	L	X	D _{IN}	Active

H = HIGH

L = LOW

X = Don't Care

NOTE: SEL applies to DPS512X16Cn3 version only.

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{OH}	HIGH Voltage	I _{OH} = -4.0mA	2.4		V
V _{OL}	LOW Voltage	I _{OL} = 8.0mA		0.4	V

ABSOLUTE MAXIMUM RATINGS ³			
Symbol	Parameter	Value	Unit
T _{STC}	Storage Temperature	-65 to +150	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
V _{DD}	Supply Voltage ¹	-0.5 to +7.0	°C
V _{I/O}	Input/Output Voltage ¹	-0.5 to V _{DD} +0.5	V

CAPACITANCE ⁴ : T _A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C _{ADR}	Address Input	100	pF	V _{IN} ² = 0V
C _{CE}	Chip Enable	30		
C _{SEL}	Active High Chip Select	50		
C _{WE}	Write Enable	100		
C _{OE}	Output Enable	100		
C _{I/O}	Data Input/Output	70		

NOTE: C_{SEL} applies to DPS512X16Cn3 version only.

DC OPERATING CHARACTERISTICS: Over operating ranges										
Symbol	Characteristics	Test Conditions	Typ. (†)	C		I		M		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = 0V to V _{DD}	-	-40	+40	-40	+40	-40	+40	µA
I _{OUT}	Output Leakage Current	V _{I/O} = 0V to V _{DD} , CE or OE = V _{IH} , or WE = V _{IL}	-	-40	+40	-40	+40	-40	+40	µA
I _{CC}	Operating Supply Current	Cycle = min., Duty = 100% I _{OUT} = 0mA	X8	275	350	385	405			mA
			X16	350	460	490	530			
I _{SB1}	Full Standby Supply Current	V _{IN} ≥ V _{DD} -0.2V or V _{IN} ≤ V _{SS} +0.2V	3.2		40	40	80			mA
I _{SB2}	Standby Current (TTL)	CE = V _{IH}	200		240	280	280			mA
I _{DR3}	Data Retention Supply Current (3V)	V _{DR} = 3V, CE ≥ V _{DR} -0.2V, (or SEL ≤ 0.2V, V _{IN} ≥ V _{DD} -0.2V or V _{IN} ≤ +0.2V)	0.56		3.20	4.80	16.00			mA
I _{DR2}	Data Retention Supply Current (2V)	V _{DR} = 2V, CE ≥ V _{DR} -0.2V, (or SEL ≤ 0.2V, V _{IN} ≥ V _{DD} -0.2V or V _{IN} ≤ +0.2V)	0.28		2.00	3.20	14.40			mA
V _{OL}	Output Low Voltage	I _{OUT} = 8.0mA	-		0.4	0.4	0.4			V
V _{OH}	Output High Voltage	I _{OUT} = -4.0mA	-	2.4		2.4	2.4			V

† Typical measurements made at +25°C, Cycle = min., V_{DD} = 5.0V.

NOTE: Test Conditions in parenthesis apply to DPS512X16Cn3 version only.

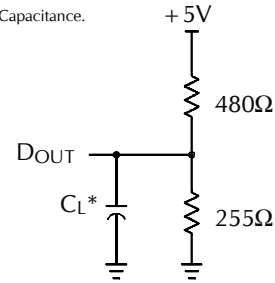
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD		
Load	C _L	Parameters Measured
1	100pF	except t _{LZ1} , t _{LZ2} , t _{HZ1} , t _{HZ2} , t _{OHZ} , t _{OLZ} , and t _{WHZ}
2	5pF	t _{LZ1} , t _{LZ2} , t _{HZ1} , t _{HZ2} , t _{OHZ} , t _{OLZ} , and t _{WHZ}

NOTE: t_{LZ2} and t_{HZ2} apply to DPS512X16Cn3 version only.

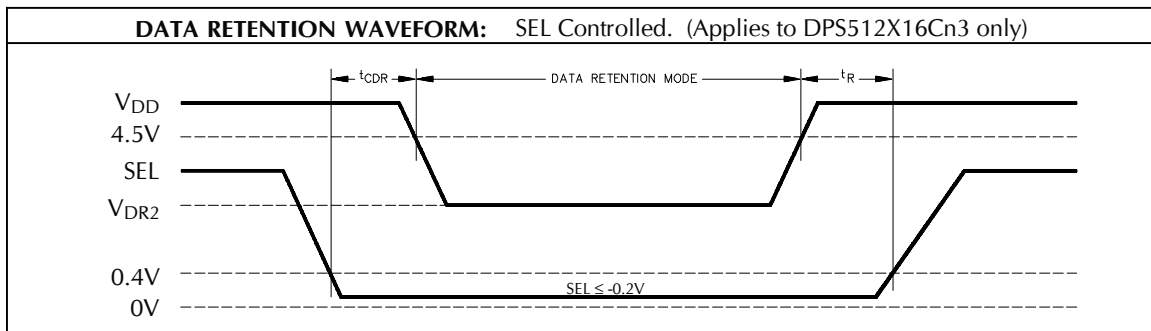
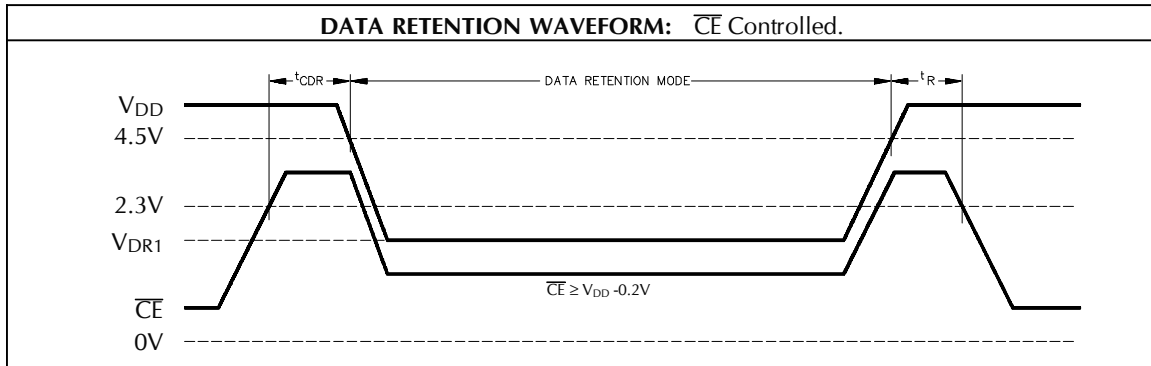
Figure 1. Output Load

* Including Probe and Jig Capacitance.



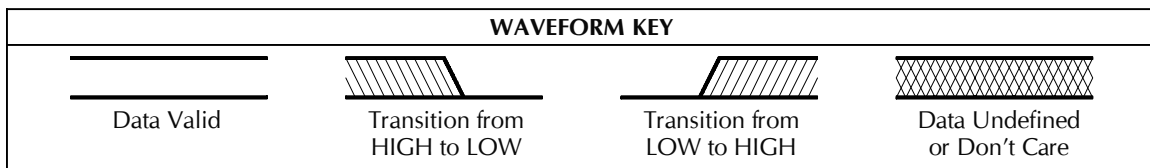
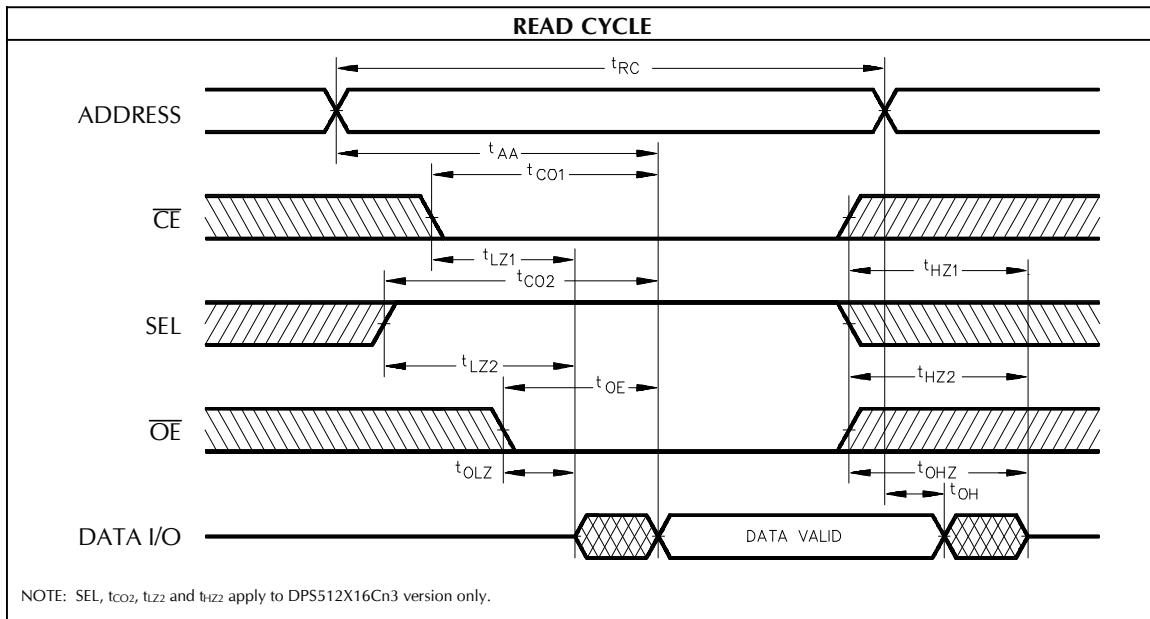
Data Retention AC Characteristics ⁸						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{DR}	V _{DD} for Data Retention	$\overline{CE} \geq V_{DR} - 0.2V$, ($SEL \geq V_{DR} - 0.2V$, or $V_{IN} \leq V_{DR} - 0.2V$ or $V_{IN} \leq 0.2V$)	2.0	-	-	V
V _{CDR}	Chip Disable to Data Retention Time	See Data Retention Waveform	0	-	-	ns
t _R	Operation Recovery Time	See Data Retention Waveform	5	-	-	ms

NOTE: Test Conditions in parenthesis apply to DPS512X16Cn3 version only.



AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	20ns*		25ns		30ns		35ns		45ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{RC}	Read Cycle Time	20		25		30		35		45		ns
2	t _{AA}	Address Access Time		20		25		30		35		45	ns
3	t _{CO1}	$\overline{CE}$ to Output Valid		20		25		30		35		45	ns
4	t _{CO2}	SEL to Output Valid		20		25		30		35		45	ns
5	t _{OE}	Output Enable to Output Valid		8		10		15		20		25	ns
6	t _{LZ1}	$\overline{CE}$ to Output in LOW-Z ^{4, 5}	3		3		3		3		3		ns
7	t _{LZ2}	SEL to Output in LOW-Z ^{4, 5}	3		3		3		3		3		ns
8	t _{OLZ}	Output Enable to Output in LOW-Z ^{4, 5}	0		0		0		0		0		ns
9	t _{HZ1}	$\overline{CE}$ to Output in HIGH-Z ^{4, 5}		10		12		15		20		25	ns
10	t _{HZ2}	SEL to Output in HIGH-Z ^{4, 5}		10		12		15		20		25	ns
11	t _{OHZ}	Output Enable to Output in HIGH-Z ^{4, 5}		8		10		15		20		25	ns
12	t _{OH}	Output Hold from Address Change	3		3		3		3		3		ns

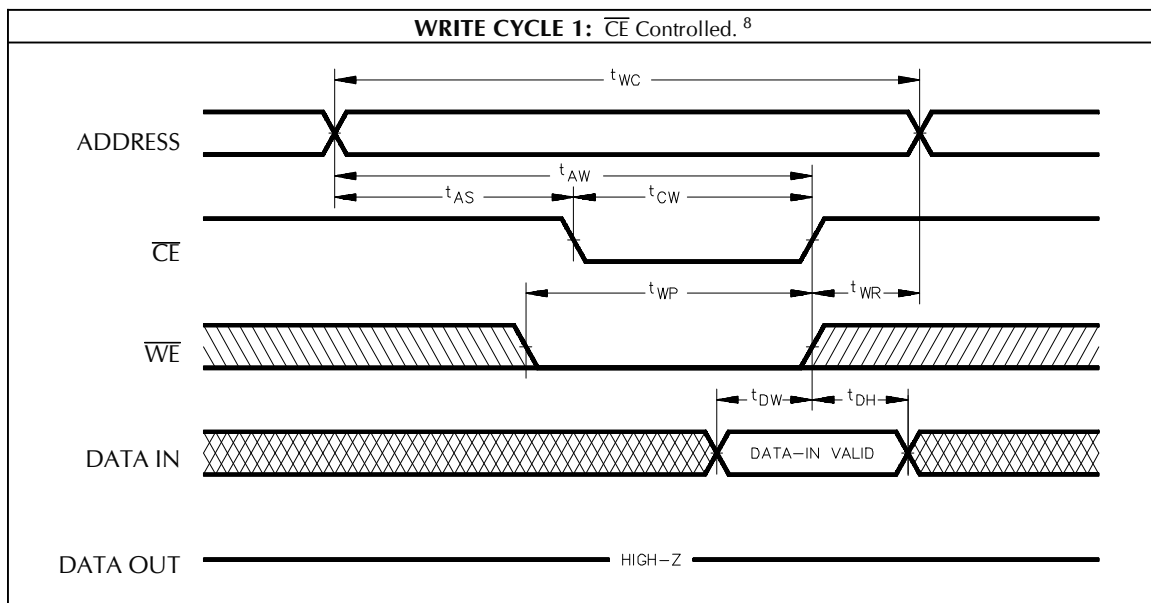
* Available in Commercial Only.

NOTE: t_{CO2}, t_{LZ2} and t_{HZ2} apply to DPS512X16Cn3 version only.

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE ^{6, 7} : Over operating ranges													
No.	Symbol	Parameter	20ns*		25ns		30ns		35ns		45ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
13	t _{WC}	Write Cycle Time	20		25		30		35		45		ns
14	t _{AW}	Address Valid to End of Write	15		20		25		30		40		ns
15	t _{CW}	Chip Enable to End of Write	15		20		25		30		40		ns
16	t _{AS}	Address Set-Up Time **	0		0		0		0		0		ns
17	t _{WP}	Write Pulse Width	15		20		25		30		35		ns
18	t _{WR}	Write Recovery Time	0		0		0		0		0		ns
19	t _{WHZ}	Write Enable to Output in HIGH-Z ^{4, 5}		8		10		12		15		20	ns
20	t _{DW}	Data to Write Time Overlap	12		15		15		20		25		ns
21	t _{DH}	Data Hold from Write Time	0		0		0		0		0		ns
22	t _{OW}	Output Active from End of Write	3		3		3		3		3		ns

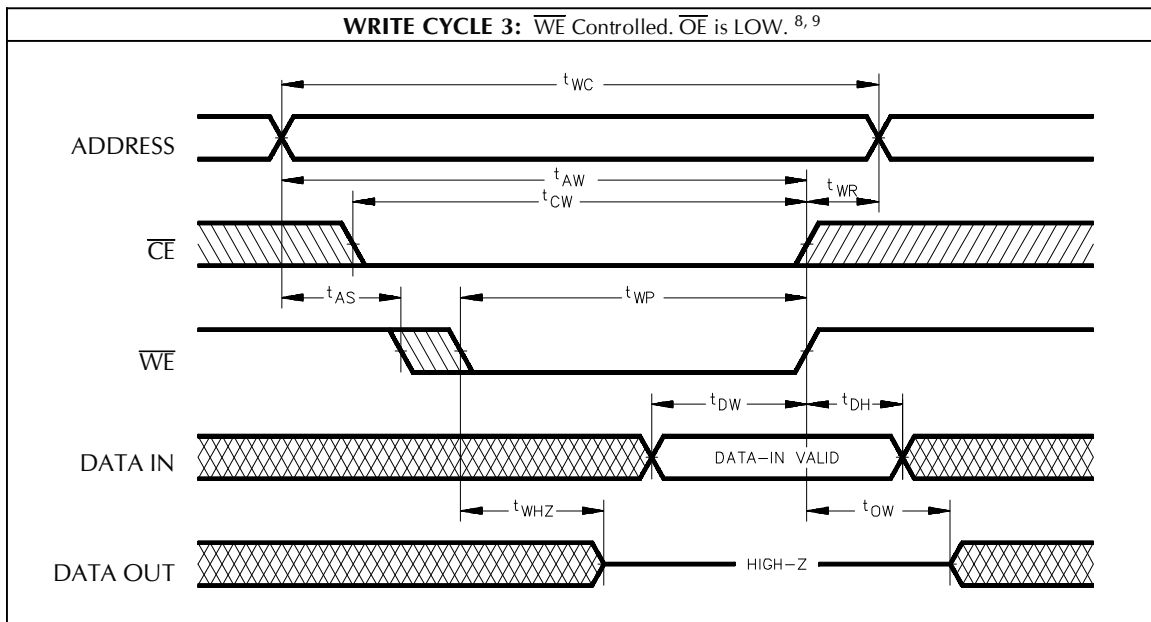
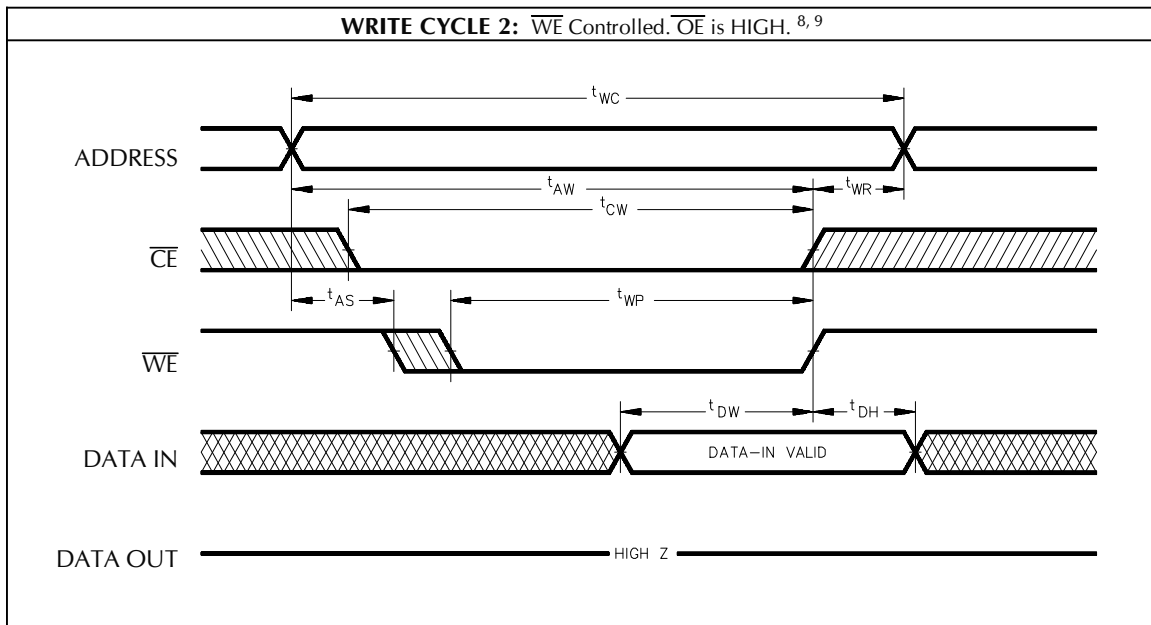
* Available in Commercial Only.

** Valid for both Read and Write Cycles.

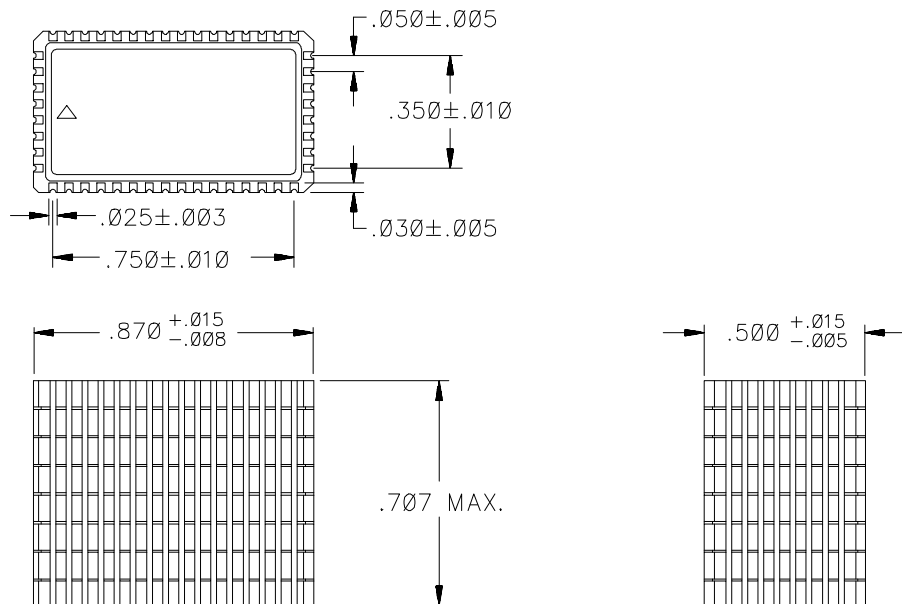


NOTES:

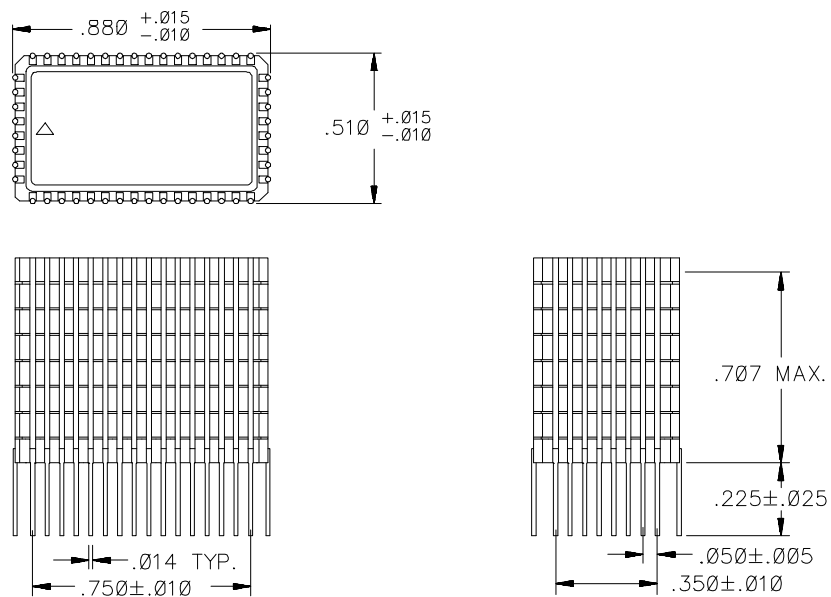
- All voltages are with respect to V_{SS} .
- 2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
- Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- This parameter is guaranteed and not 100% tested.
- Transition is measured at the point of $\pm 500\text{mV}$ from steady state voltage.
- When $\overline{\text{OE}}$ and $\overline{\text{CE}}$ are LOW and $\overline{\text{WE}}$ is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
- The outputs are in a high impedance state when $\overline{\text{WE}}$ is LOW.
- SEL timing is the same as $\overline{\text{CE}}$ timing (Valid for DPS512X16Cn3 only). The Waveform is inverted.
- Chip Enable and Write Enable can initiate and terminate WRITE Cycle.



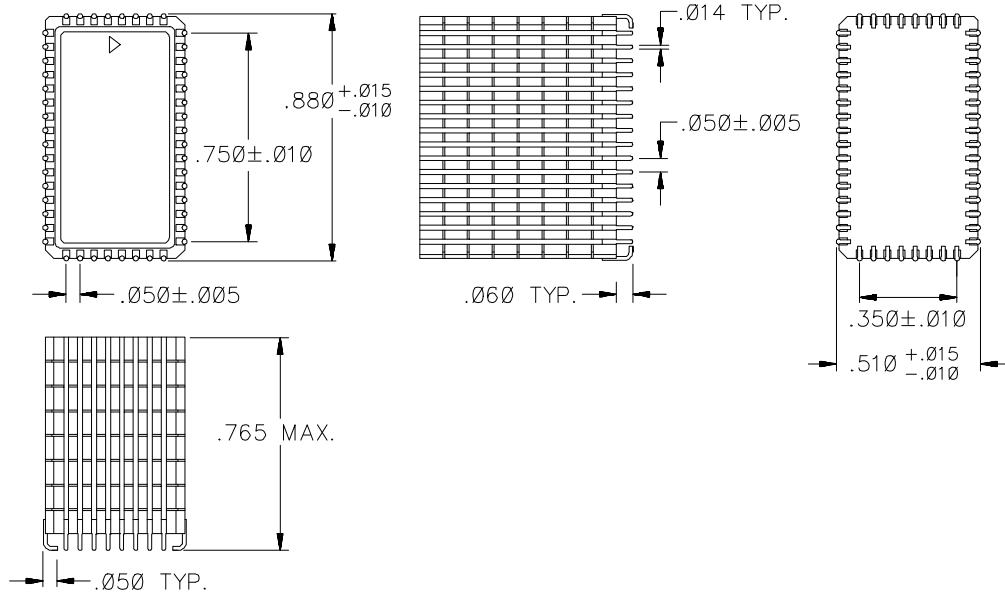
(48 - PIN LEADLESS STACK) MECHANICAL DRAWING



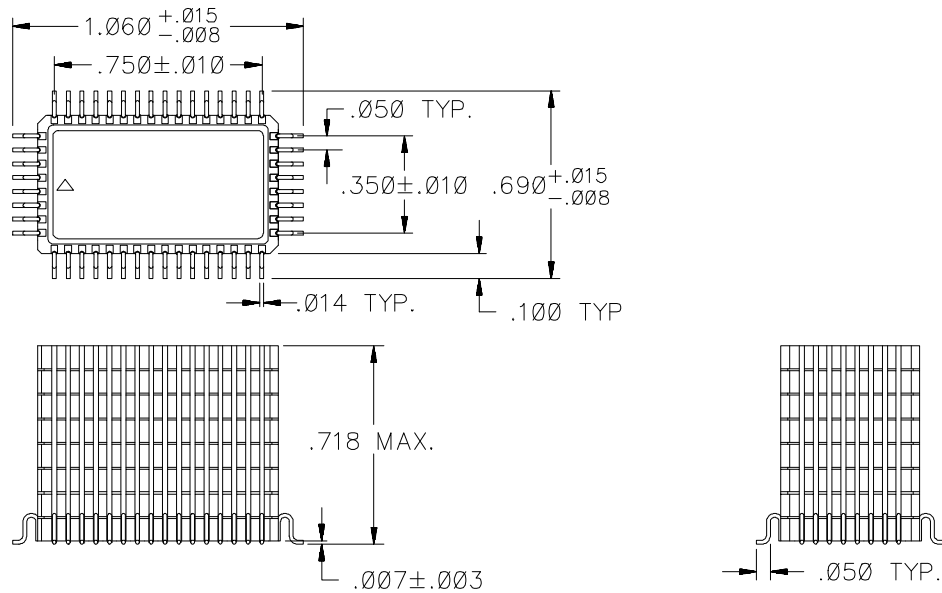
(48 - PIN STRAIGHT LEADED STACK) MECHANICAL DRAWING



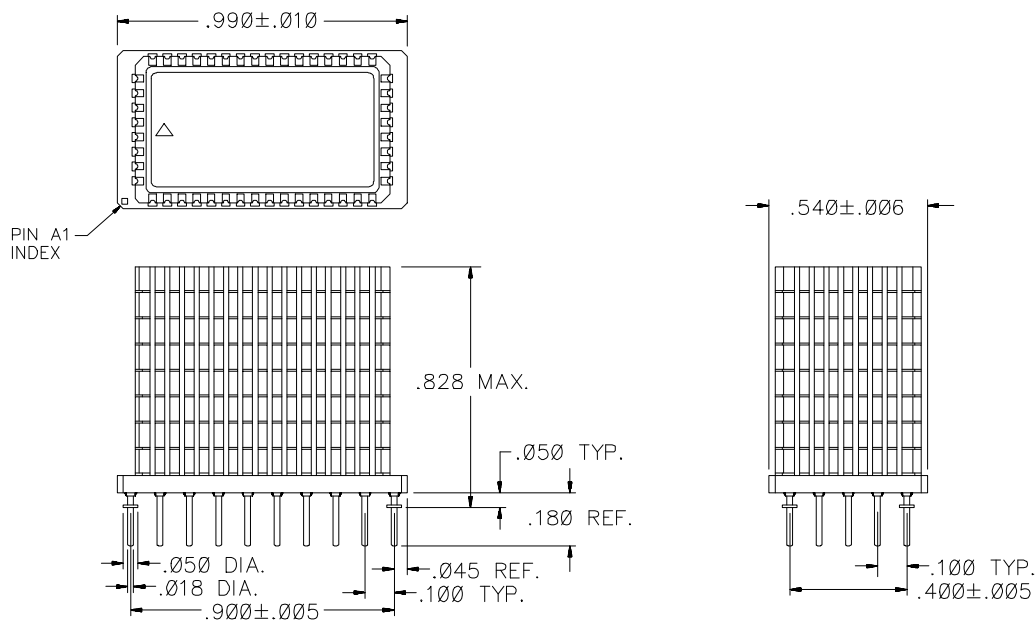
(48 - PIN "J" LEADED STACK) MECHANICAL DRAWING



(48 - PIN GULLWING LEADED STACK) MECHANICAL DRAWING



(50 - PIN PGA) MECHANICAL DRAWING



ORDERING INFORMATION

PREFIX	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	DESIG	PACKAGE	SPEED	GRADE	
DP	S	512	X	16	X	X3	-XX	X	
									C COMMERCIAL 0°C to $+70^{\circ}\text{C}$
									I INDUSTRIAL -40°C to $+85^{\circ}\text{C}$
									M MILITARY -55°C to $+125^{\circ}\text{C}$
									B MIL-PROCESSED -55°C to $+125^{\circ}\text{C}$
									20 20ns (COMMERCIAL ONLY)
									25 25ns
									30 30ns
									35 35ns
									45 45ns
									A3 DENSE-STACK PGA (PIN GRID ARRAY)
									H3 GULLWING LEADED SLCC STACK
									I3 THRU-HOLE LEADED SLCC STACK
									J3 "J" LEADED SLCC STACK
									Y3 LEADLESS SLCC STACK
									B HIGH SPEED / SINGLE CHIP ENABLE
									C HIGH SPEED / DUAL CHIP ENABLE
									MODULE WITHOUT SUPPORT LOGIC
									CMOS SRAM DEVICES

Dense-Pac Microsystems, Inc.

7321 Lincoln Way ♦ Garden Grove, California 92841-1428
 (714) 898-0007 ♦ (800) 642-4477 (Outside CA) ♦ FAX: (714) 897-1772 ♦ <http://www.dense-pac.com>