DESCRIPTION:

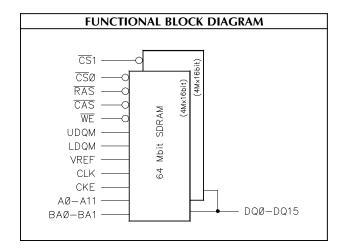
The *M-Densus* series is a family of interchangeable memory modules. The 128 Megabit SDRAM is a member of this family which utilizes the new and innovative space saving TSOP stacking technology. The modules are constructed with 4 Meg x 16 SSTL SDRAMs.

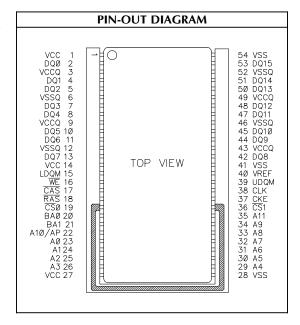
This 64 Megabit based *M-Densus* module, the DPSD8MX16RSY5 has been designed to fit in the same footprint as the 4 Meg x 16 SDRAM TSOP monolithic and 64 Megabit SDRAM based family of *M-Densus* modules. This allows the memory board designer to upgrade the memory in their products without redesigning the memory board, thus saving time and money.

FEATURES:

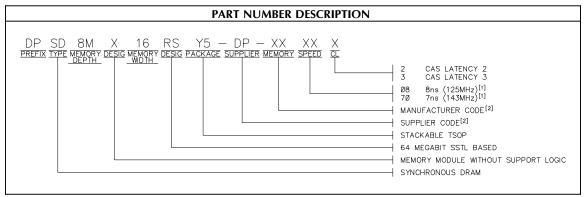
- Configuration Available:
 - 8 Meg x 16 bit (with two Chip Selects)
- Clock Frequency:
- 125, 143 MHz (max.)^[1]
- 3.3V Supply
- SSTL Compatible I/O
- Four Bank Operation
- Programmable Burst Type, Burst Length, and CAS Latency
- 4096 Cycles / 64 ms
- Auto and Self Refresh
- Package: TSOP Leadless Stack

NOTE: [1] Available in Commercial Temperature Range Only.



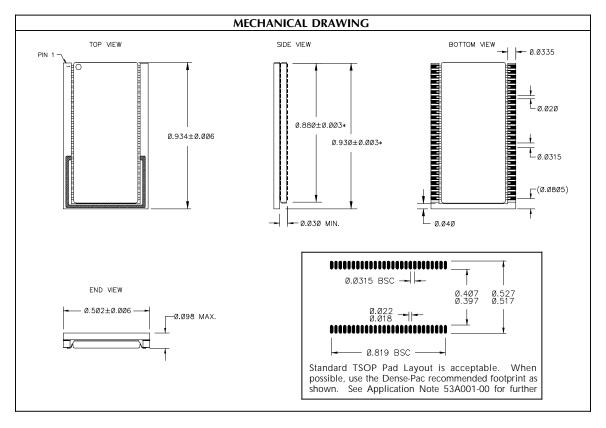


PIN NAMES	
A0 - A11	Row Address: A0 - A11 Column Address: A0 - A7
BAO, BA1	Bank Select Address
DQ0 - DQ15	Data In / Data Out
CAS	Column Address Strobes
RAS	Row Address Enables
WE	Data Write Enable
UDQM, LDQM	Upper & Lower Data Input/Output Mask
CKE	Clock Enable
CLK	System Clock
CS0-CS1	Chip Selects
V _{CC} /V _{SS}	Power Supply/Ground
Vccq/Vssq	Data Output Power/Ground
V _{REF}	Voltage Reference for Inputs
N.C.	No Connect



NOTES: [1] Available in Commercial Temperature Range Only.

Contact your sales representative for supplier and manufacturer codes.



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