# DENSE-PAC
## MICROSYSTEMS

## M-Densus
### High Density Memory Device

**256 Megabit Synchronous DRAM**
**DPSD64MX4TY5**

## DESCRIPTION:

The *M-Densus* series is a family of interchangeable memory modules. The 256 Megabit SDRAM is a member of this family which utilizes the new and innovative space saving TSOP stacking technology. The modules are constructed with 32 Meg x 4 SDRAMs.
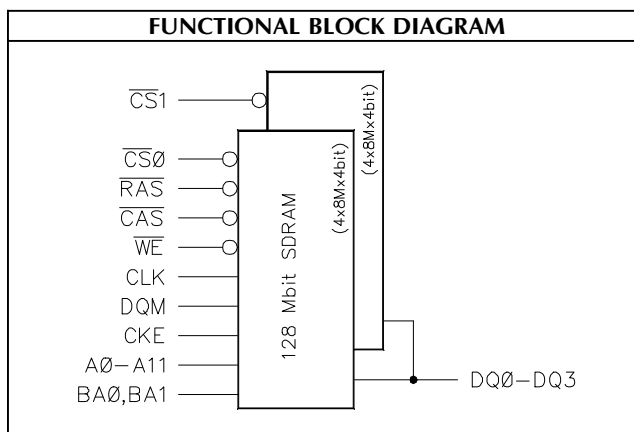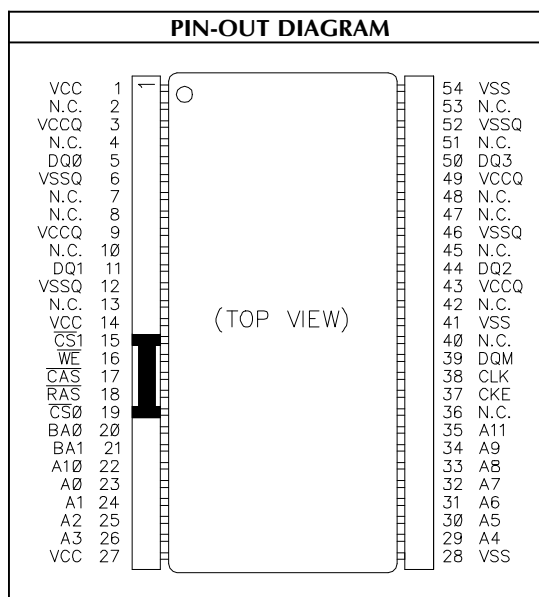
This 128 Megabit based *M-Densus* module, the DPSD64MX4TY5 has been designed to fit in the same footprint as the 32 Meg x 4 SDRAM TSOP monolithic and 64 Megabit SDRAM based family of *M-Densus* modules. This allows the memory board designer to upgrade the memory in their products without redesigning the memory board, thus saving time and money.

## FEATURES:

- Configuration Available:
  - 64 Meg x 4 (2 Banks of 8M x 4 x 4 bits)
- Clock Frequency:
  - 66[1], 83[1], 100, 125[2], 133[2] MHz (max.)
- PC100 and PC133 Compatable
- 3.3V Supply
- LVTTL Compatible I/O
- Four Bank Operation
- Programmable Burst Type, Burst Length, and CAS Latency
- 4096 Cycles / 64 ms
- Auto and Self Refresh
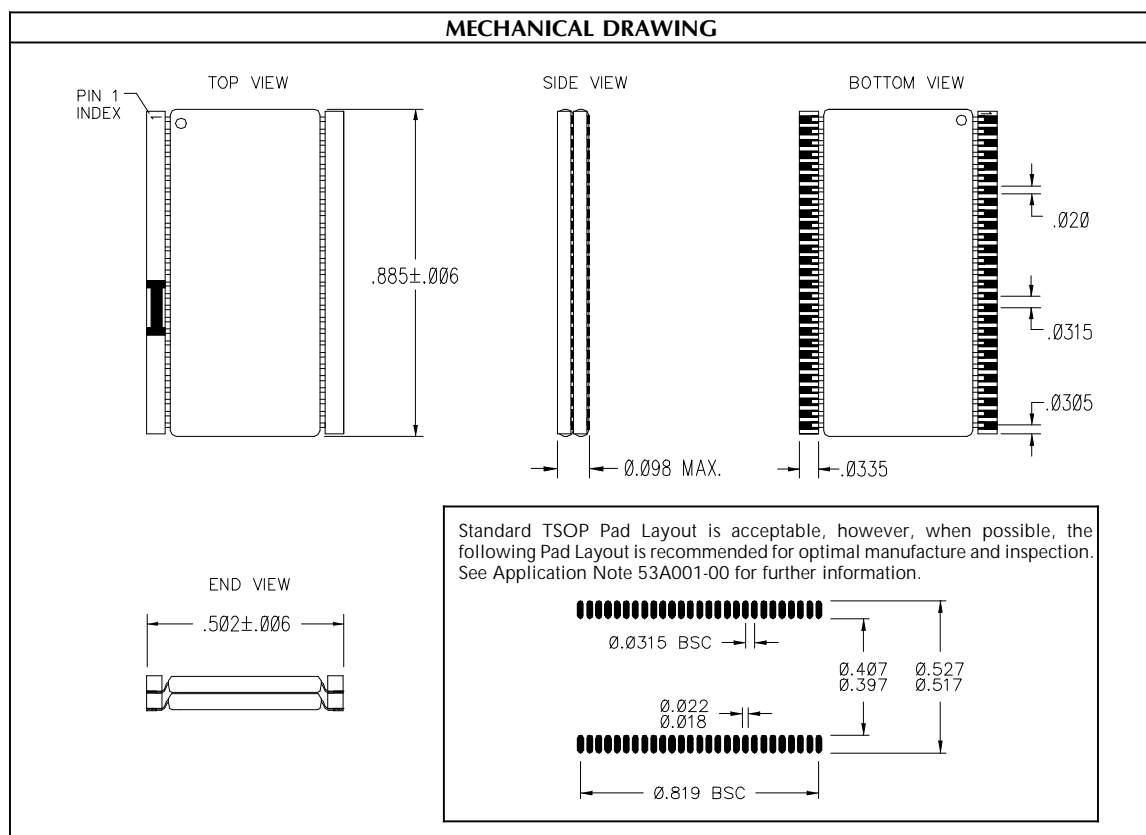- Package:   TSOP Leadless Stack

NOTES:  [1]  Available in Military and Industrial Temperature Ranges Only.
            [2]  Available in Commercial Temperature Range Only.

### PIN-OUT DIAGRAM



| VCC | 1 | | 54 | VSS |
| N.C. | 2 | | 53 | N.C. |
| VCCQ | 3 | | 52 | VSSQ |
| N.C. | 4 | | 51 | N.C. |
| DQ0 | 5 | | 50 | DQ3 |
| VSSQ | 6 | | 49 | VCCQ |
| N.C. | 7 | | 48 | N.C. |
| N.C. | 8 | | 47 | N.C. |
| VCCQ | 9 | | 46 | VSSQ |
| N.C. | 10 | | 45 | N.C. |
| DQ1 | 11 | | 44 | DQ2 |
| VSSQ | 12 | | 43 | VCCQ |
| N.C. | 13 | (TOP VIEW) | 42 | N.C. |
| VCC | 14 | | 41 | VSS |
| $\overline{CS1}$ | 15 | | 40 | N.C. |
| $\overline{WE}$ | 16 | | 39 | DQM |
| $\overline{CAS}$ | 17 | | 38 | CLK |
| $\overline{RAS}$ | 18 | | 37 | CKE |
| $\overline{CS0}$ | 19 | | 36 | N.C. |
| BA0 | 20 | | 35 | A11 |
| BA1 | 21 | | 34 | A9 |
| A10 | 22 | | 33 | A8 |
| A0 | 23 | | 32 | A7 |
| A1 | 24 | | 31 | A6 |
| A2 | 25 | | 30 | A5 |
| A3 | 26 | | 29 | A4 |
| VCC | 27 | | 28 | VSS |

### PIN NAMES

| | |
|---|---|
| A0 - A11 | Row Address:     A0 - A11<br>Column Address:  A0 - A9, A11 |
| BA0, BA1 | Bank Select Address |
| DQ0 - DQ3 | Data In / Data Out |
| $\overline{CAS}$ | Column Address Strobes |
| $\overline{RAS}$ | Row Address Enables |
| $\overline{WE}$ | Data Write Enable |
| DQM | Data Input/Output Mask |
| CKE | Clock Enable |
| CLK | System Clock |
| $\overline{CS0}$-$\overline{CS1}$ | Chip Selects |
| $V_{CC}/V_{SS}$ | Power Supply/Ground |
| $V_{CCQ}/V_{SSQ}$ | Data Output Power/Ground |
| N.C. | No Connect |

### FUNCTIONAL BLOCK DIAGRAM

## PART NUMBER DESCRIPTION

```
DP  SD  64M   X    4    T   Y5 – DP – XX   XX   X    X
```
PREFIX TYPE MEMORY DESIG MEMORY DESIG PACKAGE SUPPLIER MEMORY SPEED CL GRADE
              DEPTH       WIDTH

| | |
|---|---|
| Blank | Commercial Temperature |
| I | Industrial Temperature |
| M | Military Temperature |

2    CAS LATENCY 2

| | | |
|---|---|---|
| 15[1] | 15ns | (66MHz)[1] |
| 12[1] | 12ns | (83MHz)[1] |
| 10 | 10ns | (100MHz) |
| 08[2] | 8ns | (125MHz)[2] |
| 75[2] | 7.5ns | (133MHz)[2] |
| P1 | PC100 | |

MANUFACTURER CODE[3]

SUPPLIER CODE[3]

STACKABLE TSOP

128 MEGABIT LVTTL BASED

MEMORY MODULE WITHOUT SUPPORT LOGIC

SYNCHRONOUS DRAM

NOTES: [1] Available in Military and Industrial Temperature Ranges Only.
       [2] Available in Commercial Temperature Range Only.
       [3] Contact your sales representative for supplier and manufacturer codes.

## MECHANICAL DRAWING



TOP VIEW

PIN 1 INDEX

.885±.006

SIDE VIEW

0.098 MAX.

BOTTOM VIEW

.020

.0315

.0305

.0335

Standard TSOP Pad Layout is acceptable, however, when possible, the following Pad Layout is recommended for optimal manufacture and inspection. See Application Note 53A001-00 for further information.

0.0315 BSC

0.022
0.018

0.407    0.527
0.397    0.517

0.819 BSC

END VIEW

.502±.006