PRELIMINARY

DESCRIPTION:

The M-Densus series is a family of interchangeable memory modules. The 128 Megabit SDRAM is a member of this family which utilizes the new and innovative space saving TSOP stacking technology. The modules are constructed with 4 Meg x 16 SDRAMs.

This 128 Megabit M-Densus module, DPSD4MX32RY5, has been designed to allow 32 Output Data lines utilizing two 4 Meg x 16 SDRAM TSOP monolithics. Utilizing this M-Densus family allows the memory board designer to upgrade the memory in their products without redesigning the memory board, thus saving time and money.

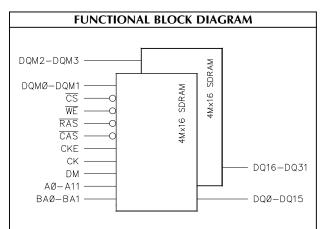
FEATURES:

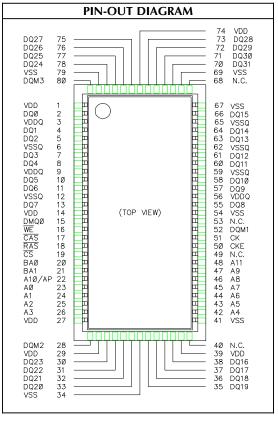
- Configuration Available:
 - 4 Meg x 32 bit

• Clock Frequency: 66^[1], 83^[1], 100, 125^[2], 133^[2] MHz (max.)

- PC100 and PC133 Compatable
- 3.3V Supply
- LVTTL Compatible I/O
- Four Bank Operation
- Programmable Burst Type, Burst Length, and CAS Latency
- 4096 Cycles / 64 ms
- Auto and Self Refresh
- Package: TSOP Leadless Stack

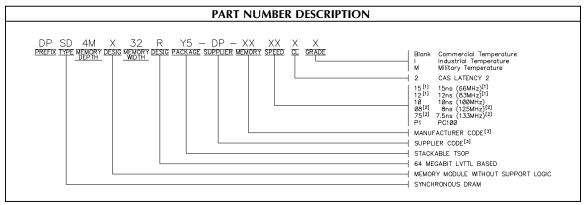
NOTES: [1] Available in Military and Industrial Temperature Ranges Only. [2] Available in Commercial Temperature Range Only.



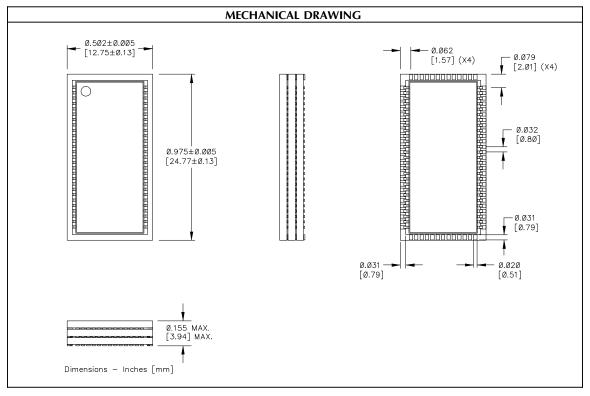


PIN NAMES	
A0 - A11	Row Address: A0 - A11 Column Address: A0 - A7
BAO, BA1	Bank Select Address
DQ0 - DQ32	Data In / Data Out
CS	Chip Select
CAS	Column Address Strobes
RAS	Row Address Enables
WE	Data Write Enable
DQM0, DQM1	Data Inputs/Output Masks
CKE	Clock Enable
CLK	System Clock
V_{DD} / V_{SS}	Power Supply/Ground
$V_{\rm DDQ}$ / $V_{\rm SSQ}$	Data Output Power/Ground
N.C.	No Connect

PRELIMINARY



- NOTES: [1] Available in Military and Industrial Temperature Ranges Only.
 [2] Available in Commercial Temperature Range Only.
 [3] Contact your sales representative for supplier and manufacturer codes.



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