DENSE-PAC
M I C R O S Y S T E M S

256 Megabit Synchronous DRAM
DPSD32MX8TY5

DESCRIPTION:

The LP-Stack™ series is a family of interchangeable memory modules. The 256 Megabit SDRAM is a member of this family which utilizes the new and innovative space saving TSOP stacking technology. The modules are constructed with 32 Meg x 4 SDRAMs.
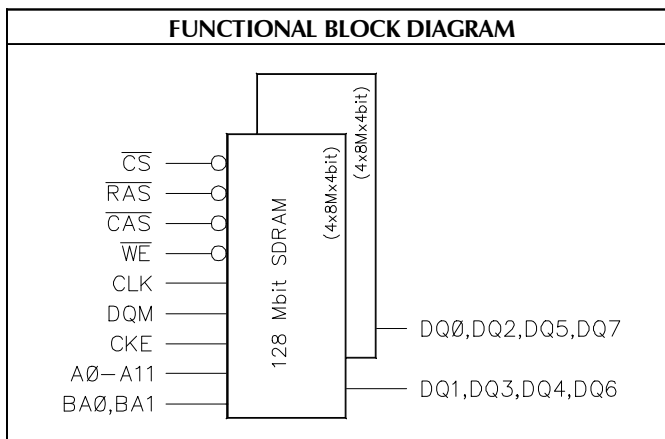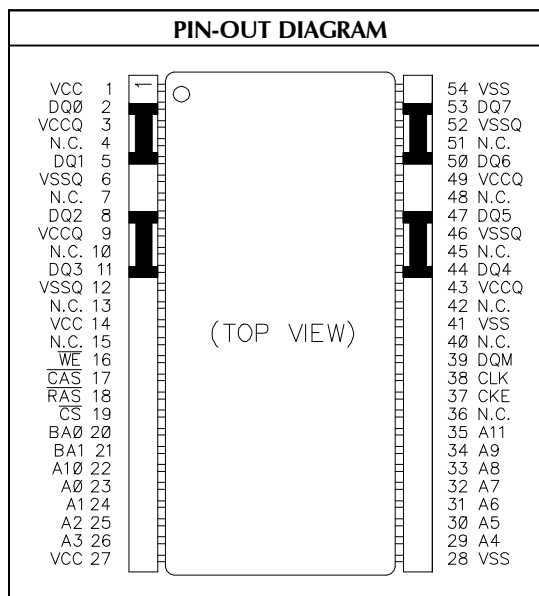
This 128 Megabit based LP-Stack™ module, the DPSD32MX8TY5 has been designed to fit in the same footprint as the 16 Meg x 8 SDRAM TSOP monolithic and 64 Megabit SDRAM based family of LP-Stack™ modules. This allows the memory board designer to upgrade the memory in their products without redesigning the memory board, thus saving time and money.

FEATURES:

- Configuration Available:
  - 32 Meg x 8 (2 Banks of 8M x 4 x 4 bits)
- Clock Frequency:
  - $66^{[1]}$, $83^{[1]}$, 100, $125^{[2]}$, $133^{[2]}$ MHz (max.)
- PC100 and PC133 Compatible
- 3.3V Supply
- LVTTL Compatible I/O
- Four Bank Operation
- Programmable Burst Type, Burst Length, and CAS Latency
- 4096 Cycles / 64 ms
- Auto and Self Refresh
- Package: TSOP Leadless Stack

NOTES: [1] Available in Extended Temperature Ranges Only.
[2] Available in Commercial Temperature Range Only

PIN-OUT DIAGRAM

VCC	1	54	VSS
DQØ	2	53	DQ7
VCCQ	3	52	VSSQ
N.C.	4	51	N.C.
DQ1	5	50	DQ6
VSSQ	6	49	VCCQ
N.C.	7	48	N.C.
DQ2	8	47	DQ5
VCCQ	9	46	VSSQ
N.C.	10	45	N.C.
DQ3	11	44	DQ4
VSSQ	12	43	VCCQ
N.C.	13	42	N.C.
VCC	14	41	VSS
N.C.	15	40	N.C.
WE	16	39	DQM
CAS	17	38	CLK
RAS	18	37	CKE
CS	19	36	N.C.
BAØ	20	35	A11
BA1	21	34	A9
A10	22	33	A8
AØ	23	32	A7
A1	24	31	A6
A2	25	30	A5
A3	26	29	A4
VCC	27	28	VSS

(TOP VIEW)

PIN NAMES

A0 - A11	Row Address: A0 - A11 Column Address: A0 - A9
BA0, BA1	Bank Select Address
DQ0 - DQ7	Data In / Data Out
CAS	Column Address Strobes
RAS	Row Address Enables
WE	Data Write Enable
DQM	Data Input/Output Mask
CKE	Clock Enable
CLK	System Clock
CS	Chip Select
V$_{CC}$/V$_{SS}$	Power Supply/Ground
V$_{CCQ}$/V$_{SSQ}$	Data Output Power/Ground
N.C.	No Connect

FUNCTIONAL BLOCK DIAGRAM

CS, RAS, CAS, WE, CLK, DQM, CKE, AØ—A11, BAØ,BA1 → 128 Mbit SDRAM (4x8Mx4bit) (4x8Mx4bit) → DQØ,DQ2,DQ5,DQ7 / DQ1,DQ3,DQ4,DQ6

PART NUMBER DESCRIPTION

DP SD 32M X 8 T Y5 — DP — XX XX X X
PREFIX TYPE MEMORY DESIG MEMORY DESIG PACKAGE SUPPLIER MEMORY SPEED CL GRADE
           DEPTH   WIDTH

Blank	Commercial Temperature
I	Industrial Temperature
M	Military Temperature
2	CAS LATENCY 2
15 [1]	15ns (66MHz) [1]
12 [1]	12ns (83MHz) [1]
10	10ns (100MHz)
Ø8 [2]	8ns (125MHz) [2]
75 [2]	7.5ns (133MHz) [2]
P1	PC100

MANUFACTURER CODE [3]
SUPPLIER CODE [3]
STACKABLE TSOP
128 MEGABIT LVTTL BASED
MEMORY MODULE WITHOUT SUPPORT LOGIC
SYNCHRONOUS DRAM
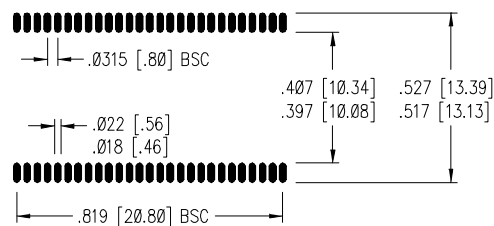
NOTES: [1] Available in Extended Temperature Ranges Only.
         [2] Available in Commercial Temperature Range Only.
         [3] Contact your sales representative for supplier and manufacturer codes.

MECHANICAL DRAWING

TOP VIEW

PIN 1 INDEX

.885±.010
[22.48±.25]

.502±.008
[12.75±.20]

END VIEW

SIDE VIEW

.098 MAX.
[2.45 MAX.]

BOTTOM VIEW

.020 [.51]

.0315 [.80]

.0305 [.775]

.0335 [.85]
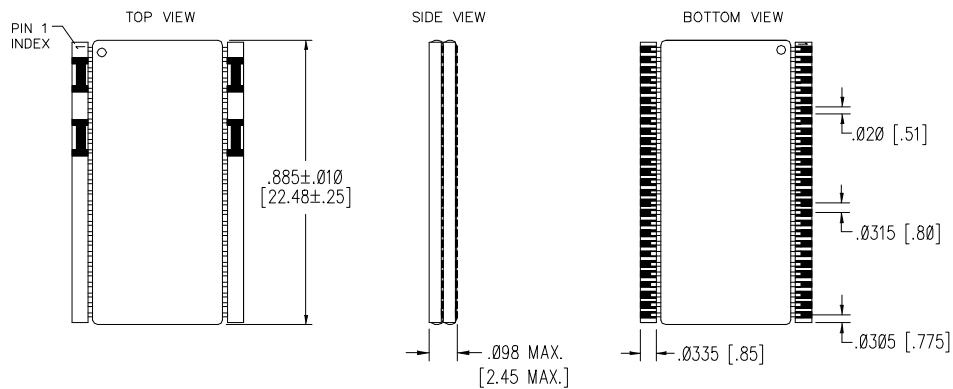
Standard TSOP pad layout is acceptable, however, when possible, the following pad layout is recommended for optimal manufacture and inspection. See Application Note 53A001−00 for further information.

.0315 [.80] BSC

.022 [.56]
.018 [.46]

.407 [10.34] .527 [13.39]
.397 [10.08] .517 [13.13]

.819 [20.80] BSC

30A213-00
REV. C