256 Megabit Synchronous DRAM DPSD32MX8TKY5

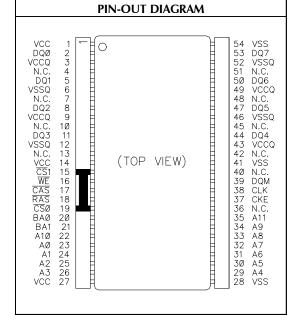
DESCRIPTION:

The LP-Stack™ series is a family of interchangeable memory modules. The 256 Megabit SDRAM is a member of this family which utilizes the new and innovative space saving TSOP stacking technology. The modules are constructed with 16 Meg x 8 SDRAMs.

This 128 Megabit based LP-Stack™ module, the DPSD32MX8TKY5 has been designed to fit in the same footprint as the 16 Meg x 8 SDRAM TSOP monolithic and 128 Megabit SDRAM based family of LP-Stack™ modules. This allows the memory board designer to upgrade the memory in their products without redesigning the memory board, thus saving time and money.

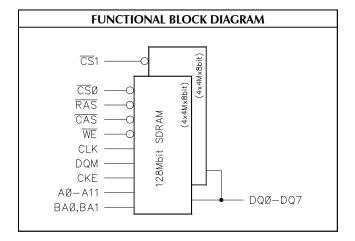


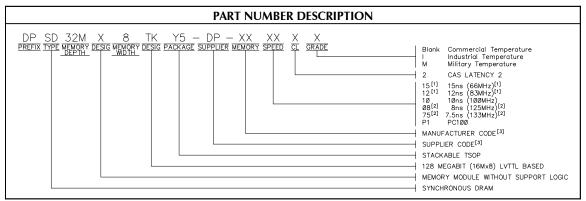
- Configuration Available:
 - 32 Meg x 8 (2 Banks of 4M x 4 x 8 bits)
- Clock Frequency: 66^[1], 83^[1], 100, 125^[2], 133^[2] MHz (max.)
- PC100 and PC133 Compatable
- 3.3V Supply
- LVTTL Compatible I/O
- Four Bank Operation
- Programmable Burst Type, Burst Length, and CAS Latency
- 4096 Cycles / 64 ms
- Auto and Self Refresh
- Package: TSOP Leadless Stack



| NOTES: | Available in Military and Industrial Temperature Ranges O | nly. |
|--------|---|------|
| | 21 Available in Commercial Temperature Range Only | |

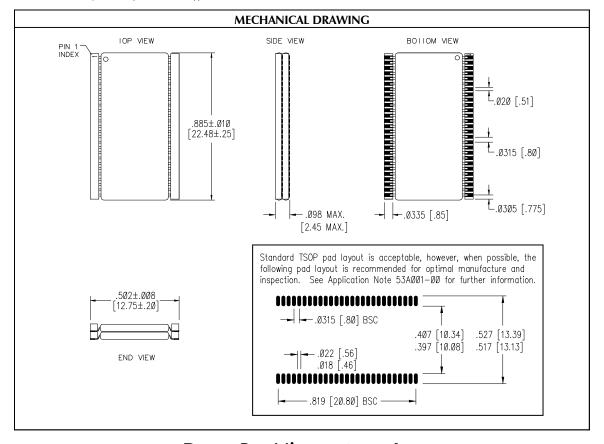
| PIN NAMES | | | |
|------------------------------------|--|--|--|
| A0 - A11 | Row Address: A0 - A11 Column Address: A0 - A9 | | |
| BAO, BA1 | Bank Select Address | | |
| DQ0 - DQ7 | Data In / Data Out | | |
| CAS | Column Address Strobes | | |
| RAS | Row Address Enables | | |
| WE | Data Write Enable | | |
| DQM | Data Input/Output Mask | | |
| CKE | Clock Enable | | |
| CLK | System Clock | | |
| CS0-CS1 | Chip Selects | | |
| V _{CC} /V _{SS} | Power Supply/Ground | | |
| V _{CCQ} /V _{SSQ} | Data Output Power/Ground | | |
| N.C. | No Connect | | |





- [1] Available in Military and Industrial Temperature Ranges Only.

 - [2] Available in Commercial Temperature Range Only.[3] Contact your sales representative for supplier and manufacturer codes.



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