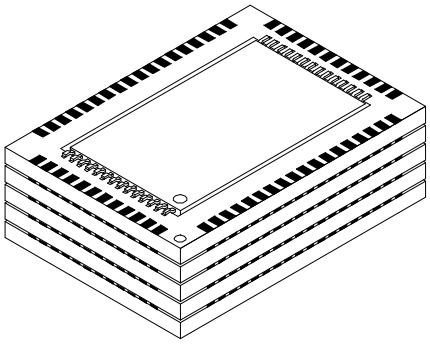
DENSE-PAC MICROSYSTEMS

M-Densus
High Density Memory Device

1 Megabit High Speed SRAM
DPS32KX32Y5

PRELIMINARY



DESCRIPTION:

The DPS32KX32Y5 a 32K x 32 SRAM module the utilize the new and innovative space saving TSOP stacking technology. The module is constructed of four 32K x 8 SRAM's that are configured as 32K x 32.

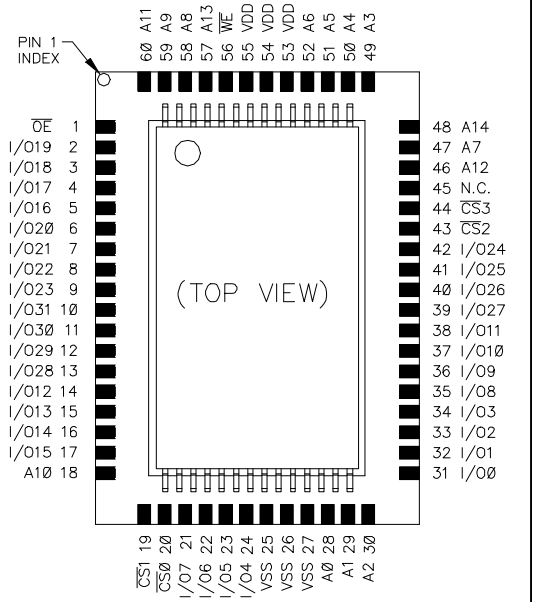
The DPS32KX32Y5 provides for a compatible upgrade path to lower density compatible modules. The module features high speed access times with common data inputs and outputs.

PIN NAMES	
A0 - A13	Address Inputs
I/O0 - I/O31	Data Input/Output
$\overline{CE}$0 - $\overline{CE}$3	Low Chip Enables
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

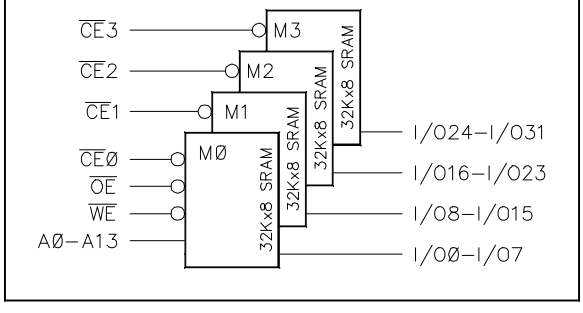
FEATURES:

- Organizations Available:
  32K x 32, 64K x 16 or 128K x 8
- Access Times: 12, 15, 20ns
- Fully Static Operation
  - No clock or refresh required
- Single +5V Power Supply, ±10% Tolerance
- TTL Compatible
- Common Data Inputs and Outputs
- Package: 60-Pin TSOP Stack

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY

RECOMMENDED OPERATING RANGE [3]						
Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage		2.2		V_{DD}+0.5	V
V_{IL}	Input LOW Voltage		-0.5[2]		0.8	V
T_A	Operating Temperature	C	0	+25	+70	°C
		CI	-40	+25	+85	

TRUTH TABLE					
Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	H	X	X	High-Z	Standby
D_{OUT} Disable	L	H	H	High-Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

H = HIGH L = LOW X = Don't Care

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	30	pF	V_{IN}[2] = 0V
C_{CE}	Chip Enable	10		
C_{WE}	Write Enable	30		
C_{OE}	Output Enable	30		
$C_{I/O}$	Data Input/Output	10		

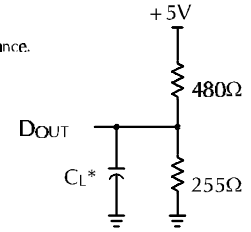
ABSOLUTE MAXIMUM RATINGS [3]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [1]	-0.5 to +7.0	°C
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD}+0.5	V

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH}= -4.0mA	2.4		V
V_{OL}	LOW Voltage	I_{OL}=8.0mA		0.4	V

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	50pF	except t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, and t_{WHZ}
2	5pF	t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, and t_{WHZ}

Figure 1. Output Load
* Including Probe and Jig Capacitance.



DC OPERATING CHARACTERISTICS: Over operating ranges						
Symbol	Characteristics	Test Conditions		Min.	Max.	Unit
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}		-8	+8	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}		-2	+2	µA
I_{CC}	Operating Supply Current	Cycle=min., Duty=100% I_{OUT} = 0mA	X8		320	mA
			X16		480	
			X32		800	
I_{SB1}	Full Standby Supply Current	$V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ +0.2V			60	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}			200	mA
V_{OL}	Output Low Voltage	I_{OUT} = 8.0mA			0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -4.0mA		2.4		V

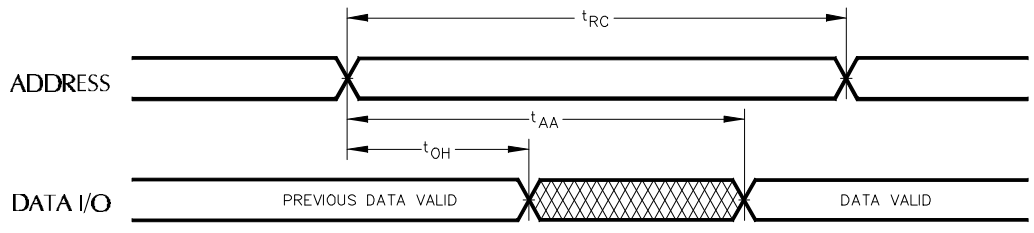
† Typical measurements made at +25°C, Cycle = min., V_{DD} = 5.0V.

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges									
No.	Symbol	Parameter	12ns		15ns		20ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	12		15		20		ns
2	t_{AA}	Address Access Time		12		15		20	ns
3	t_{CO}	$\overline{CE}$ to Output Valid		12		15		20	ns
4	t_{OE}	Output Enable to Output Valid		6		7		10	ns
5	t_{CLZ}	$\overline{CE}$ to Output in LOW-Z [4, 5]	3		3		3		ns
6	t_{OLZ}	Output Enable to Output in LOW-Z [4, 5]	0		0		0		ns
7	t_{CHZ}	$\overline{CE}$ to Output in HIGH-Z [4, 5]	0	6	0	7	0	10	ns
8	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 5]	0	6	0	7	0	8	ns
9	t_{OH}	Output Hold from Address Change	3		3		3		ns

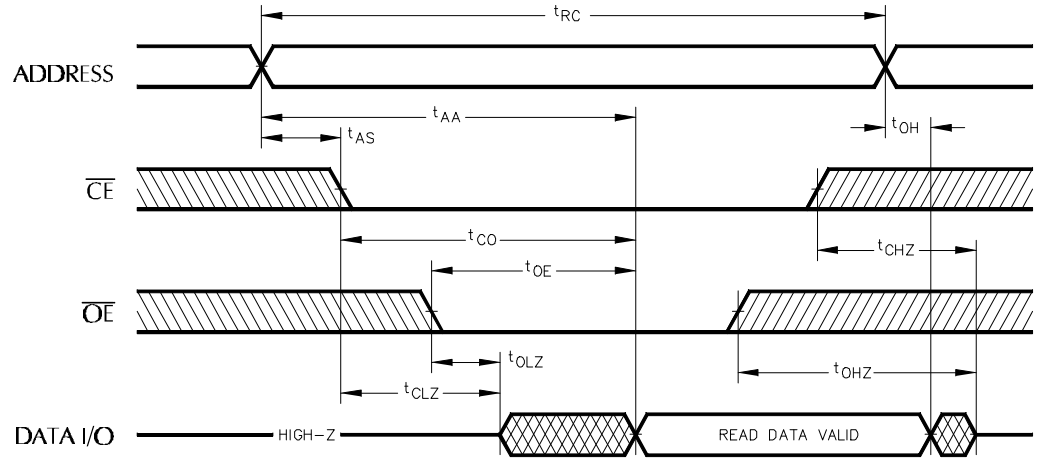
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE [6, 7]: Over operating ranges									
No.	Symbol	Parameter	12ns		15ns		20ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{WC}	Write Cycle Time	12		15		20		ns
11	t_{AW}	Address Valid to End of Write	9		12		15		ns
12	t_{CW}	Chip Enable to End of Write	9		12		15		ns
13	t_{AS}	Address Set-Up Time *	0		0		0		ns
14	t_{WP}	Write Pulse Width ($\overline{OE}$ High)	9		12		15		ns
15	t_{WP1}	Write Pulse Width ($\overline{OE}$ Low)	12		15		20		ns
16	t_{WR}	Write Recovery Time	0		0		0		ns
17	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 5]	0	6	0	8	0	8	ns
18	t_{DW}	Data to Write Time Overlap	7		8		10		ns
19	t_{DH}	Data Hold from Write Time	0		0		0		ns
20	t_{OW}	Output Active from End of Write	0		0		0		ns

* Valid for both Read and Write Cycles.

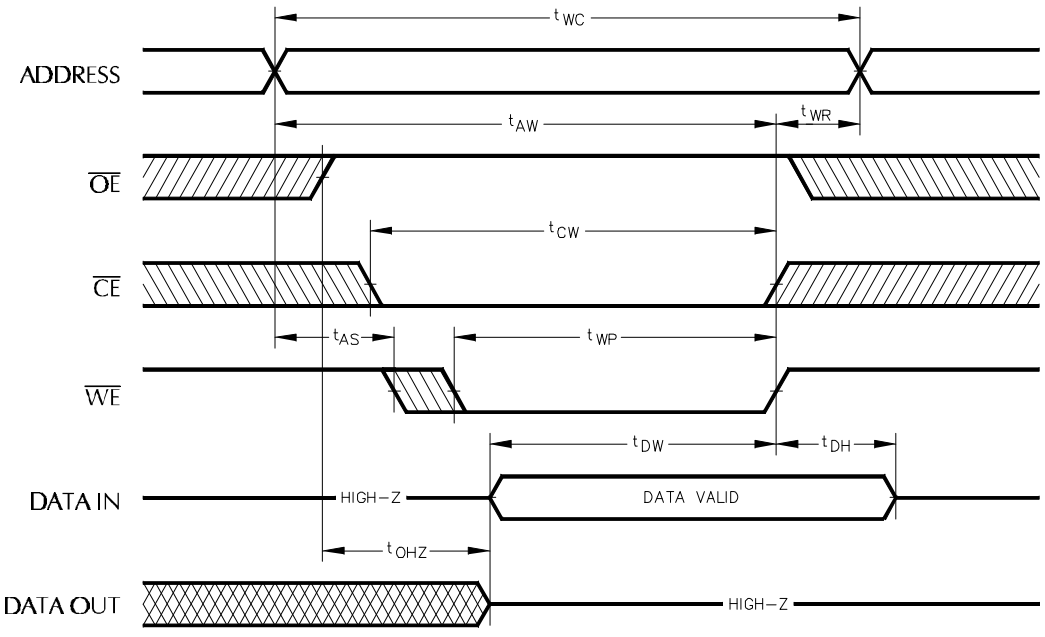
READ CYCLE 1: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ and $\overline{OE}$ are LOW.



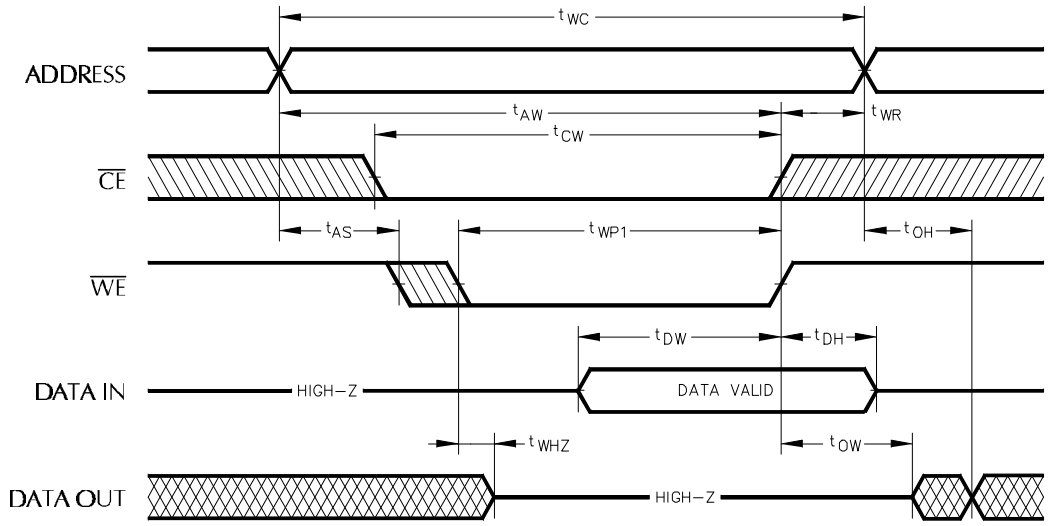
READ CYCLE 2: $\overline{CE}$ Controlled. ($\overline{WE}$ is HIGH).



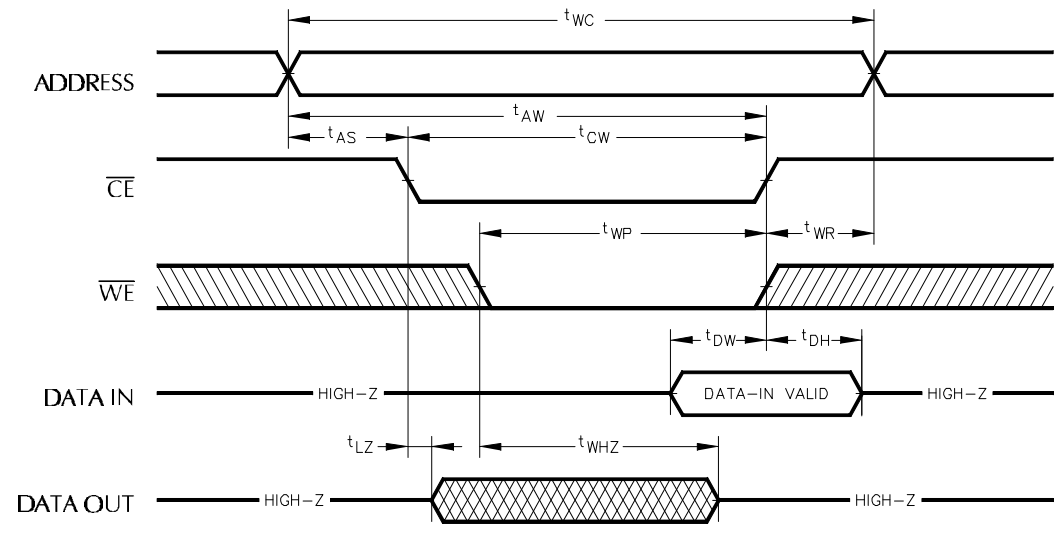
WRITE CYCLE 1: $\overline{OE}$ Clock.



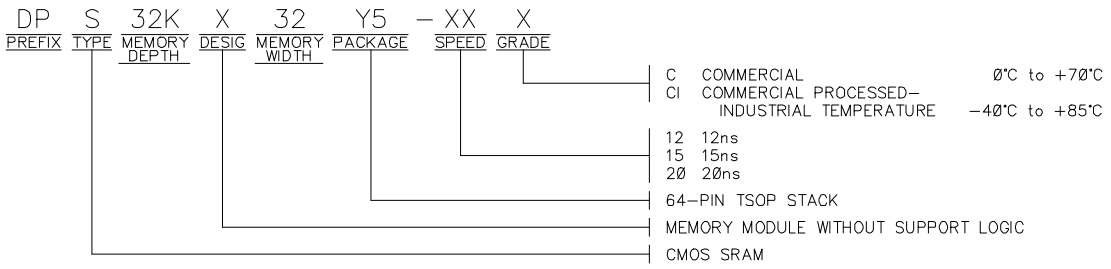
WRITE CYCLE 2: $\overline{OE}$ is LOW.



WRITE CYCLE 3: $\overline{CE}$ Controlled



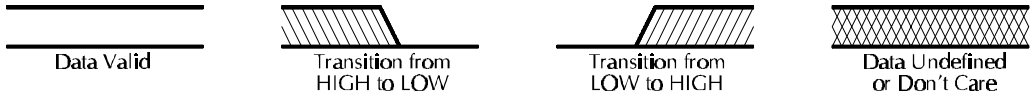
ORDERING INFORMATION



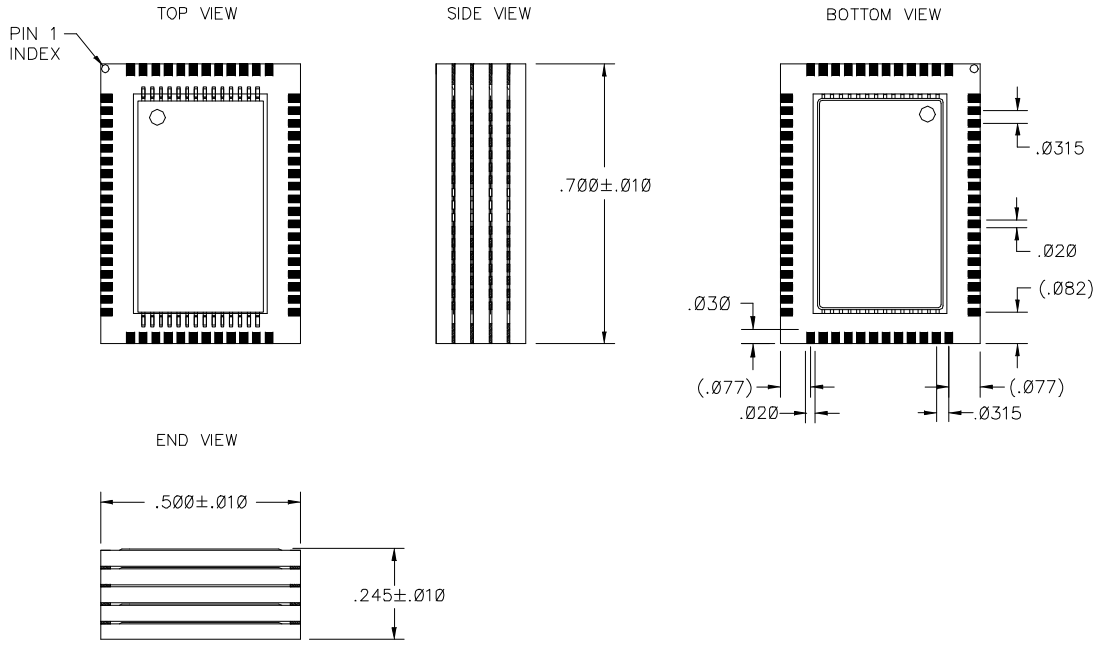
NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.
8. $\overline{CE}$ and $\overline{WE}$ can initiate and terminate WRITE Cycle.

WAVEFORM KEY



MECHANICAL DRAWING



Dense-Pac Microsystems, Inc.

7321 Lincoln Way ◆ Garden Grove, California 92841-1431

(714) 898-0007 (800) 642-4477 (Outside CA) ◆ FAX: (714) 897-1772 ◆ http://www.dense-pac.com