DENSE-PAC
MICROSYSTEMS

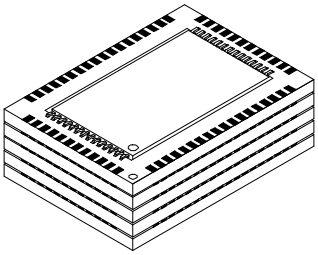
M-Densus
High Density Memory Device

4 Megabit High Speed EEPROM
DPE128X32Y5

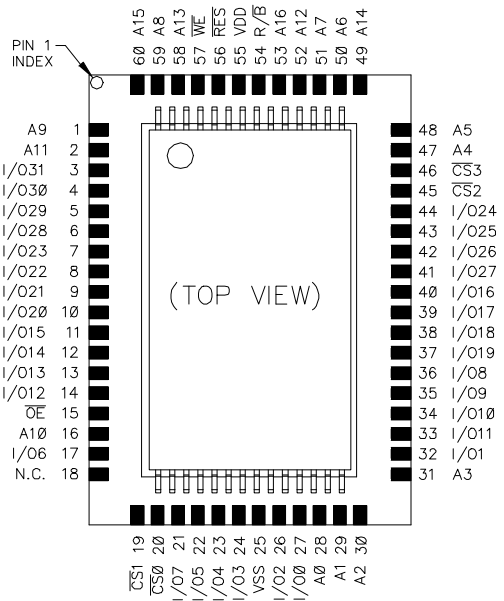
ADVANCED INFORMATION

DESCRIPTION:

The DPE128X32Y5 is a high-performance Electrically Erasable and Programmable Read Only Memory (EEPROM) module and may be organized as 128K X 32, 256K X 16 or 512K X 8.
The module is built with four low-power CMOS 128K X 8 EEPROMs. The four chip enables are used for individual BWDW* selection. The DPE128X32Y5 is ideally suited for those computer systems having 16-bit or 32-bit architectures.
The DPE128X32Y5 contains a 128-BWDW page register to allow writing of up to 128 BWDWs simultaneously. During a write cycle, the address and 1 to 128 BWDWs of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the module will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ Polling of the most significant data bit in each byte. Once the end of a write cycle has been detected, a new access for a read or write can begin.



PIN-OUT DIAGRAM



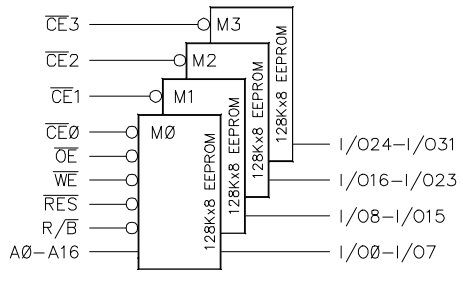
FEATURES:

- Fast Access Time: 150ns
- Organizations Available:
  128Kx32, 256Kx16 or 512Kx8
- Automatic Page Write Operation
  Internal Address and Data Latches
  Internal Control Timer
- Fast Write Cycle Times
  Page Write Cycle Time: 10ms maximum
  1 to 128 BWDW* Page Write Operation
- $\overline{\text{DATA}}$ Polling and R/$\overline{\text{B}}$ for END of Write Detection
- Write Protection by $\overline{\text{RES}}$ Pin
- High Reliability CMOS Technology
  Endurance: 10^4 Cycles (in Page Mode)
  Data Retention: 10 years
- Single +5V Power Supply, ±10% Tolerance
- CMOS and TTL Compatible Inputs and Outputs
- Package Available: 60-Pin TSOP Stack

* Byte, Word or Double Word (BWDW).

PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O31	Data Input/Output
$\overline{\text{CE}}$0 - $\overline{\text{CE}}$3	Low Chip Enables
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RES}}$	Reset
R/B	Ready/Busy
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

FUNCTIONAL BLOCK DIAGRAM



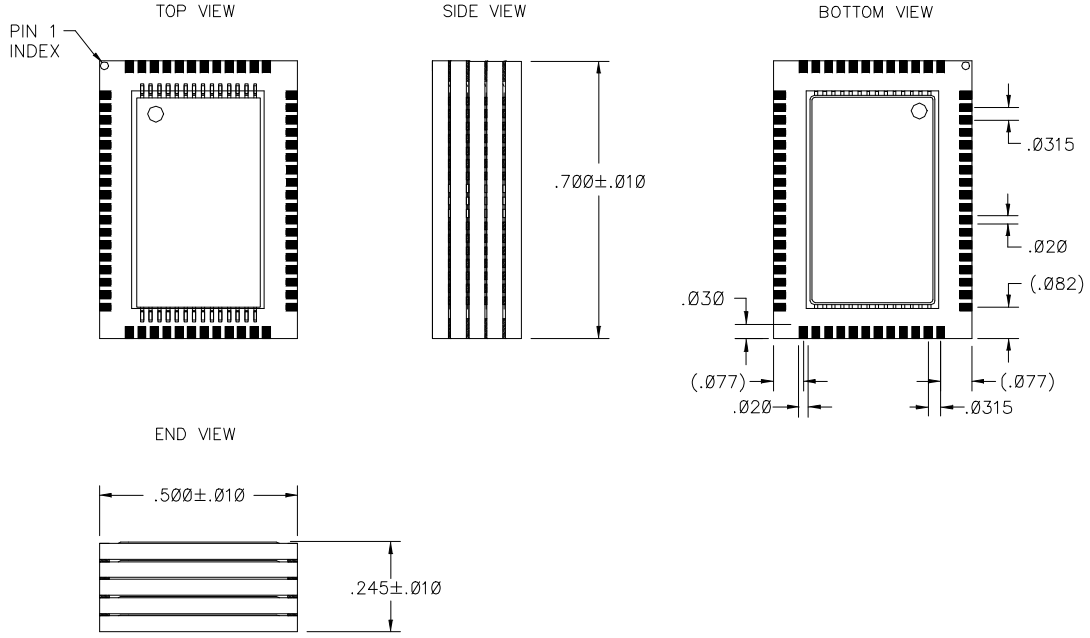
ADVANCED INFORMATION

ORDERING INFORMATION

DP	E	128	X	32	Y5	– 15	C
PREFIX	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	PACKAGE	SPEED	GRADE

- C COMMERCIAL Ø°C to +7Ø°C
- 15 15Øns
- 6Ø–PIN TSOP STACK
- MEMORY MODULE WITHOUT SUPPORT LOGIC
- CMOS EEPROM

MECHANICAL DRAWING



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