

DESCRIPTION:

The DPS1MX16MKn3 High Speed SRAM "STACK" modules are a revolutionary new memory subsystem using Dense-Pac Microsystems' ceramic Stackable Leadless Chip Carriers (SLCC). Available in straight leaded, "J" leaded or gullwing leaded packages. The module packs 16-Megabits of low-power CMOS static RAM in an area as small as 0.549 in², while maintaining a total height as low as 0.269 inches.

The DPS1MX16MKn3 STACK modules contain four individual 512K x 8 SRAMs, each packaged in a hermetically sealed SLCC, making the modules suitable for commercial, industrial and military applications.

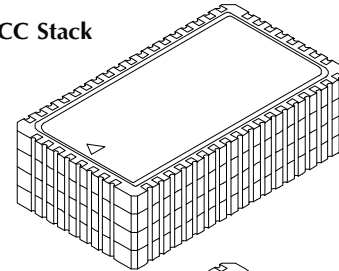
By using SLCCs, the "Stack" family of modules offer a higher board density of memory than available with conventional through-hole, surface mount or hybrid techniques.

FEATURES:

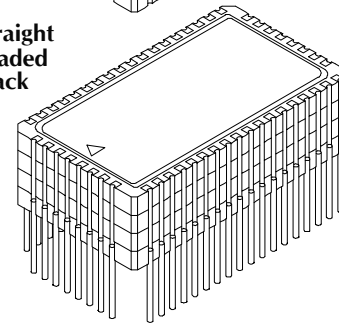
- Organizations Available:
1Meg x 16 or 2 Meg x 8
- Access Times: 20*, 25, 30, 35, 45ns
- Fully Static Operation
- No clock or refresh required
- Single +5V Power Supply, $\pm 10\%$ Tolerance
- TTL Compatible
- Common Data Inputs and Outputs
- Low Data Retention Voltage: 2.0V min.
- Packages Available:
SLCC Stack
Straight Leaded Stack
"J" Leaded Stack
Gullwing Leaded Stack

* Commercial and Industrial Grade only.

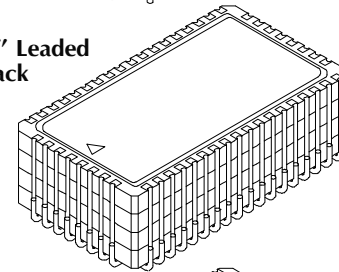
SLCC Stack



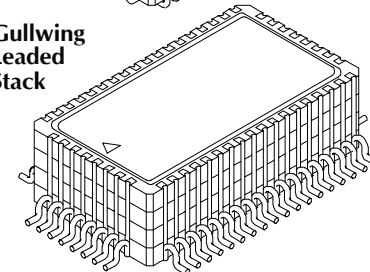
Straight Leaded Stack



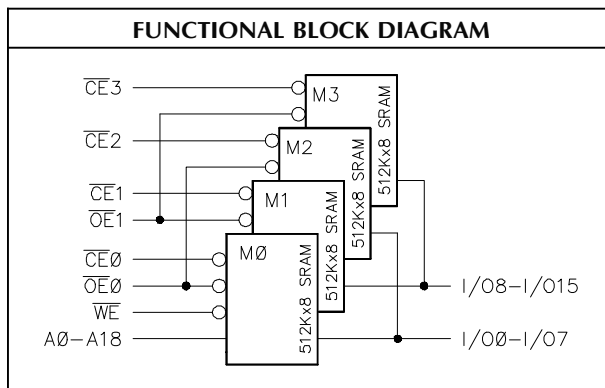
"J" Leaded Stack



Gullwing Leaded Stack

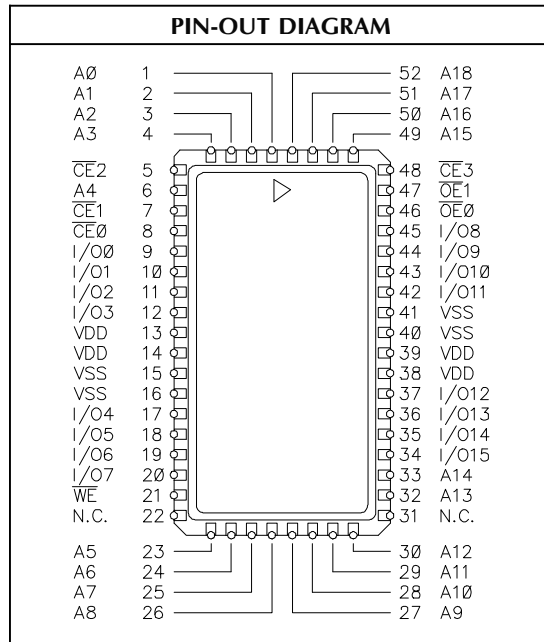


FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A0 - A18	Address Inputs
I/O0 - I/O15	Data Input/Output
$\overline{CE}0 - \overline{CE}3$	Low Chip Enables
$\overline{WE}$	Write Enable
$\overline{OE}0, \overline{OE}1$	Output Enables
V _{DD}	Power (+5V)
V _{SS}	Ground
N.C.	No Connect



CAPACITANCE ⁴ : T _A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C _{ADR}	Address Input	40	pF	V _{IN} ² = 0V
C _{CE}	Chip Enable	16		
C _{WE}	Write Enable	40		
C _{OE}	Output Enable	25		
C _{I/O}	Data Input/Output	25		

TRUTH TABLE					
Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	H	X	X	High-Z	Standby
DOUT Disable	L	H	H	High-Z	Active
Read	L	H	L	DOUT	Active
Write	L	L	X	DIN	Active

H = HIGH

L = LOW

X = Don't Care

ABSOLUTE MAXIMUM RATINGS ³			
Symbol	Parameter	Value	Unit
T _{STC}	Storage Temperature	-65 to +150	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
V _{DD}	Supply Voltage ¹	-0.5 to +7.0	°C
V _{I/O}	Input/Output Voltage ¹	-0.5 to V _{DD} + 0.5	V

RECOMMENDED OPERATING RANGE ³					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input HIGH Voltage	2.2		V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage	-0.5 ²		0.8	V
T _A	Operating Temperature	M/B	-55	+25	+125
		I	-40	+25	+85
		C	0	+25	+70

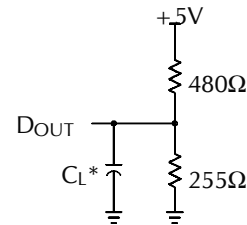
DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{OH}	HIGH Voltage	I _{OH} = -4.0mA	2.4		V
V _{OL}	LOW Voltage	I _{OL} = 8.0mA		0.4	V

DC OPERATING CHARACTERISTICS: Over operating ranges											
Symbol	Characteristics	Test Conditions		Typ. (†)	C		I		M/B		Unit
					Min.	Max.	Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = 0V to V _{DD}		-	-20	+20	-20	+20	-20	+20	μA
I _{OUT}	Output Leakage Current	V _{I/O} = 0V to V _{DD} , CE or OE = V _{IH} , or $\overline{WE}$ = V _{IL}		-	-20	+20	-20	+20	-20	+20	μA
I _{CC}	Operating Supply Current	Cycle = min., Duty = 100% I _{OUT} = 0mA	X8	185		350		360		36.0	mA
			X16	290		460		480		480	
I _{SB1}	Full Standby Supply Current	V _{IN} ≥ V _{DD} -0.2V or V _{IN} ≤ V _{SS} +0.2V		4		40		40		60	mA
I _{SB2}	Standby Current (TTL)	$\overline{CE}$ = V _{IH}		80		240		240		240	mA
I _{DR3}	Data Retention Supply Current (3.0V)	V _{DR} = 3.0V, $\overline{CE}$ ≥ V _{DR} -0.2V		0.6		2.0		4.0		8.0	mA
I _{DR2}	Data Retention Supply Current (2.0V)	V _{DR} = 2.0V, $\overline{CE}$ ≥ V _{DR} -0.2V		0.4		1.2		3.2		7.2	mA
V _{OL}	Output Low Voltage	I _{OUT} = 8.0mA		-		0.4		0.4		0.4	V
V _{OH}	Output High Voltage	I _{OUT} = -4.0mA		-	2.4		2.4		2.4		V

† Typical measurements made at +25°C, Cycle = min., V_{DD} = 5.0V.

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V

Figure 1. Output Load



OUTPUT LOAD		
Load	CL	Parameters Measured
1	100pF	except tLZ, tHZ, tOHZ, tOLZ, and tWHZ
2	5pF	tLZ, tHZ, tOHZ, tOLZ, and tWHZ

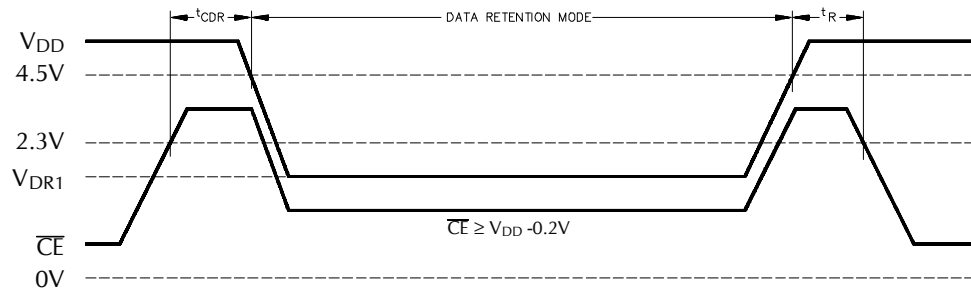
Data Retention AC Characteristics ⁸						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{DR}	V _{DD} for Data Retention	$\overline{CE} \geq V_{DR} - 0.2V$	2.0	-	-	V
V _{CDR}	Chip Disable to Data Retention Time	See Data Retention Waveform	0	-	-	ns
t _R	Operation Recovery Time	See Data Retention Waveform	5	-	-	ms

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	20ns*		25ns		30ns		35ns		45ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{RC}	Read Cycle Time	20		25		30		35		45		ns
2	t _{AA}	Address Access Time		20		25		30		35		45	ns
3	t _{CO}	$\overline{CE}$ to Output Valid		20		25		30		35		45	ns
4	t _{OE}	Output Enable to Output Valid		10		12		15		20		25	ns
5	t _{LZ}	$\overline{CE}$ to Output in LOW-Z ^{4, 5}	3		3		3		3		3		ns
6	t _{OLZ}	Output Enable to Output in LOW-Z ^{4, 5}	0		0		0		0		0		ns
7	t _{HZ}	$\overline{CE}$ to Output in HIGH-Z ^{4, 5}		8		10		15		20		25	ns
8	t _{OHZ}	Output Enable to Output in HIGH-Z ^{4, 5}	0	8	0	10	0	15	0	20	0	25	ns
9	t _{OH}	Output Hold from Address Change	4		5		5		5		5		ns

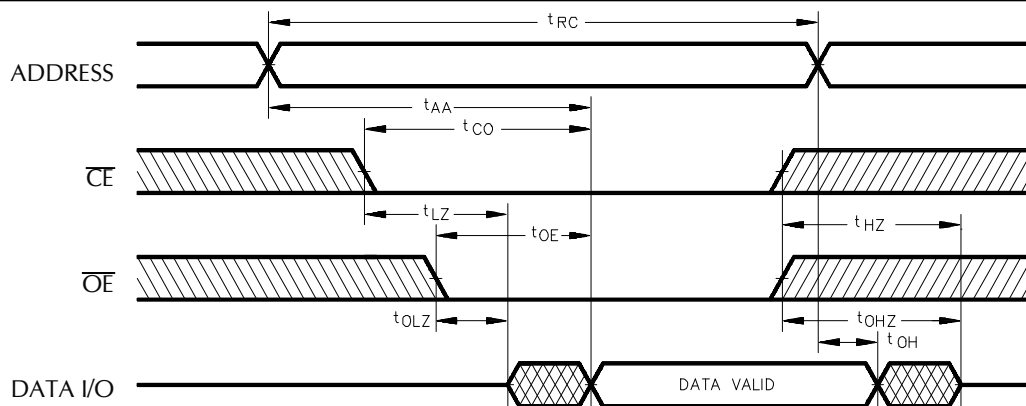
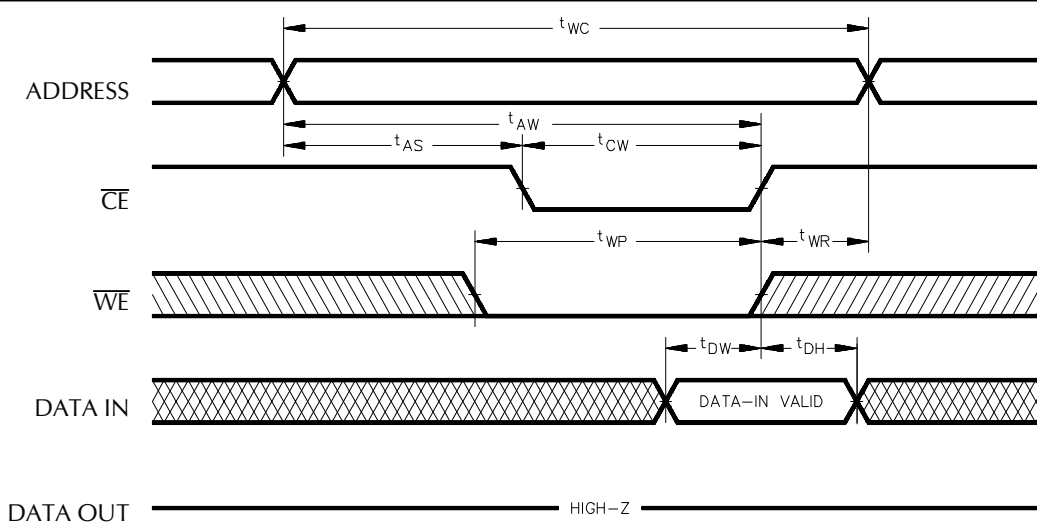
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE ^{6,7} : Over operating ranges													
No.	Symbol	Parameter	20ns*		25ns		30ns		35ns		45ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t _{WC}	Write Cycle Time	20		25		30		35		45		ns
11	t _{AW}	Address Valid to End of Write	13		15		20		25		35		ns
12	t _{CW}	Chip Enable to End of Write	13		15		20		25		35		ns
13	t _{AS}	Address Set-Up Time **	0		0		0		0		0		ns
14	t _{WP}	Write Pulse Width	13		15		20		25		35		ns
15	t _{WR}	Write Recovery Time	0		0		0		0		0		ns
16	t _{WHZ}	Write Enable to Output in HIGH-Z ^{4, 5}	0	8	0	10	0	12	0	15	0	20	ns
17	t _{DW}	Data to Write Time Overlap	9		10		12		15		20		ns
18	t _{DH}	Data Hold from Write Time	0		0		0		0		0		ns
19	t _{OW}	Output Active from End of Write	3		3		3		3		3		ns

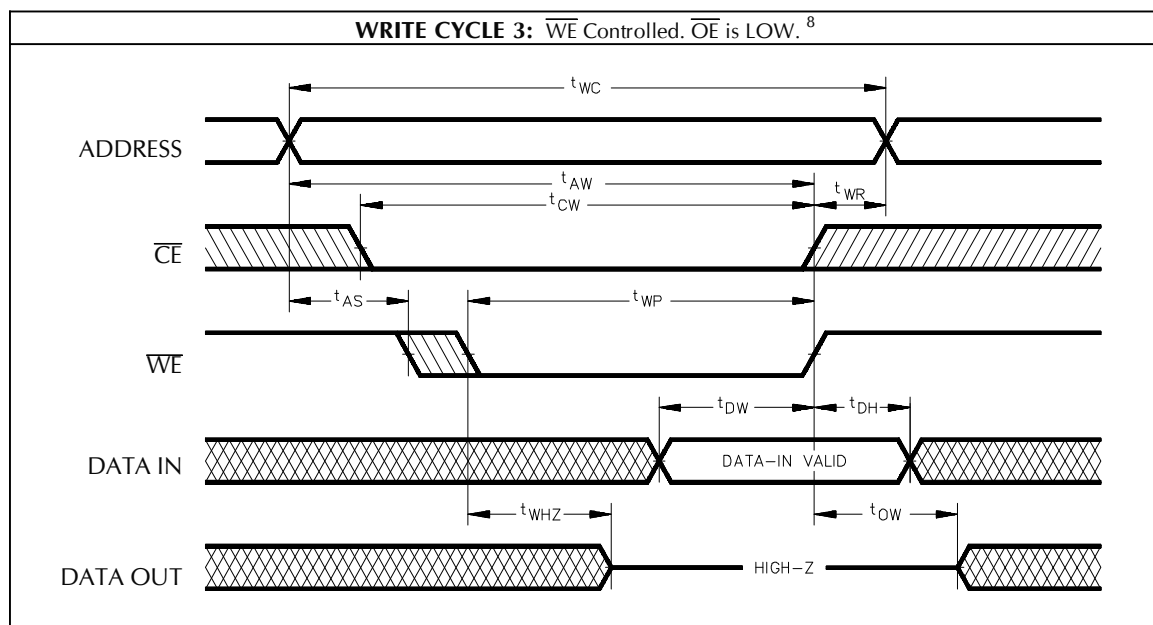
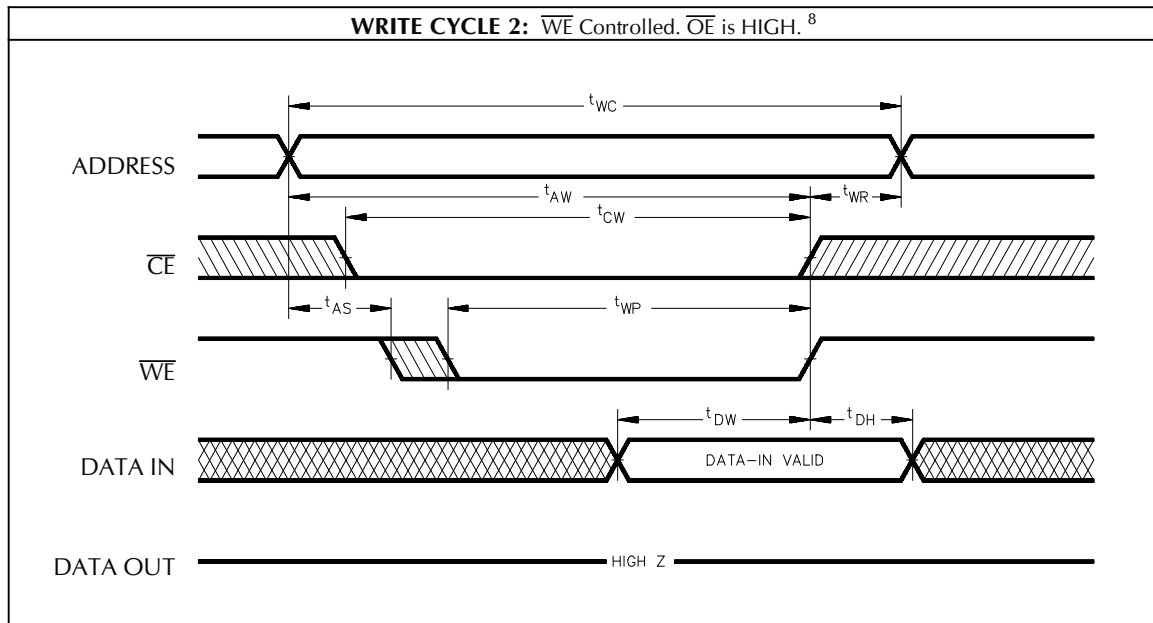
* Available in Commercial and Industrial Grade Only.

** Valid for both Read and Write Cycles.

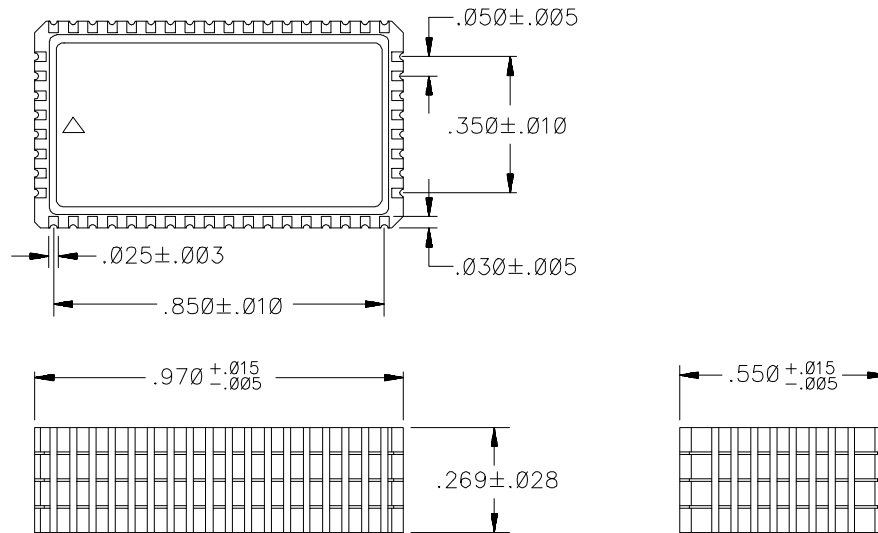
DATA RETENTION WAVEFORM: $\overline{CE}$ Controlled.

READ CYCLE

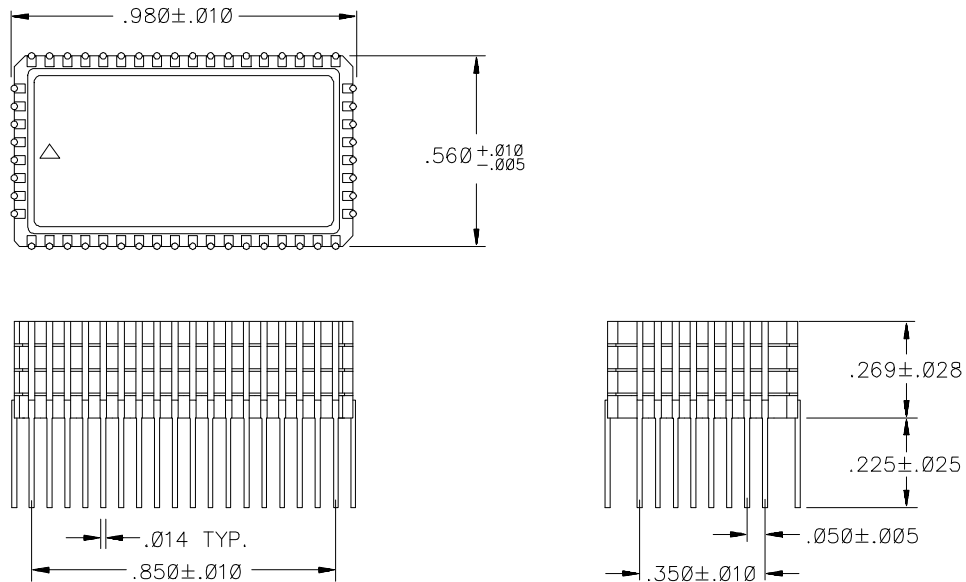
WRITE CYCLE 1: $\overline{CE}$ Controlled.



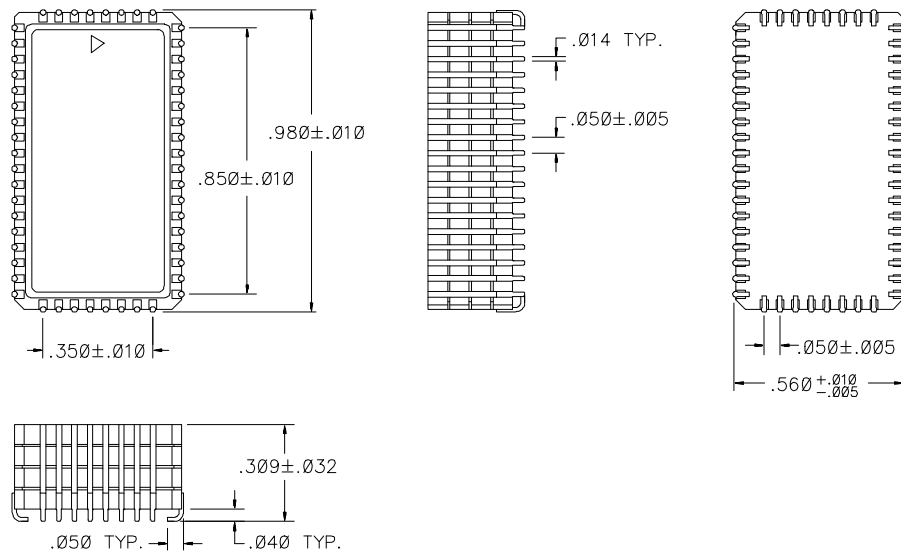
(52 - PIN LEADLESS STACK) MECHANICAL DRAWING



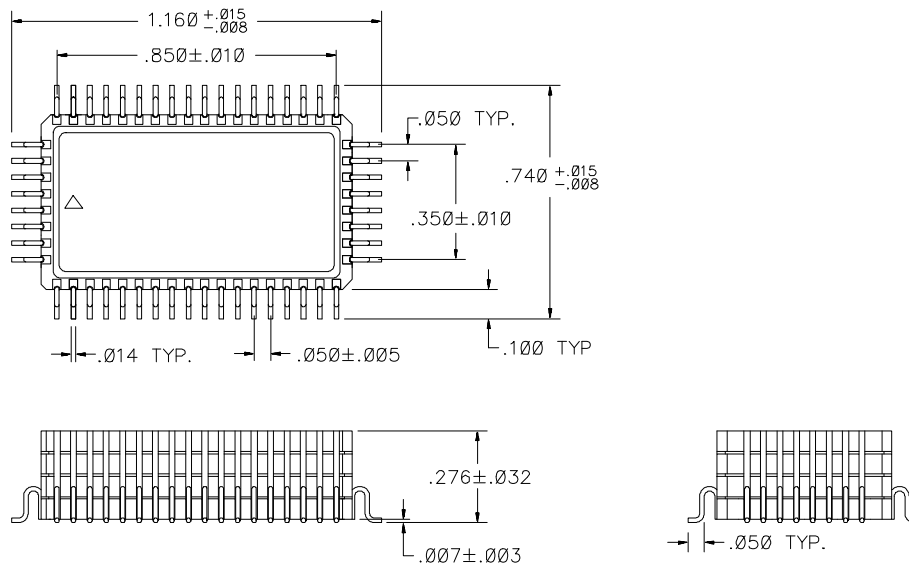
(52 - PIN STRAIGHT LEADED STACK) MECHANICAL DRAWING



(52 - PIN "J" LEADED STACK) MECHANICAL DRAWING



(52 - PIN GULLWING LEADED STACK) MECHANICAL DRAWING



ORDERING INFORMATION									
DP	S	1M	X	16	MK	X3	— XX	X	
PREFIX	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	DESIG.	PACKAGE	SPEED	GRADE	
									C COMMERCIAL 0°C to +70°C
									I INDUSTRIAL -40°C to +85°C
									M MILITARY -55°C to +125°C
									B MIL-PROCESSED -55°C to +125°C
									20 20ns ("C" & "I" GRADE ONLY)
									25 25ns
									30 30ns
									35 35ns
									45 45ns
									H3 GULLWING LEADED SLCC STACK
									I3 THRU-HOLE LEADED SLCC STACK
									J3 "J" LEADED SLCC STACK
									Y3 LEADLESS SLCC STACK
									4 MEGABIT / SPECIAL PACKAGE
									MODULE WITHOUT SUPPORT LOGIC
									CMOS SRAM DEVICES

NOTES:

1. All voltages are with respect to V_{SS} .
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ± 500 mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.
8. $\overline{CE}$ and $\overline{WE}$ can initiate and terminate WRITE Cycle.

WAVEFORM KEY			
Data Valid	Transition from HIGH to LOW	Transition from LOW to HIGH	Data Undefined or Don't Care

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