**DENSE-PAC**
MICROSYSTEMS

# *M-Densus*
## High Density Memory Device

**512 Megabit CMOS 3.3V EDO DRAM**
**256 Megabit CMOS 3.3V EDO DRAM**
**128 Megabit CMOS 3.3V EDO DRAM**

PRELIMINARY

**DESCRIPTION:**

The ***M-Densus*** series is a family of interchangeable memory modules. The 64 Megabit DRAM is a member of this family which utilizes the new and innovative space saving TSOP technology. The modules are constructed with 16 Meg x 4 EDO, 3.3 Volt DRAM's available in 512, 256 and 128 Megabits.

The 64 Megabit based ***M-Densus*** modules have been designed to fit in the same footprint as the 16 Meg x 4 DRAM TSOP monolithic and are backward compatible with the 16 Megabit based family of ***M-Densus*** modules. This allows the memory board designer to upgrade the memory in their products without redesigning the memory board, thus saving time and money.

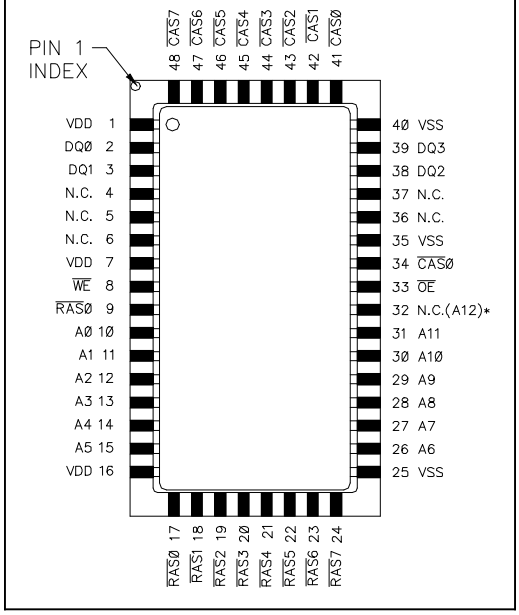
**FEATURES:**

- Configurations Available:
  - 128 Megabit: 32 Meg x 4
  - 256 Megabit: 64 Meg x 4
  - 512 Megabit: 128 Meg x 4
- Access Times: 50, 60, 70ns (max.)
- 3.3 Volt Supply
- Common Data Inputs and Outputs
- Extended Data Out Capability (EDO)
- 4K/8K 64ms Refresh
- 3 Variations of Refresh:
  - $\overline{RAS}$ only Refresh
  - $\overline{CAS}$ before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Package: Leadless TSOP Module

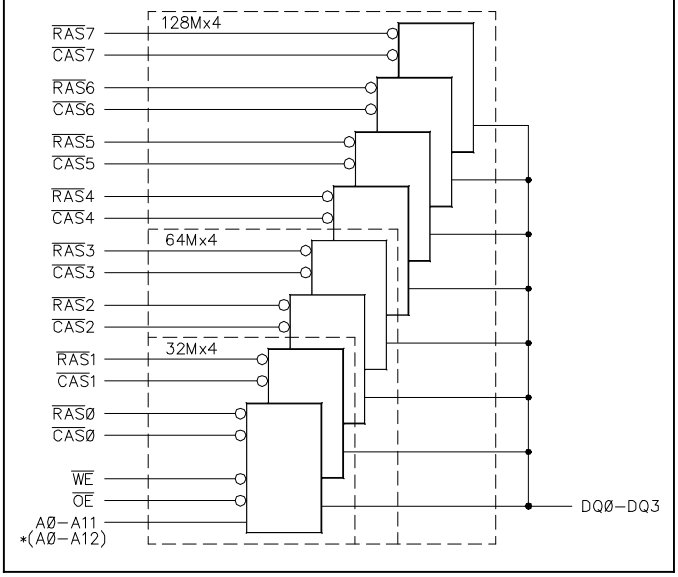
| PIN NAMES | |
|---|---|
| A0 - A11 | Row Address: A0 - A11<br>Column Address: A0 - A11<br>Refresh Address: A0 - A11 |
| A0 - A12* | Row Address: A0 - A12<br>Column Address: A0 - A10<br>Refresh Address: A0 - A12 |
| DQ0 - DQ3 | Data In / Data Out |
| $\overline{CAS}$0 - $\overline{CAS}$7 | Column Address Strobes |
| $\overline{RAS}$0 - $\overline{RAS}$7 | Row Address Enables |
| $\overline{WE}$ | Data Write Enable |
| $\overline{OE}$ | Data Output Enable |
| $V_{DD}$ | Power Supply (+3.3V) |
| $V_{SS}$ | Ground |
| N.C. | No Connect |

* A12 for 8K refresh device.

**PIN-OUT DIAGRAM**




**FUNCTIONAL BLOCK DIAGRAM**



PRELIMINARY

| ABSOLUTE MAXIMUM RATINGS | | | |
|---|---|---|---|
| Symbol | Parameter | Value | Units |
| $T_{STC}$ | Storage Temperature | -55 to +150 | °C |
| $V_{I/O}$ | Voltage on Any Pin | -0.5 to +6.5 | V |
| $V_{DD}$ | $V_{DD}$ Supply Voltage | -0.5 to +4.6 | V |
| $I_{OUT}$ | Output Current | 50 | mA |

* -1.3V at pulse width ≤ 15ns which is measured at $V_{DD}$.
** 6.5V at pulse width ≤ 15ns which is measured at $V_{DD}$.

| RECOMMENDED OPERATING CONDITIONS | | | | | |
|---|---|---|---|---|---|
| Symbol | Parameter | Min. | Typ. | Max. | Units |
| $V_{DD}$ | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| $V_{IL}$ | Input Low Voltage | -0.3* | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | 2.0 | | +5.5** | V |
| $T_A$ | Operating Temperature | 0 | +25 | +70 | °C |

NOTE: All voltages referenced to $V_{SS}$.

| CAPACITANCE: $t_A$ = 25°C, f = 1MHz | | | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | 32Mx4 | 64Mx4 | 128Mx4 | Unit | Condition |
| $C_{ADR}$ | Address Input | 12 | 25 | 45 | pF | $V_{IN}$ = 0V |
| $C_{CAS}$ | $\overline{CAS}$ Input | 8 | 10 | 12 | | |
| $C_{RAS}$ | $\overline{RAS}$ Input | 8 | 10 | 12 | | |
| $C_{WE}$ | Write Enable | 15 | 30 | 60 | | |
| $C_{OE}$ | Output Enable | 15 | 30 | 60 | | |
| $C_{I/O}$ | Data Input/Output | 15 | 30 | 60 | | |

| DC INPUT/OUTPUT CHARACTERISTICS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristic | Conditions | 32Mx4 | | 64Mx4 | | 128Mx4 | | Units |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $I_{IN}$ | Input Leakage Current | $\overline{CAS}$, $\overline{RAS}$ | -5 | +5 | -5 | +5 | -5 | +5 | µA |
| | | A0-A11, $\overline{WE}$, $\overline{OE}$ | -10 | +10 | -20 | +20 | -40 | +40 | |
| $I_{OUT}$ | Output Leakage Current | | -10 | +10 | -20 | +20 | -40 | +40 | µA |
| $V_{OL}$ | Output Low Voltage | IOL = 4.2mA | | 0.4 | | 0.4 | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | IOH = -5mA | 2.4 | | 2.4 | | 2.4 | | V |

| DC OPERATING CHARACTERISTICS | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristic | Conditions | | MAXIMUM | | | | | | Units |
| | | | | 50ns | | 60ns | | 70ns | | |
| | | | | 4K | 8K | 4K | 8K | 4K | 8K | |
| $I_{CC1}$ | Operating Current | $\overline{RAS}$ and $\overline{CAS}$ cycling @ $t_{RC}$ = min. | 32Mx4 | 152 | 102 | 142 | 92 | 132 | 82 | mA |
| | | | 64Mx4 | 156 | 106 | 146 | 96 | 136 | 86 | |
| | | | 128Mx4 | 164 | 114 | 154 | 104 | 144 | 94 | |
| $I_{CC2}$ | Standby Current | $\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = $V_{IH}$ | 32Mx4 | 4 | 4 | 4 | 4 | 4 | 4 | mA |
| | | | 64Mx4 | 8 | 8 | 8 | 8 | 8 | 8 | |
| | | | 128Mx4 | 16 | 16 | 16 | 16 | 16 | 16 | |
| $I_{CC3}$* | $\overline{RAS}$ - Only Refresh Current | $\overline{CAS}$ = $V_{IH}$, $\overline{RAS}$ Cycling @ $t_{RC}$ = min. | 32Mx4 | 152 | 102 | 142 | 92 | 132 | 82 | mA |
| | | | 64Mx4 | 156 | 106 | 146 | 96 | 136 | 86 | |
| | | | 128Mx4 | 164 | 114 | 154 | 104 | 144 | 94 | |
| $I_{CC4}$ | FAST-PAGE-MODE Current | $\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$, Address Cycling @ $t_{PC}$ = min. | 32Mx4 | 82 | 72 | 72 | 62 | 67 | 57 | mA |
| | | | 64Mx4 | 86 | 76 | 76 | 66 | 71 | 61 | |
| | | | 128Mx4 | 94 | 84 | 84 | 74 | 49 | 69 | |
| $I_{CC5}$ | Standby Current | $\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = $V_{DD}$ -2.0V | 32Mx4 | 2 | 2 | 2 | 2 | 2 | 2 | mA |
| | | | 64Mx4 | 4 | 4 | 4 | 4 | 4 | 4 | |
| | | | 128Mx4 | 8 | 8 | 8 | 8 | 8 | 8 | |
| $I_{CC6}$*** | $\overline{CAS}$ - Before - $\overline{RAS}$ Refresh Current | $\overline{RAS}$ and $\overline{CAS}$ Cycling @ $t_{RC}$ = min. | 32Mx4 | 152 | 152 | 142 | 142 | 132 | 132 | mA |
| | | | 64Mx4 | 156 | 156 | 146 | 146 | 136 | 136 | |
| | | | 128Mx4 | 164 | 164 | 154 | 154 | 144 | 144 | |

*** Assumes distributed refresh.

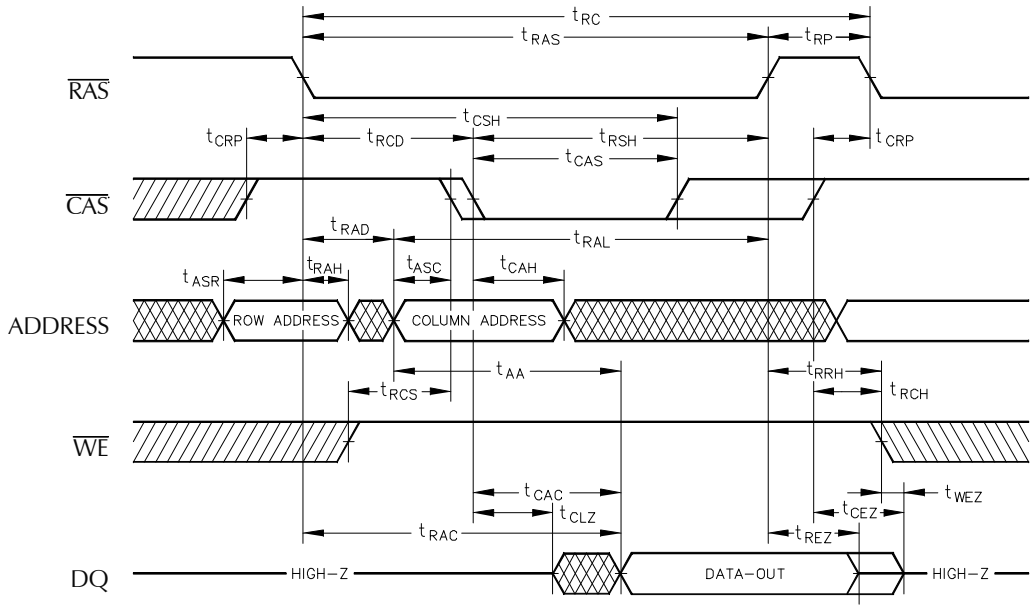
| A.C. OPERATING AND CHARACTERISTICS ($V_{CC}$ = 3.3V ± 0.3V, $T_A$ = 0°C to 70°C) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| No. | Symbol | Parameter | 50ns | | 60ns | | 70ns | | Unit |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| 1 | $t_{RC}$ | Random Read or Write Cycle Time | 90 | | 110 | | 125 | | ns |
| 2 | $t_{RAC}$ | Access Time from $\overline{RAS}$ [3, 4, 10] | | 50 | | 60 | | 70 | ns |
| 3 | $t_{CAC}$ | Access Time from $\overline{CAS}$ [3, 4, 5] | | 13 | | 15 | | 20 | ns |
| 4 | $t_{AA}$ | Access Time from Column Address [3, 10] | | 25 | | 30 | | 35 | ns |
| 5 | $t_{CLZ}$ | $\overline{CAS}$ to Output in LOW-Z [3] | 3 | | 3 | | 3 | | ns |
| 6 | $t_{CEZ}$ | Output Buffer Turn-Off Delay From $\overline{CAS}$ [6,12] | 3 | 13 | 3 | 13 | 3 | 15 | ns |
| 7 | $t_T$ | Transition Time (rise and fall) [2] | 1 | 50 | 1 | 50 | 1 | 50 | ns |
| 8 | $t_{RP}$ | $\overline{RAS}$ Precharge Time | 30 | | 40 | | 50 | | ns |
| 9 | $t_{RAS}$ | $\overline{RAS}$ Pulse Width | 50 | 10,000 | 60 | 10,000 | 70 | 10,000 | ns |
| 10 | $t_{RSH}$ | $\overline{RAS}$ Hold Time | 13 | | 15 | | 20 | | ns |
| 11 | $t_{CSH}$ | $\overline{CAS}$ Hold Time | 38 | | 45 | | 55 | | ns |
| 12 | $t_{CAS}$ | $\overline{CAS}$ Pulse Width [4] | 8 | 10,000 | 15 | 10,000 | 15 | 10,000 | ns |
| 13 | $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ Delay Time [9] | 20 | 37 | 20 | 45 | 20 | 50 | ns |
| 14 | $t_{RAD}$ | $\overline{RAS}$ to Column Address Delay Time | 15 | 25 | 15 | 30 | 15 | 35 | ns |
| 15 | $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | 5 | | 5 | | 5 | | ns |
| 16 | $t_{ASR}$ | Row Address Setup Time | 0 | | 0 | | 0 | | ns |
| 17 | $t_{RAH}$ | Row Address Hold Time | 10 | | 10 | | 10 | | ns |
| 18 | $t_{ASC}$ | Column Address Setup Time | 0 | | 0 | | 0 | | ns |
| 19 | $t_{CAH}$ | Column Address Hold Time | 8 | | 10 | | 15 | | ns |
| 20 | $t_{RAL}$ | Column Address to $\overline{RAS}$ Lead Time | 25 | | 30 | | 40 | | ns |
| 21 | $t_{RCS}$ | Read Command Setup Time | 0 | | 0 | | 0 | | ns |
| 22 | $t_{RCH}$ | Read Command Hold Time Referenced to $\overline{CAS}$ [8] | 0 | | 0 | | 0 | | ns |
| 23 | $t_{RRH}$ | Read Command Hold Time Referenced to $\overline{RAS}$ [8] | 0 | | 0 | | 0 | | ns |
| 24 | $t_{WCH}$ | Write Command Hold Time | 10 | | 10 | | 15 | | ns |
| 25 | $t_{WP}$ | Write Command Pulse Width | 10 | | 10 | | 15 | | ns |
| 26 | $t_{RWL}$ | Write Command to $\overline{RAS}$ Lead Time | 13 | | 15 | | 25 | | ns |
| 27 | $t_{CWL}$ | Write Command to $\overline{CAS}$ Lead Time | 8 | | 10 | | 20 | | ns |
| 28 | $t_{DS}$ | Data-In Setup Time [9] | 0 | | 0 | | 0 | | ns |
| 29 | $t_{DH}$ | Data-In Hold Time [9] | 8 | | 10 | | 20 | | ns |
| 30 | $t_{REF}$ | Refresh Period | | 64 | | 64 | | 64 | ms |
| 31 | $t_{WCS}$ | Write Command Setup Time [7] | 0 | | 0 | | 0 | | ns |
| 32 | $t_{CSR}$ | $\overline{CAS}$ Set Up time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh) | 5 | | 5 | | 10 | | ns |
| 33 | $t_{CHR}$ | $\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh) | 10 | | 10 | | 15 | | ns |
| 34 | $t_{RPC}$ | $\overline{RAS}$ to $\overline{CAS}$ precharge time | 5 | | 5 | | 5 | | ns |
| 35 | $t_{CPA}$ | Access time From $\overline{CAS}$ Precharge [3] | | 28 | | 35 | | 40 | ns |
| 36 | $t_{HPC}$ | Hyper Page Cycle Time [11] | 25 | | 30 | | 35 | | ns |

| A.C. OPERATING AND CHARACTERISTICS ($V_{DD}$ = 5.0V±10%, $T_A$ = 0°C to 70°C) (Continued) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| No. | Symbol | Parameter | 50ns | | 60ns | | 70ns | | Unit |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| 37 | $t_{CP}$ | $\overline{CAS}$ Precharge Time (Hyper Page Cycle) | 8 | | 10 | | 10 | | ns |
| 38 | $t_{CACP}$ | Access Time from $\overline{CAS}$ (Hyper Page Cycle) [3] | | 15 | | 15 | | 15 | ns |
| 39 | $t_{AAP}$ | Access Time from Column Address (Hyper Page Cycle)[3] | | 25 | | 30 | | 35 | ns |
| 40 | $t_{RASP}$ | $\overline{RAS}$ Pulse Width (Hyper Page Cycle) | 50 | 200,000 | 60 | 200,000 | 70 | 200,000 | µs |
| 41 | $t_{RHCP}$ | $\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge | 30 | | 35 | | 40 | | ns |
| 42 | $t_{WRP}$ | $\overline{WE}$ to $\overline{RAS}$ Precharge time ($\overline{C}$-B-$\overline{R}$ Refresh) | 10 | | 10 | | 10 | | ns |
| 43 | $t_{WRH}$ | $\overline{WE}$ to $\overline{RAS}$ Hold Time ($\overline{C}$-B-$\overline{R}$ Refresh) | 10 | | 10 | | 10 | | ns |
| 44 | $t_{DOH}$ | Output Data Hold Time | 5 | | 5 | | 5 | | ns |
| 45 | $t_{REZ}$ | Output Buffer Turn Off Delay From $\overline{RAS}$ [6, 12] | 3 | 13 | 3 | 15 | 3 | 20 | ns |
| 46 | $t_{WEZ}$ | Output Buffer Turn Off Delay From $\overline{WE}$ [6] | 3 | 13 | 3 | 15 | 3 | 20 | ns |
| 47 | $t_{WED}$ | $\overline{WE}$ to Data Delay | 15 | | 15 | | 20 | | ns |
| 48 | $t_{WPE}$ | $\overline{WE}$ Pulse Width (Hyper Page Cycle) | 5 | | 5 | | 5 | | ns |

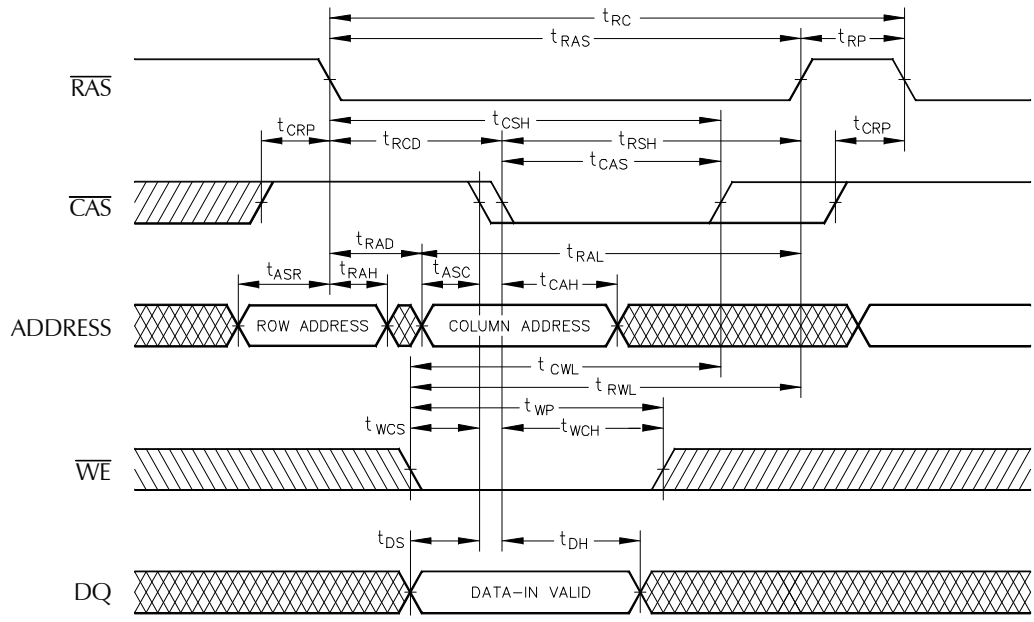
NOTES:

1. An initial pause of 200µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper operation is assured.
2. $V_{IH}$ (min.) and $V_{IL}$ (max.) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ (min.) and $V_{IL}$ (max.) and are assumes to be 5ns for all inputs.
3. Measured with the load equivalent to (2) two TTL load and 100pF.
4. Operation within the $t_{RCD}$ (max.) limit ensures that $t_{RAC}$ (max.) and can be met. $t_{RCD}$ (max.) is specified as a reference point only. If $t_{RCD}$ is greater than the specified $t_{RCD}$ (max.) limit, then access time is controlled exclusively by $t_{CAC}$.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max.).
6. This parameter defines the time at which the output achieves the open circuit conditions and is not referenced to $V_{OL}$ or $V_{OH}$.
7. $t_{WCS}$, $t_{RWC}$, $t_{CWD}$ and $t_{AWD}$ are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{AWD}$ (min), the cycles is an early write cycle and the data output will remain high impedancefor the duration of the cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the $t_{RAD}$ (max) limit insures that $t_{RAC}$ (max) can be met. $t_{RAD}$(max) is specified as a reference point only. If $t_{RAD}$ is greater than the specified $t_{RAD}$ (max) limit, then access time is controlled by $t_{AA}$.
11. $t_{CEZ}$ (max), $t_{REZ}$ (max) and $t_{OEZ}$ (max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
12. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the ouput is achieved by $\overline{RAS}$ high going.
13. $t_{ASC} \geq 6$ns. Assume $t_T = 2.0$ns
14. It can get less $\overline{CAS}$ before $\overline{RAS}$ current loss if $t_{CHR} \geq t_{RAS}$ or $\overline{CAS} \leq 0.2$V at $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

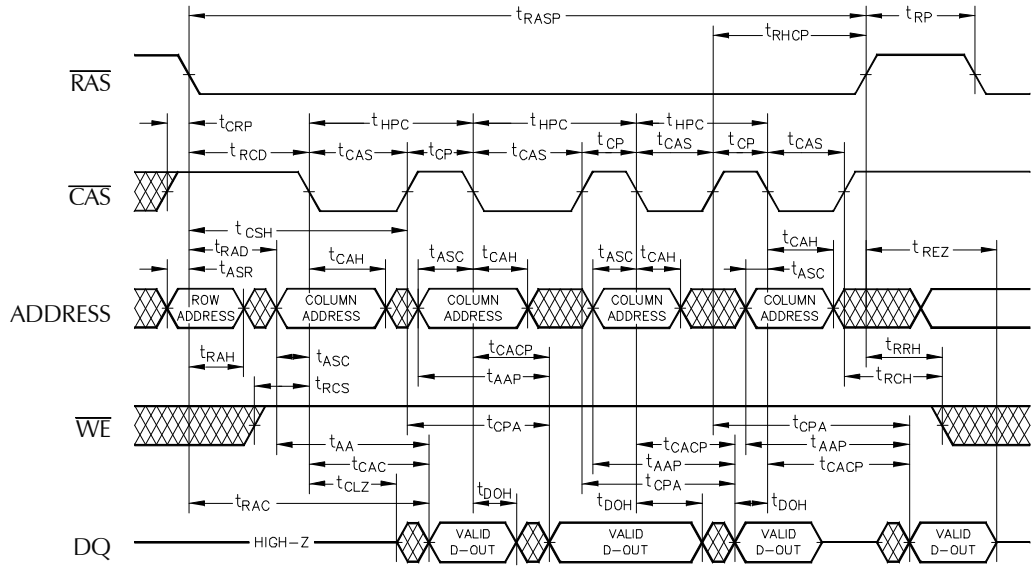
**READ CYCLE**



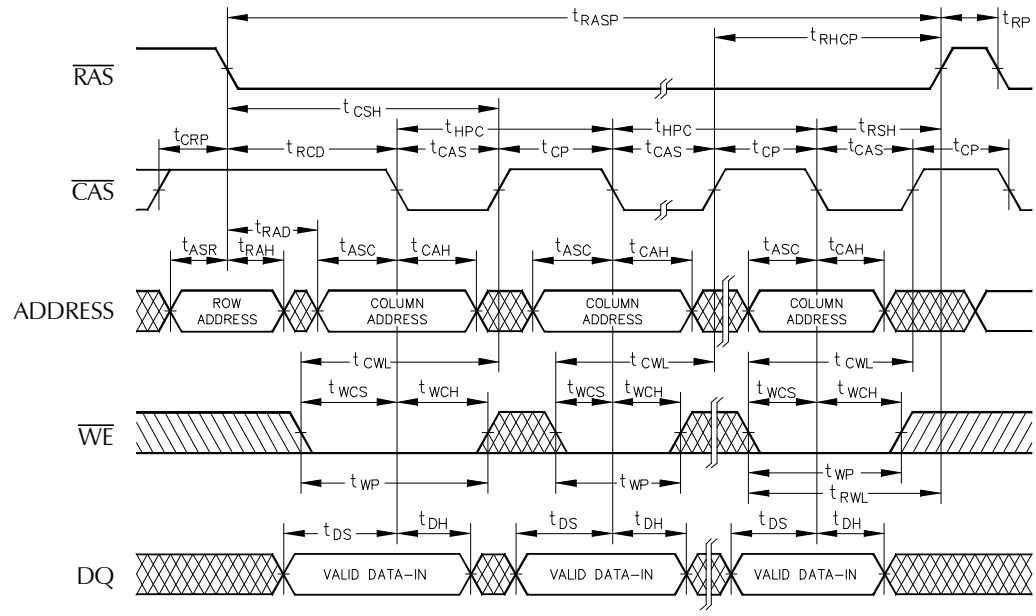

WRITE CYCLE (EARLY WRITE): $D_{OUT}$ = OPEN



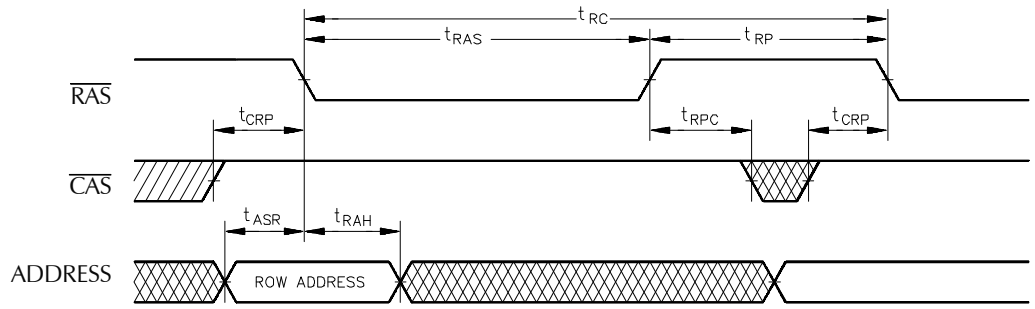
## HYPER PAGE READ CYCLE



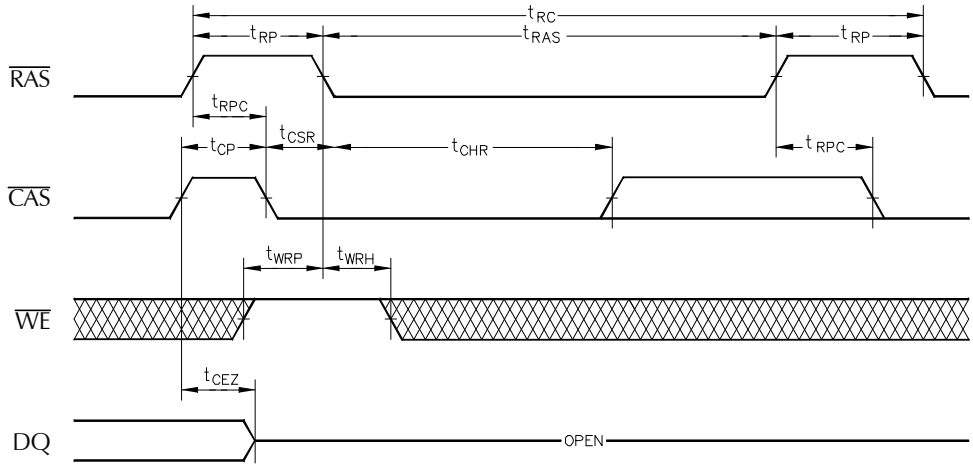

## HYPER PAGE WRITE CYCLE (EARLY WRITE): $D_{OUT}$ = OPEN



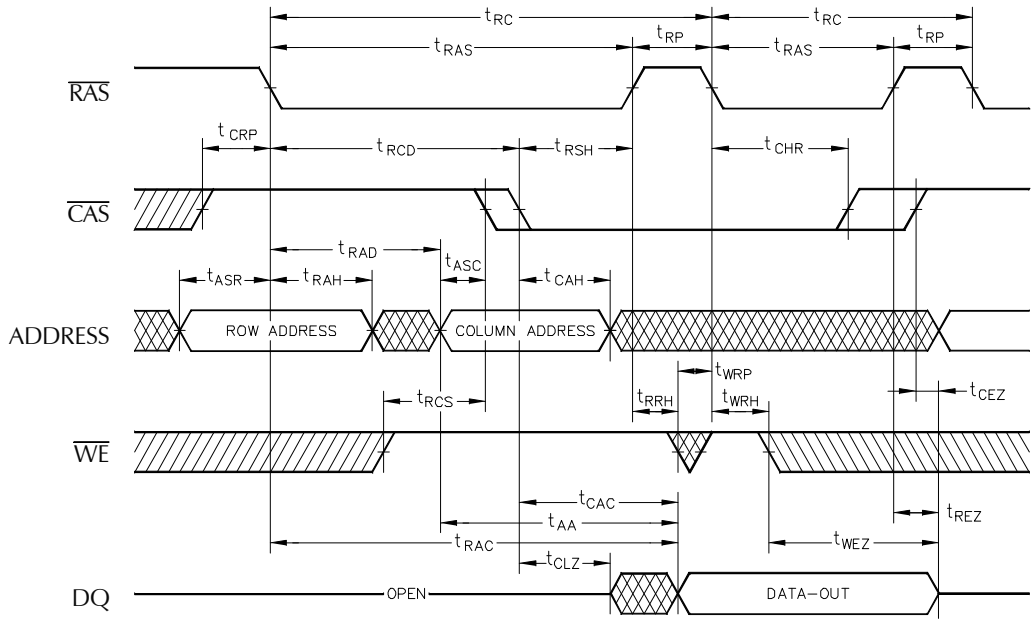
**$\overline{RAS}$ - ONLY REFRESH CYCLE:** $\overline{WE}$, $D_{IN}$ = Don't Care: $D_{OUT}$ = Open



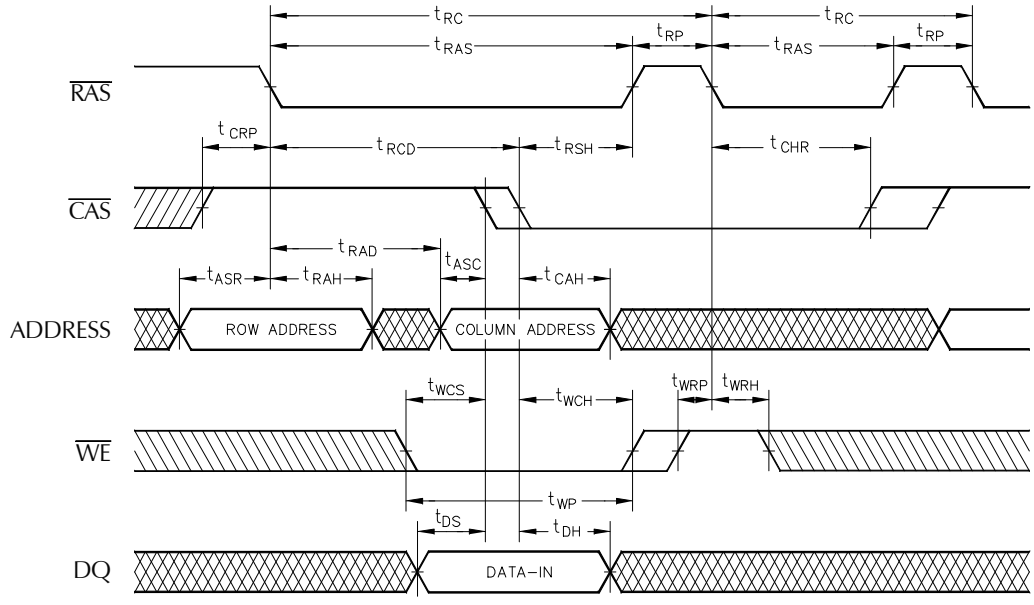

**$\overline{CAS}$ - BEFORE- $\overline{RAS}$ REFRESH CYCLE:** Address = Don't Care



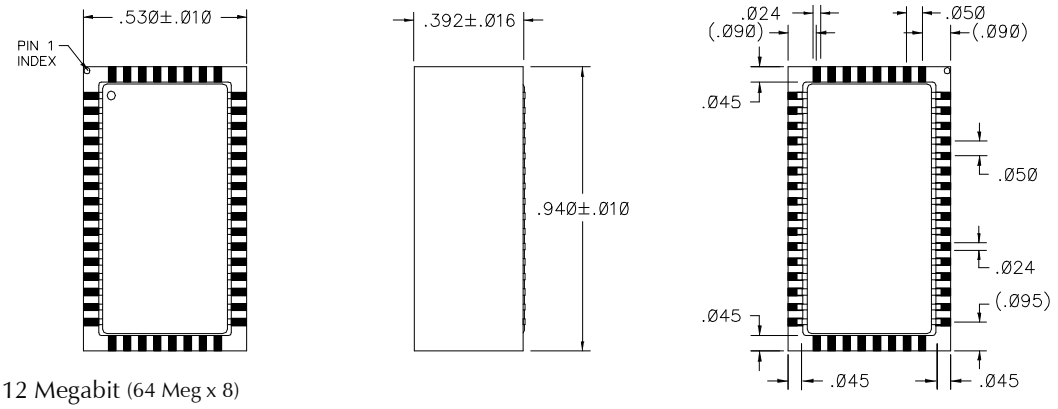
**HIDDEN REFRESH CYCLE (READ)**



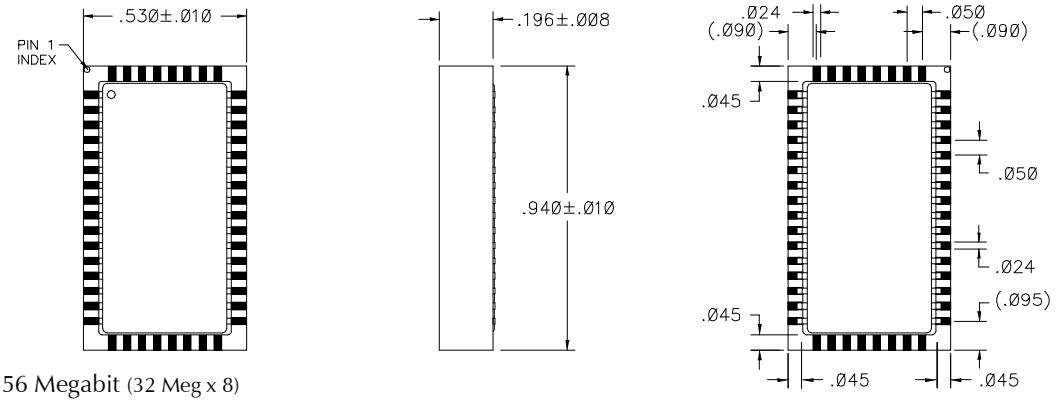

HIDDEN REFRESH CYCLE (WRITE): $D_{OUT}$ = Open



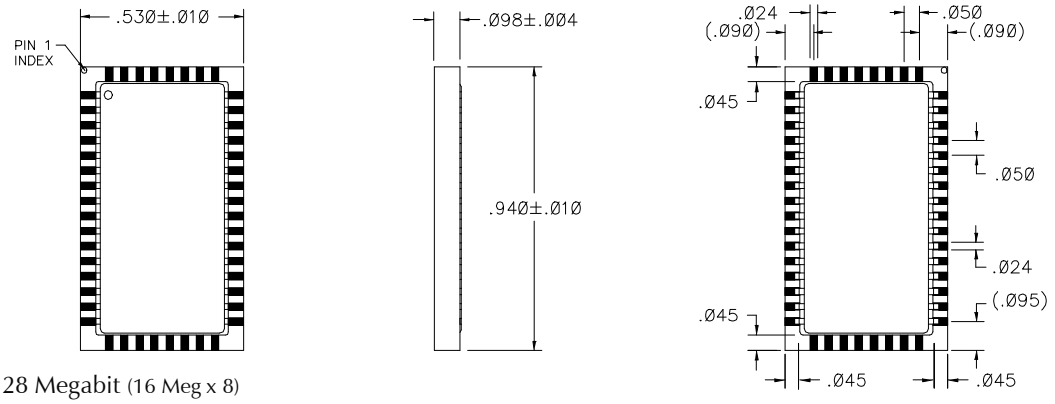
## MECHANICAL DRAWING




512 Megabit (64 Meg x 8)

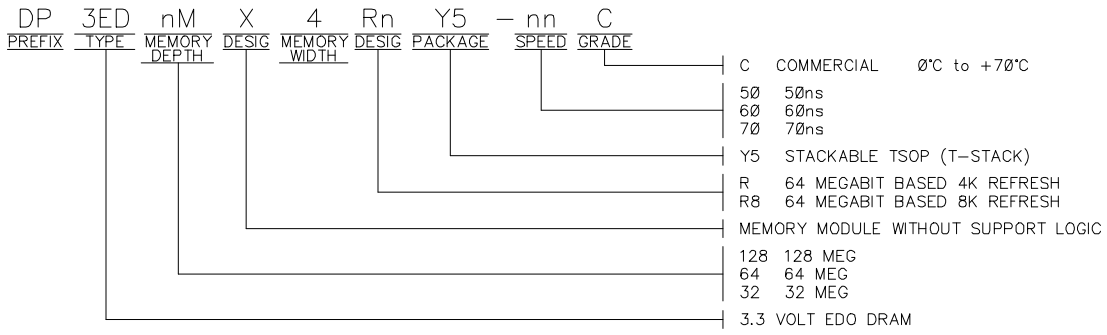



256 Megabit (32 Meg x 8)




128 Megabit (16 Meg x 8)

**ORDERING INFORMATION**

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