DENSE-PAC
MICROSYSTEMS

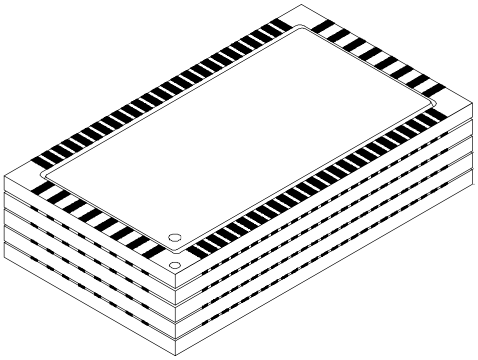
256 Megabit CMOS DRAM
DPnnD8MX32RY5

PRELIMINARY

DESCRIPTION:

The DPnnD8MX32RY5 is the 8 Meg x 32 Dynamic RAM module that utilize the new and innovative space saving TSOP stacking technology. The module is constructed of four 4 Meg x 16 Dynamic RAM's that are configured as 2 banks of 4 Meg x 32.

The DPnnD8MX32RY5 provides for a compatible upgrade path to lower density compatible modules. The module features high speed access times, common data inputs and outputs, and three standard refresh modes.

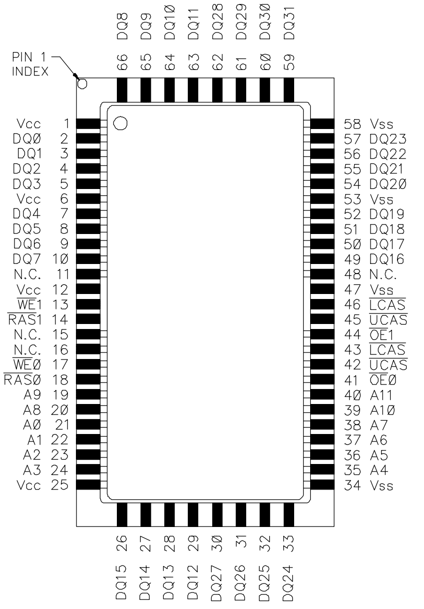


FEATURES:

- Access Times: 60, 70, 80ns (max.)
- 5.0V or 3.3V Supply
- Common Data Inputs and Outputs
- EDO or Fast Page Mode Capability
- 4096 Cycles / 64 ms
- 3 Variations of Refresh:
  - $\overline{\text{RAS}}$ only Refresh
  - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh
  - Hidden Refresh
- Package: TSOP Leadless Stack

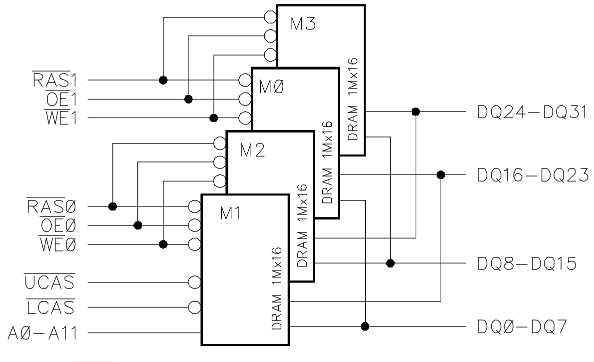
PIN NAMES	
A0 - A11	Row Address: A0 - A11 Column Address: A0 - A9 Refresh Address: A0 - A11
DQ0 - DQ31	Data In / Data Out
$\overline{\text{UCAS}}$	Upper Column Addres Strobe
$\overline{\text{LCAS}}$	Lower Column Addres Stobe
$\overline{\text{RAS}}$0 - $\overline{\text{RAS}}$1	Row Address Enables
$\overline{\text{WE}}$0 - $\overline{\text{WE}}$1	Data Write Enables
$\overline{\text{OE}}$0 - $\overline{\text{OE}}$1	Data Output Enables
V_{DD}	Power Supply (+5V)
V_{SS}	Ground
N.C.	No Connect

PIN-OUT DIAGRAM



NOTE: Pin 43 and Pin 46 are connected together,
Pin 42 and Pin 45 are connected together.

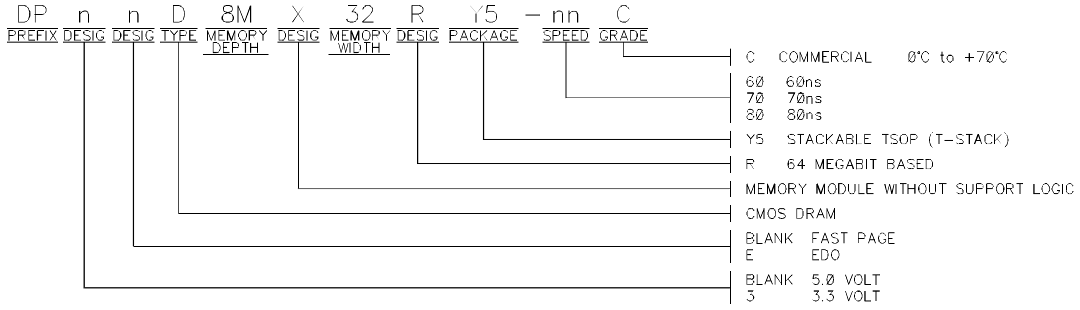
FUNCTIONAL BLOCK DIAGRAM



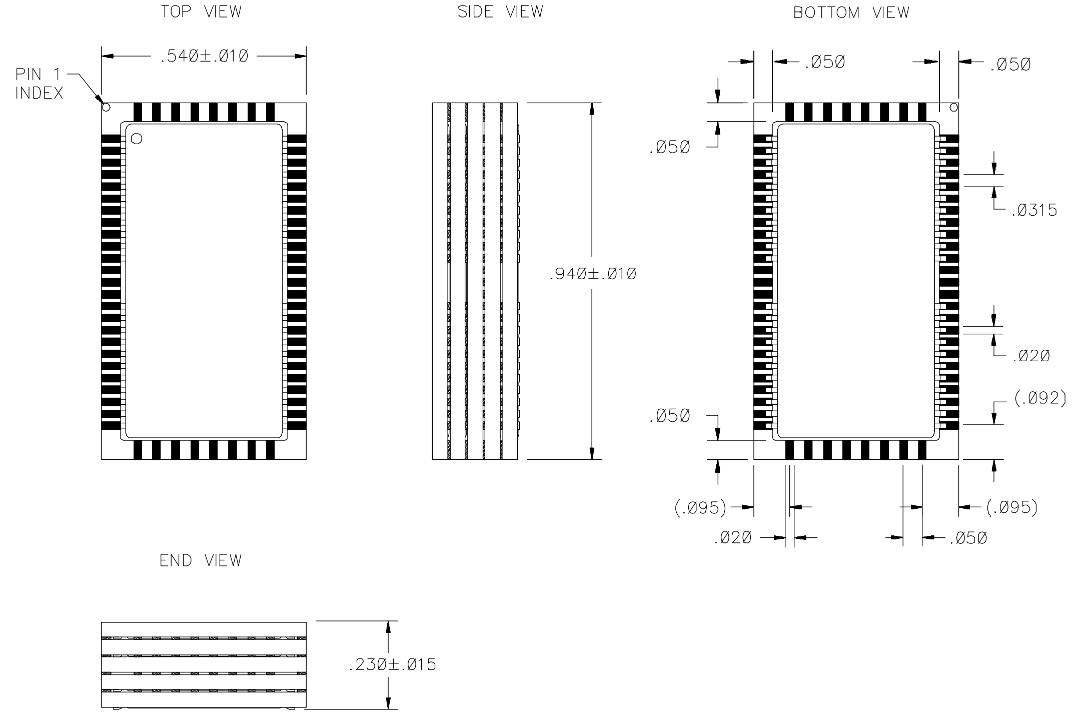
NOTE: $\overline{\text{LCAS}}$ controls DQ0-DQ15, UCAS controlls DQ16-DQ31.

PRELIMINARY

ORDERING INFORMATION



MECHANICAL DRAWING



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