

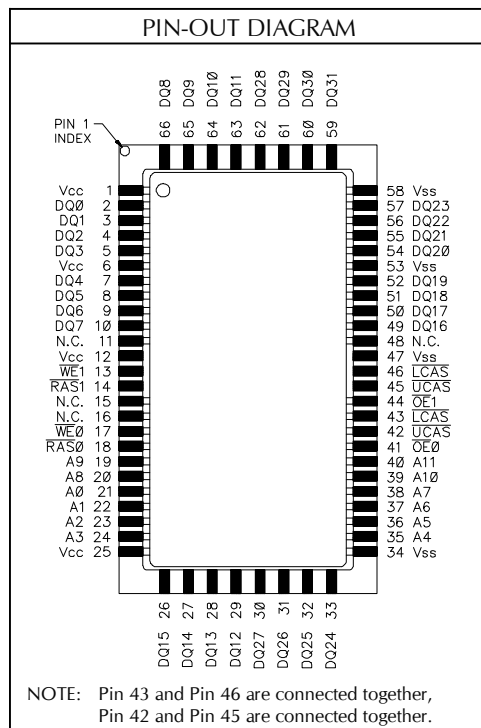
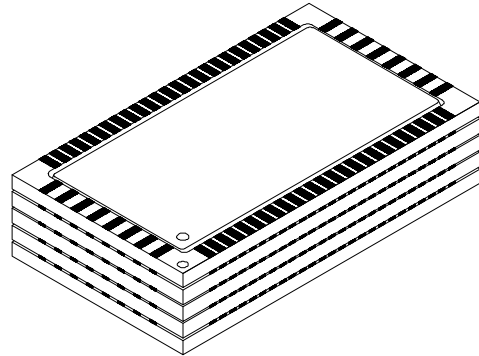
DESCRIPTION:

The DPnnD2MX32PY5 is the 2 Meg x 32 Dynamic RAM module that utilize the new and innovative space saving TSOP stacking technology. The module is constructed of four 1 Meg x 16 Dynamic RAM's that are configured as 2 banks of 1 Meg x 32.

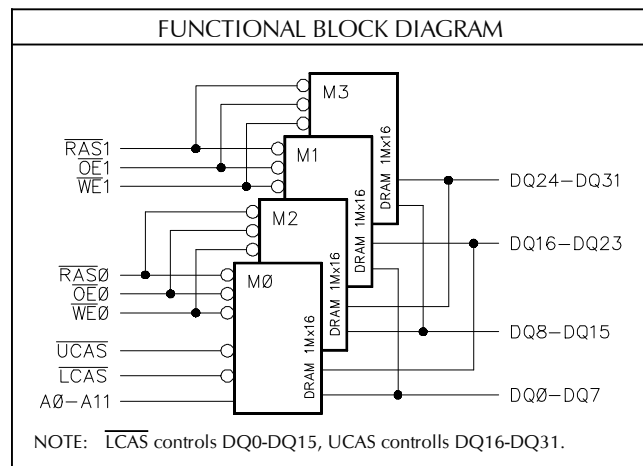
The DPnnD2MX32PY5 provides for a compatible upgrade path to higher density compatible modules. The module features high speed access times, common data inputs and outputs, and three standard refresh modes.

FEATURES:

- Access Times: 60, 70, 80ns (max.)
- 5.0V or 3.3V Supply
- Common Data Inputs and Outputs
- EDO or Fast Page Mode Capability
- 4096 Cycles / 64 ms
- 3 Variations of Refresh:
 - $\overline{RAS}$ only Refresh
 - $\overline{CAS}$ before $\overline{RAS}$ Refresh
 - Hidden Refresh
- Package: TSOP Leadless Stack



PIN NAMES	
A0 - A11	Row Address: A0 - A11 Column Address: A0 - A7 Refresh Address: A0 - A11
DQ0 - DQ31	Data In / Data Out
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{RAS0}$ - $\overline{RAS1}$	Row Address Enables
$\overline{WE0}$ - $\overline{WE1}$	Data Write Enables
$\overline{OE0}$ - $\overline{OE1}$	Data Output Enables
VDD	Power Supply (+5V)
Vss	Ground
N.C.	No Connect



DPnnD2MX32PY5

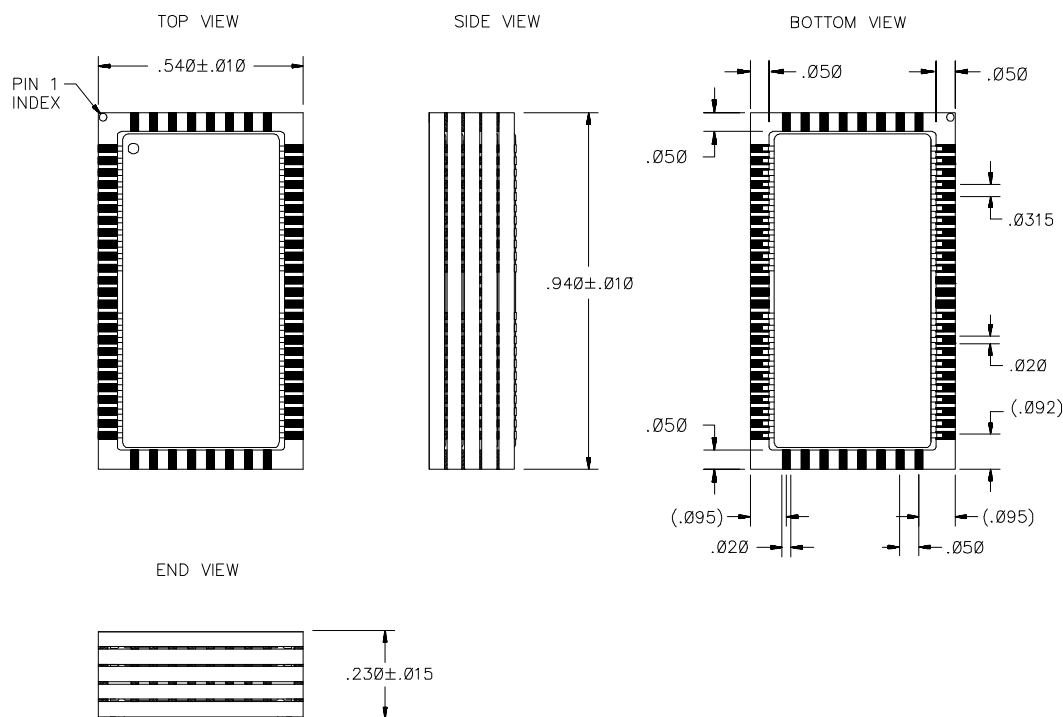
Dense-Pac Microsystems, Inc.

PRELIMINARY

ORDERING INFORMATION

PREFIX	DESIG	DESIG	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	DESIG	PACKAGE	SPEED	GRADE	
DP	n	n	D	2M	X	32	P	Y5	-nn	C	
											C COMMERCIAL 0°C to +70°C
											60 60ns
											70 70ns
											80 80ns
											Y5 STACKABLE TSOP (T-STAKE)
											P 16 MEGABIT BASED
											MEMORY MODULE WITHOUT SUPPORT LOGIC
											CMOS DRAM
											BLANK FAST PAGE
											E EDO
											BLANK 5.0 VOLT
											3 3.3 VOLT

MECHANICAL DRAWING



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