

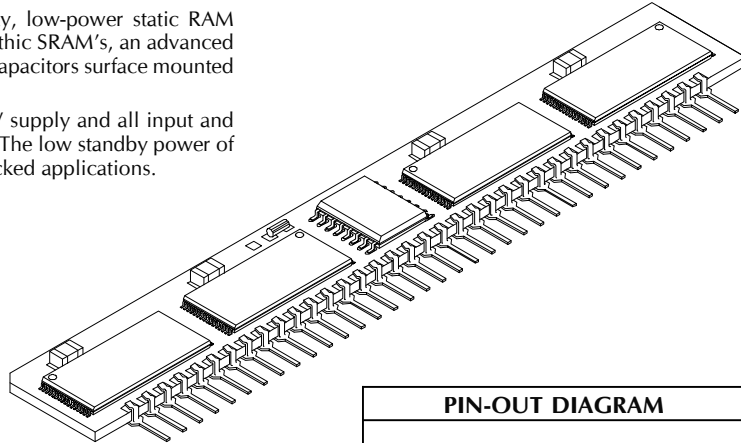
DESCRIPTION:

The DPS1MS8U is a 1Meg X 8 high-density, low-power static RAM module comprised of eight 128K X 8 monolithic SRAM's, an advanced high-speed CMOS decoder and decoupling capacitors surface mounted on an epoxy laminate substrate.

The DPS1MS8U operates from a single +5V supply and all input and output pins are completely TTL-compatible. The low standby power of the DPS1MS8U makes it ideal for battery-backed applications.

FEATURES:

- 1024K by 8 Bit Configuration
- Access Times: 70, 85, 100, 120, 150ns
- Low Power Dissipation:
 - 80 μ W (typ.) Standby
 - 400 mW (typ.) Operating
- 2-Volt Data Retention
- Fully Static Operation
 - No Clock or Refresh Required
- All inputs and Outputs are TTL-Compatible
- 36-PIN Plastic SIP Package

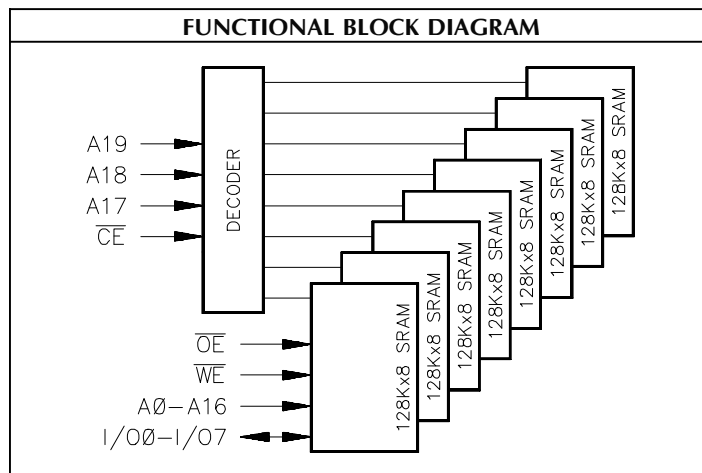


PIN NAMES	
A0 - A19	Address Inputs
I/O0 - I/O7	Data In/Out
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VDD	Power (+ 5V)
VSS	Ground
N.C.	No Connect

PIN-OUT DIAGRAM

N.C.	1
VDD	2
$\overline{WE}$	3
I/O2	4
I/O3	5
I/O0	6
A1	7
A2	8
A3	9
A4	10
VSS	11
I/O5	12
A10	13
A11	14
A5	15
A13	16
A14	17
A19	18
$\overline{CE}$	19
A15	20
A16	21
A12	22
A6	23
I/O1	24
VSS	25
A0	26
A7	27
A8	28
A9	29
I/O7	30
I/O4	31
I/O6	32
A17	33
VDD	34
$\overline{OE}$	35
	36

FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING RANGE ¹					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input HIGH Voltage	2.2		V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage	-0.5 ²		0.8	V
T _A	Operating Temperature	0	+25	+70	°C

TRUTH TABLE					
Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	H	X	X	HIGH-Z	Standby
DOUT Disable	L	H	H	HIGH-Z	Active
Read	L	H	L	D _{OUT}	Active
Write	L	L	X	D _{IN}	Active

H = HIGH

L = LOW

X = Don't Care

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{OH}	HIGH Voltage	I _{OH} = -1.0mA	2.4	-	V
V _{OL}	LOW Voltage	I _{OL} = 2.1mA		0.4	V

ABSOLUTE MAXIMUM RATINGS ³			
Symbol	Parameter	Max.	Unit
T _{STC}	Storage Temperature	-40 to +125	°C
T _{BIAS}	Temperature Under Bias	-10 to +85	°C
V _{DD}	Supply Voltage ¹	-0.5 to +7.0	V
V _{I/O}	Input/Output Voltage ¹	-0.5 to V _{DD} + 0.5	V

CAPACITANCE ⁴ : T _A = 25°C, F = 1.0MHz					
Symbol	Parameter	Max.	Unit	Condition	
C _{ADR}	Address Input	50	pF	V _{IN} = 0V	
C _{CE}	Chip Enable	20			
C _{WE}	Write Enable	45			
C _{OE}	Output Enable	45			
C _{I/O}	Data Input/Output	50			

DC OPERATING CHARACTERISTICS: Over operating ranges						
Symbol	Characteristics	Test Conditions	COMMERCIAL			Unit
			Min.	TYP.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = 0V to V _{DD}	-10		+10	μA
I _{OUT}	Output Leakage Current	V _{I/O} = 0V to V _{DD} , $\overline{CE}$ or $\overline{OE}$ = V _{IH} , or $\overline{WE}$ = V _{IL}	-10		+10	μA
I _{CC1}	Active Supply Current	$\overline{CE}$ = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA		35	60	mA
I _{CC2}	Operating Supply Current	Cycle = min., Duty = 100%, I _{OUT} = 0mA		80	120	mA
I _{SB1}	Full Standby Supply Current (CMOS)	V _{IN} ≥ V _{DD} - 0.2V or V _{IN} ≤ V _{SS} + 0.2V, $\overline{CE}$ ≥ V _{DD} - 0.2V		16	600	μA
I _{SB2}	Standby Current (TTL)	$\overline{CE}$ = V _{IH} , V _{IN} = V _{IH} or V _{IN}		6	24	mA
V _{OL}	Output Low Voltage	I _{OUT} = 2.1mA			0.4	V
V _{OH}	Output High Voltage	I _{OUT} = -1.0mA	2.4			V

DATA RETENTION CHARACTERISTICS						
Symbol	Parameter	Test Conditions	Min.	TYP.	Max.	Unit
V _{DR}	Data Retention Voltage	$\overline{CE}$ ≥ V _{DR} - 0.2V	2.0		5.5	V
I _{CCDR2}	Data Retention Supply Current	V _{DR} = 2.0V		8	360	μA
I _{CCDR3}	Data Retention Supply Current	V _{DR} = 3.0V		8	400	μA
t _{CDR}	Chip Disable to Data Retention Time		0			ns
t _R	Recovery Time	t _{RC} = Read Cycle Timing	5			ms

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns *
Input and Output Timing Reference Levels	1.5V

* Transition measured between 0.8V and 2.2V.

Output Load		
Load	C _L	Parameters Measured
1	100pF	except tCLZ, tOLZ, tCHZ, tOHZ, tWHZ, and tWLZ
2	5pF	tCLZ, tOLZ, tCHZ, tOHZ, tWHZ, and tWLZ

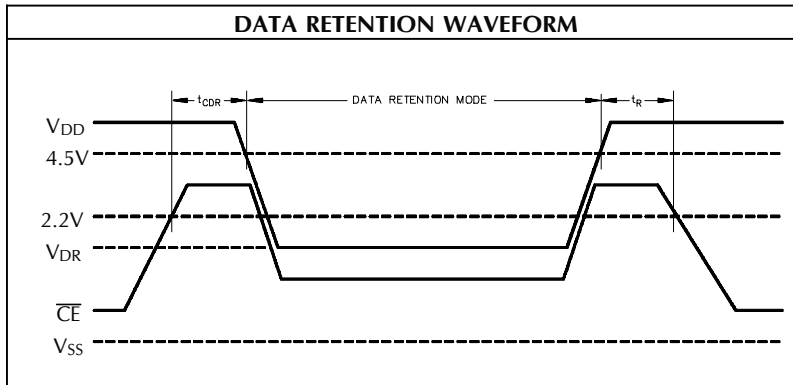
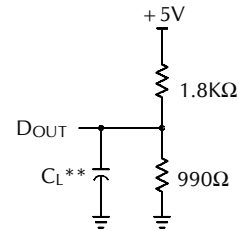


Figure 1. Output Load

** Including Probe and Jig Capacitance.

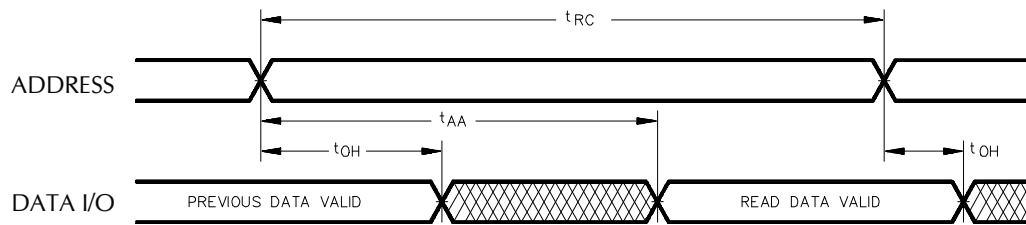
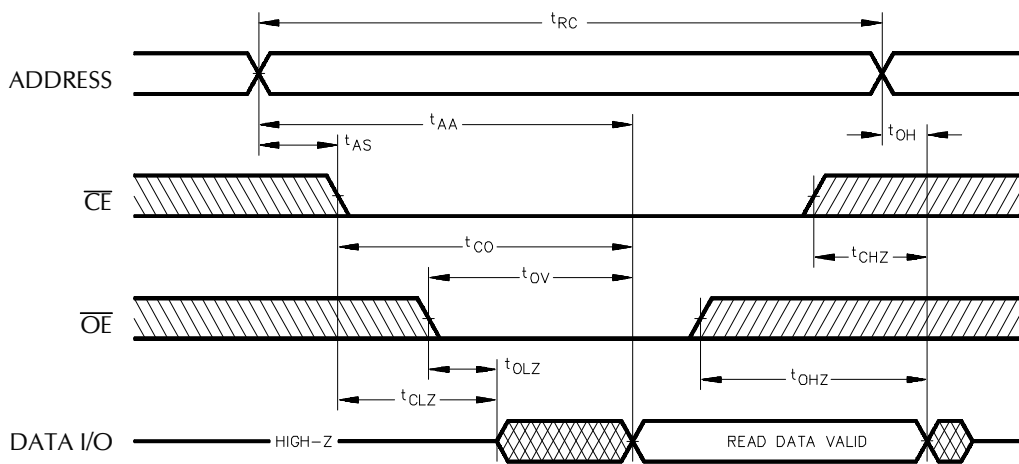
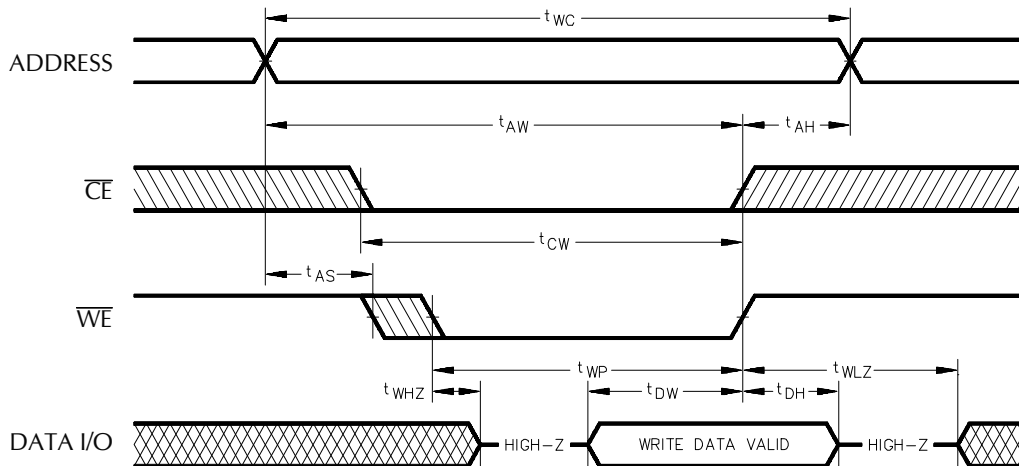


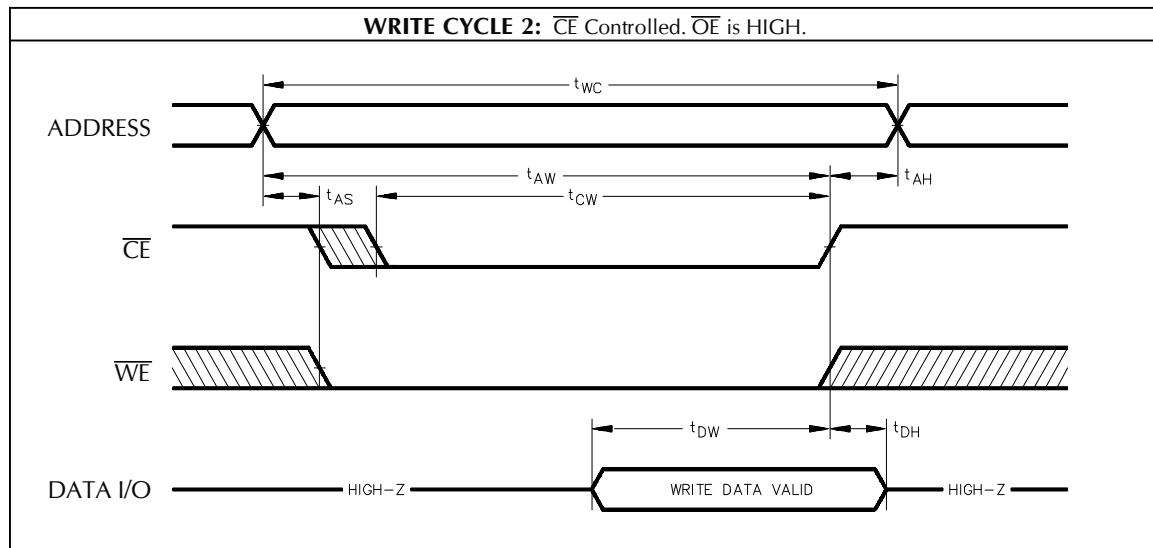
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	70ns		85ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{RC}	Read Cycle Time	70		85		100		120		150		ns
2	t _{AA}	Address Access Time		70		85		100		120		150	ns
3	t _{CO}	Chip Enable to Output Valid		70		85		100		120		150	ns
4	t _{OV}	Output Enable to Output Valid		40		40		45		50		60	ns
5	t _{OH}	Output Hold from Address Change	10		10		10		10		10		ns
6	t _{CLZ}	Chip Enable to Output in LOW-Z ^{4, 6}	5		5		5		10		10		ns
7	t _{OLZ}	Output Enable to Output in LOW-Z ^{4, 6}	0		0		0		0		0		ns
8	t _{CHZ}	Chip Enable to Output in HIGH-Z ^{4, 6}		40		45		45		50		60	ns
9	t _{OHZ}	Output Enable to Output in HIGH-Z ^{4, 6}		25		30		30		35		45	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges ⁷													
No.	Symbol	Parameter	70ns		85ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t _{WC}	Write Cycle Time	70		85		100		120		150		ns
11	t _{AW}	Address Valid to End of Write	65		80		90		105		115		ns
12	t _{CW}	Chip Enable to End of Write	65		80		90		105		115		ns
13	t _{DW}	Data to Write Time Overlap	30		35		35		40		50		ns
14	t _{DH}	Data Hold Time from Write Time	0		0		0		0		0		ns
15	t _{WP}	Write Pulse Width	50		55		65		75		85		ns
16	t _{AS}	Address Set-up Time ***	0		0		0		0		0		ns
17	t _{AH}	Address Hold Time	5		5		5		5		5		ns
18	t _{WHZ}	Write Enable to Output in HIGH-Z ^{4, 6}		25		30		30		35		40	ns
19	t _{WLZ}	Write Enable to Output in LOW-Z ^{4, 6}	5		5		5		5		5		ns

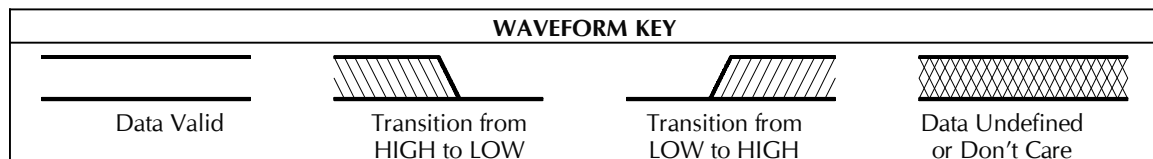
*** Valid for both Read and Write Cycles.

† Available in commercial only.

READ CYCLE 1: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ and $\overline{OE}$ are LOW.**READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.****WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW.**

**NOTES:**

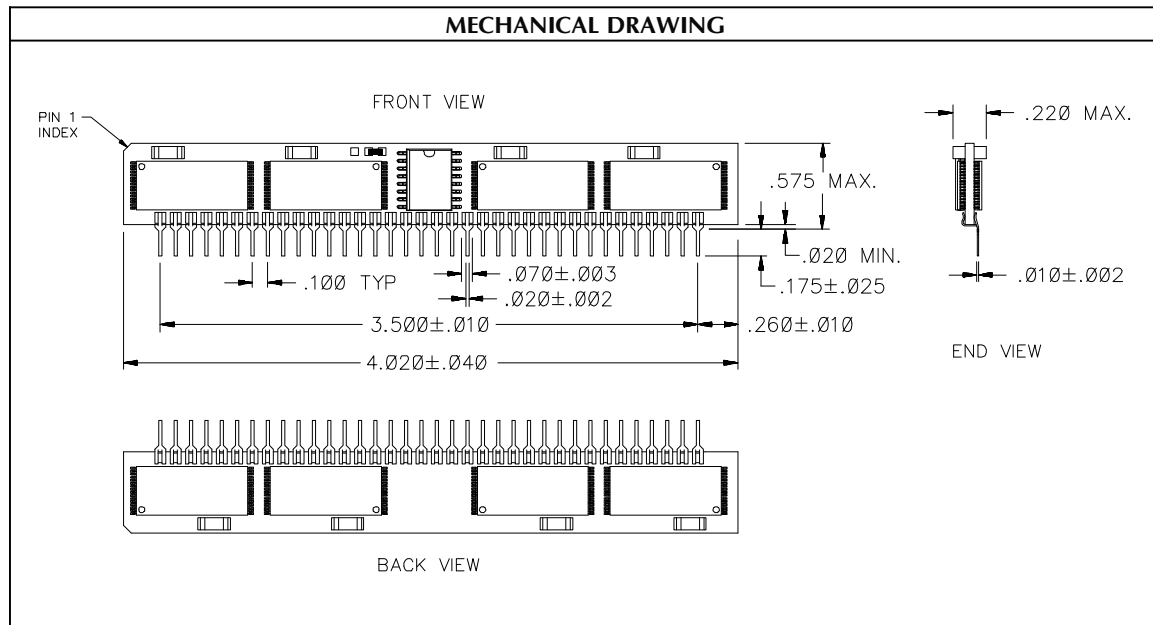
1. All voltages are with respect to V_{SS} .
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of $\pm 500\text{mV}$ from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.



ORDERING INFORMATION

DP	S	1M	S	8	U	-XX	C	
PREFIX	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	PACKAGE	SPEED	GRADE	
							C	COMMERCIAL 0°C to +70°C
						70		70ns
						85		85ns
						10		100ns
						12		120ns
						15		150ns
								36-PIN PLASTIC SINGLE INLINE PACKAGE (SIP)
								MEMORY MODULE WITH SUPPORT LOGIC
								CMOS SRAM

MECHANICAL DRAWING



Dense-Pac Microsystems, Inc.

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