DENSE-PAC
MICROSYSTEMS

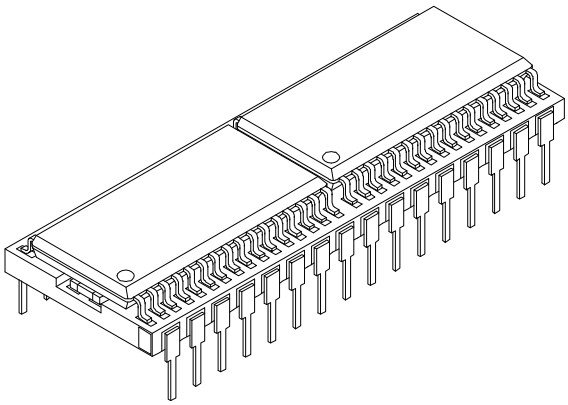
8 Megabit CMOS SRAM
DPS1MS8MP

DESCRIPTION:

The DPS1MS8MP is a 1Meg x 8 high-density, low-power static RAM module comprised of two 512K x 8 monolithic SRAM's, an advanced high-speed CMOS decoder and decoupling capacitors surface mounted on a co-fired ceramic substrate having side-brazed leads.

The DPS1MS8MP is available in a 600-mil-wide, 32-pin dual-in-line package that is upward compatible to the JEDEC standard pin configuration for 4 megabit monolithics.

The DPS1MS8MP operates from a single +5V supply and all input and output pins are completely TTL-compatible. The low standby power of the DPS1MS8MP makes it ideal for battery-backed applications.



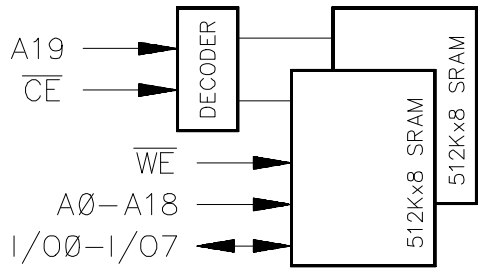
FEATURES:

- 1 Megabit x 8 Configuration
- Access Times: 55*, 70, 85, 100, 120, 150ns
- Low Power Dissipation:
  300 µA (max.) Standby (CMOS)
  100 mA (max.) Operating
- 2-Volt Data Retention
- Fully Static Operation
  - No Clock or Refresh Required
- All inputs and Outputs are TTL-Compatible
- 600 mil, 32-pin JEDEC Standard DIP Pinout

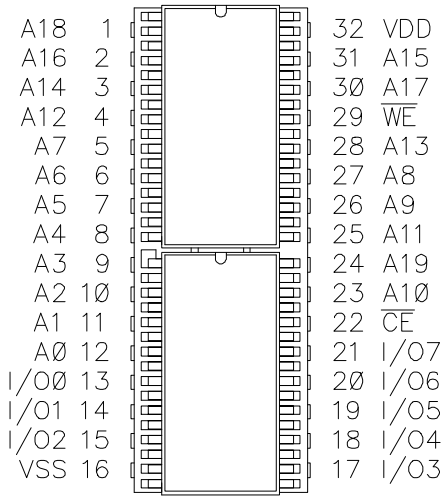
* Available in Commercial only.

PIN NAMES	
A0 - A17	Address Inputs
I/O0 - I/O7	Data In/Out
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{DD}	Power (+5V)
V_{SS}	Ground

FUNCTIONAL BLOCK DIAGRAM



PIN-OUT DIAGRAM



RECOMMENDED OPERATING RANGE [1]						
Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage		2.2		$V_{DD}+0.3$	V
V_{IL}	Input LOW Voltage		-0.5[2]		0.8	V
T_A	Operating Temperature	C	0	+25	+70	°C
		I	-40	+25	+85	

TRUTH TABLE				
Mode	$\overline{CE}$	$\overline{WE}$	I/O Pin	Supply Current
Not Selected	H	X	HIGH-Z	Standby
D_{OUT} Disable	L	H	HIGH-Z	Active
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

H = HIGH L = LOW X = Don't Care

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH} = -1.0mA	2.4	-	V
V_{OL}	LOW Voltage	I_{OL} = 2.1mA		0.4	V

ABSOLUTE MAXIMUM RATINGS [3]			
Symbol	Parameter	Max.	Unit
T_{STC}	Storage Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to + 85	°C
V_{DD}	Supply Voltage [1]	-0.5 to + 7.0	V
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD} +0.5	V

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	25	pF	V_{IN} = 0V
C_{CE}	Chip Enable	20		
C_{WE}	Write Enable	25		
$C_{I/O}$	Data Input/Output	35		

DC OPERATING CHARACTERISTICS: Over operating ranges							
Symbol	Characteristics	Test Conditions	COMMERCIAL		INDUSTRIAL †		Unit
			Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-5	+5	-5	+5	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-5	+5	-5	+5	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		45		50	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100%, I_{OUT} = 0mA		100		100	mA
I_{SB1}	Full Standby Supply Current	$V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ +0.2V, $\overline{CE} \geq V_{DD}$ -0.2V		250		300	µA
I_{SB2}	Standby Current	$\overline{CE}$ = V_{IH}, V_{IN} = V_{IH} or V_{IN}		6		6	mA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA	2.4		2.4		V

DATA RETENTION CHARACTERISTICS								
Symbol	Parameter	Test Conditions	Typ.	COMMERCIAL		INDUSTRIAL †		Unit
				Min.	Max.	Min.	Max.	
V_{DR}	Data Retention Voltage	$\overline{CE} \geq V_{DR}$ -0.2V	-	2.0	5.5	2.0	5.5	V
I_{CCDR2}	Data Retention Supply Current	V_{DR} = 2.0V	2		100		135	µA
I_{CCDR3}	Data Retention Supply Current	V_{DR} = 3.0V	2		120		150	µA
t_{CDR}	Chip Disable to Data Retention Time		-	0		0		ns
t_R	Recovery Time	t_{RC} = Read Cycle Timing		5		5		ms

† Not Available in 55ns.

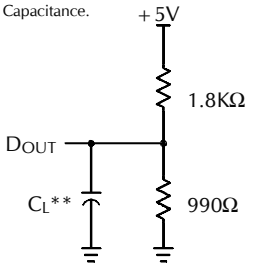
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns *
Input and Output Timing Reference Levels	1.5V

* Transition measured between 0.8V and 2.2V.

Output Load		
Load	C_L	Parameters Measured
1	100pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{WLZ}
2	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{WLZ}

Figure 1. Output Load

** Including Probe and Jig Capacitance.

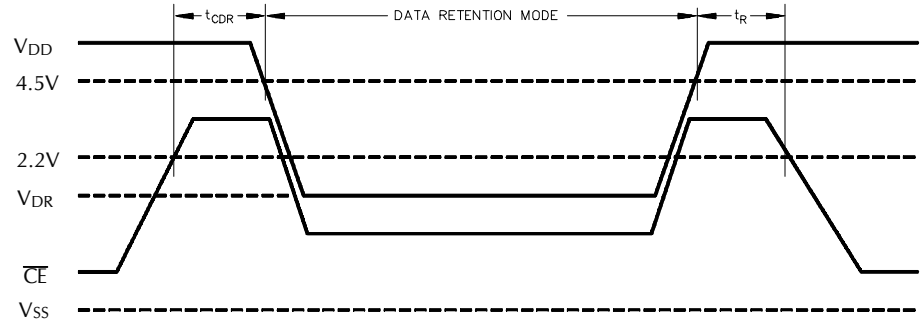


AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges														
No.	Symbol	Parameter	55ns††		70ns		85ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	55		70		85		100		120		150		ns
2	t_{AA}	Address Access Time		55		70		85		100		120		150	ns
3	t_{CO}	Chip Enable to Output Valid		55		70		85		100		120		150	ns
4	t_{OH}	Output Hold from Address Change	10		10		10		10		10		10		ns
5	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 6]	10		10		10		10		10		10		ns
6	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 6]		35		35		45		45		50		60	ns

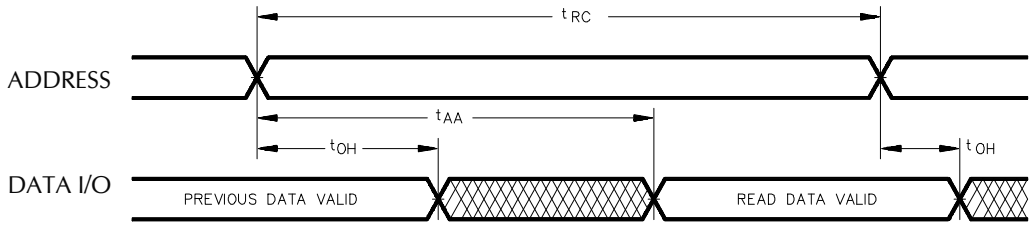
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [7]														
No.	Symbol	Parameter	55ns††		70ns		85ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
7	t_{WC}	Write Cycle Time	55		70		85		100		120		150		ns
8	t_{AW}	Address Valid to End of Write	50		65		80		90		105		115		ns
9	t_{CW}	Chip Enable to End of Write	50		65		80		90		105		115		ns
10	t_{DW}	Data to Write Time Overlap	30		35		35		35		40		50		ns
11	t_{DH}	Data Hold Time from Write Time	0		0		0		0		0		0		ns
12	t_{WP}	Write Pulse Width	45		55		55		65		75		85		ns
13	t_{AS}	Address Set-up Time ***	0		0		0		0		0		0		ns
14	t_{AH}	Address Hold Time	5		5		5		5		5		5		ns
15	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 6]		25		30		30		30		35		40	ns
16	t_{WLZ}	Write Enable to Output in LOW-Z [4, 6]	5		5		5		5		5		5		ns

*** Valid for both Read and Write Cycles.

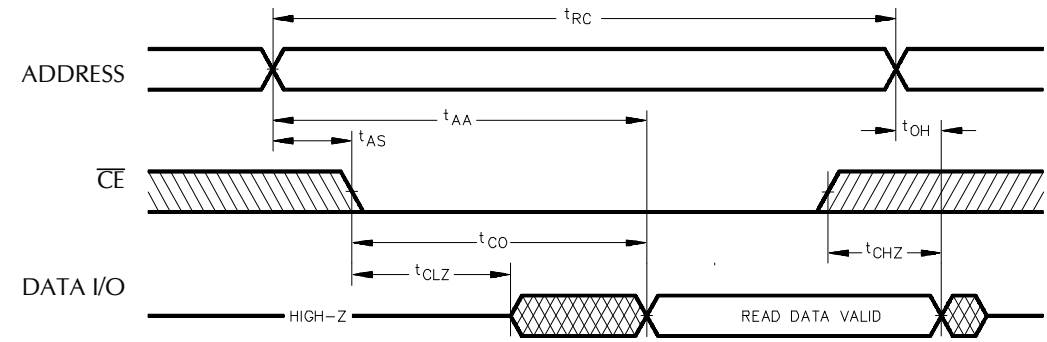
DATA RETENTION WAVEFORM



READ CYCLE 1: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ is LOW.



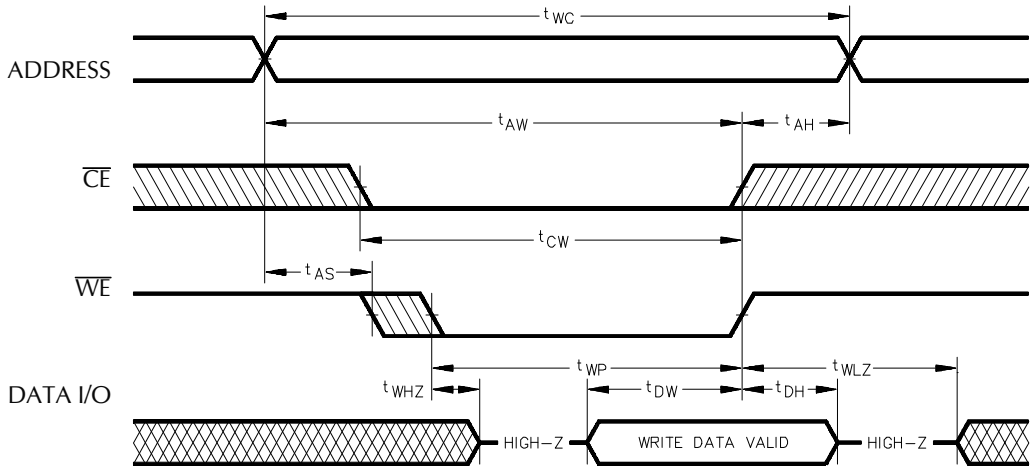
READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.



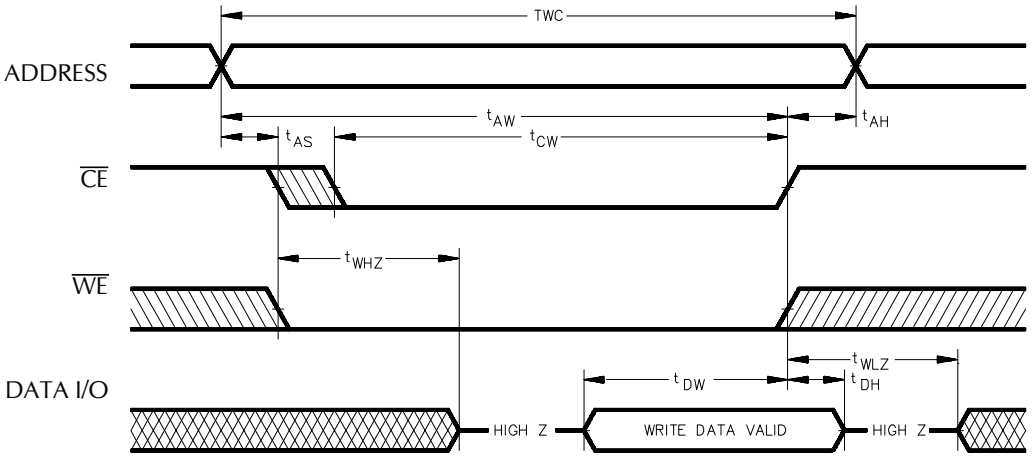
NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

WRITE CYCLE 1: $\overline{WE}$ Controlled

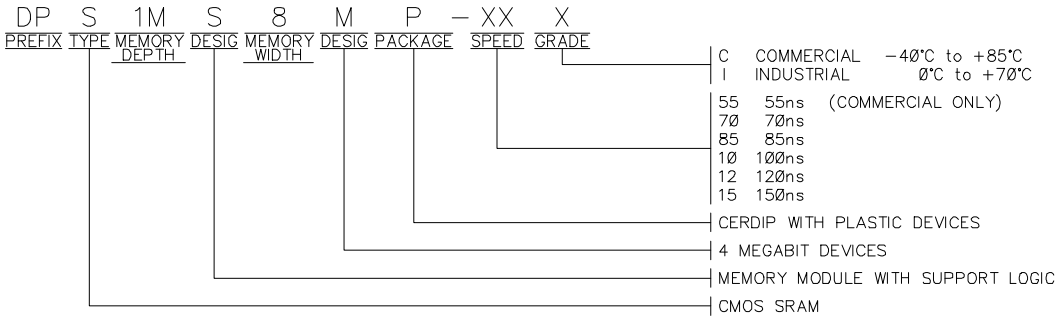


WRITE CYCLE 2: $\overline{CE}$ Controlled.



WAVEFORM KEY

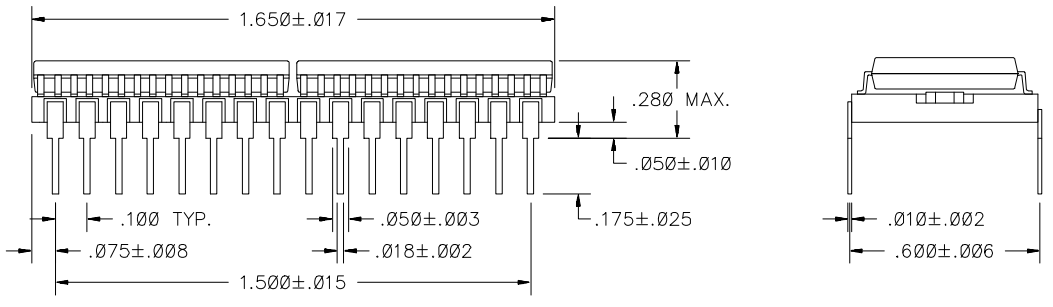
ORDERING INFORMATION



APPLICATION NOTE:

An upgrade to an existing memory design that uses 512Kx8 or lower density SRAM memories in a 32-pin plastic DIP to a design that uses 1Mx8 SRAM memories can be achieved by some slight modifications of the P.C.B. board. It should be noted that the only pin-out difference between the 512Kx8 memory and the 1Mx8 memory is that pin 24 is the ''Output Enable'' ($\overline{OE}$) for the 512Kx8 and it is Address 19 (A19) for the 1Mx8. The 1Mx8 emulation module is made with two 512Kx8 monolithic memories and a decoder. A19 is input to the decoder to select between the two 512Kx8 SRAM memories. The 32-pin module does not have a spare pin to allow the addition of A19, therefore the $\overline{OE}$ to both monolithic 512Kx8's on the module are hard wired to ground and the corresponding module pin is used for A19. This arrangement provides the user a simple hardware modification of one cut and one jumper to achieve the upgrade. Since the $\overline{OE}$ and Address signals are most often common signals to the users SRAM array, the $\overline{OE}$ signal line can be simply cut where it is fed to the SRAM array, thereby not affecting other circuitry that uses this signal. The signal that is provided to drive A19 is then jumpered to what was the $\overline{OE}$ input to the array. This is the basic concept, additional cuts and jumpers may be needed depending on the memory configurations and P.C.B. routing. In addition, the designer will need to analyze the possible effects on system timing that a grounded $\overline{OE}$ pin on the monolithic memories will exhibit. The I/O pins of the memories will now be active within 5ns of when the $\overline{CE}$ pin of the memory goes low and the $\overline{WE}$ pin is high (the $\overline{OE}$ pin is no longer available to control the output state of the I/O's). When the memory is selected by the $\overline{CE}$ going low, the $\overline{WE}$ pin will determine when a read or a write is being performed. To avoid possible bus contention problems, the designer should evaluate the I/O timing changes.

MECHANICAL DRAWING



Dense-Pac Microsystems, Inc.
7321 Lincoln Way ◆ Garden Grove , California 92841-1431
(714) 898-0007 (800) 642-4477 (Outside CA) ◆ FAX: (714) 897-1772 ◆ http://www.dense-pac.com