DENSE-PAC
MICROSYSTEMS

4 Megabit CMOS EEPROM

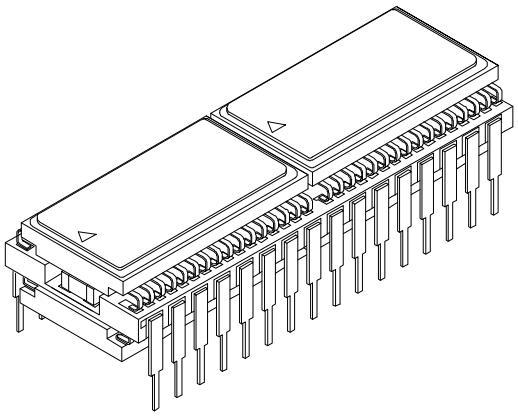
DPE512S8N

DESCRIPTION:

The DPE512S8N is a 512K X 8 high-density, low-power EEPROM module comprised of four ceramic 128K X 8 monolithic EEPROM's, an advanced high-speed CMOS decoder and decoupling capacitors surface mounted on a co-fired ceramic substrate having side-brazed leads.

The DPE512S8N is available in a 600-mil-wide, 32-pin dual-in-line package that conforms to the same JEDEC standard pin configuration as the future four megabit monolithics.

The DPE512S8N operates from a single +5V supply and all input and output pins are completely TTL-compatible.

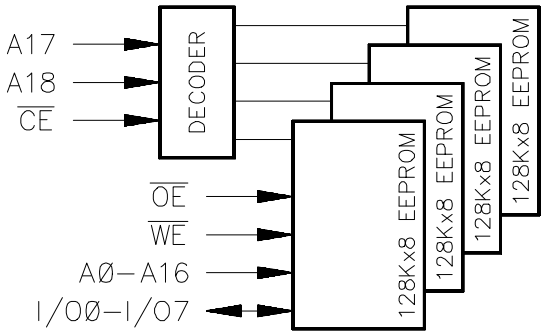


FEATURES:

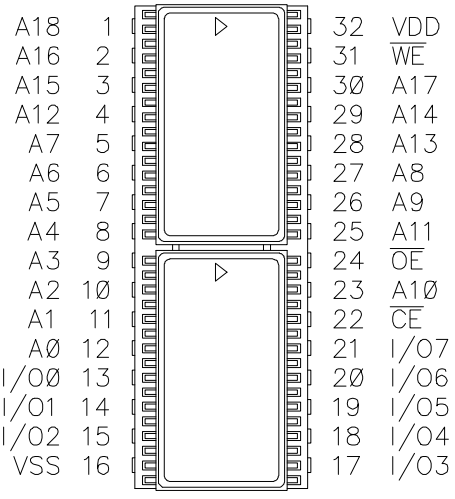
- 524,288 by 8 bit configuration
- Fast Access Times: 135, 170, 250, 300ns (max.)
- Low Power Available in Commercial Only
  Dissipation:
  - 495 mW Operating
  - 6.6 mW (CMOS) Standby
- Fast Write Cycle Times
  - 128 Byte Page Write Operation
  - 10ms Typical Byte Write Operation
- Data Protection
  - Hardware and Software (JEDEC - Approved)
  - Write Protection
- High Endurance
  - 10,000 Program / Erase Cycles
  - 10 Year Data Retention
- JEDEC Approved Byte Wide Pinout
- Only 1.660 x 0.600 x 0.400 inches

PIN NAMES	
A0 - A18	Address Inputs
I/O0 - I/O7	Data In/Out
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground

FUNCTIONAL BLOCK DIAGRAM



PIN-OUT DIAGRAM



RECOMMENDED OPERATING RANGE [1]						
Symbol	**Characteristic**		**Min.**	**Typ.**	**Max.**	**Unit**
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
T_A	Operating Temperature	C	0	+25	+70	°C
		I	-40	+25	+85	
		M/B	-55	+25	+125	

TRUTH TABLE				
Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	**I/I Pin**
Standby	H	X	X	HIGH-Z
Read	L	L	H	D_{OUT}
Write	L	H	L	D_{IN}
Write Inhibit	X	L	X	HIGH-Z
Write Inhibit	X	X	H	HIGH-Z

L = LOW H = HIGH X = Don't Care

ABSOLUTE MAXIMUM RATINGS [1]			
Symbol	**Parameter**	**Value**	**Unit**
T_{STG}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
V_{DD}	Supply Voltage [2]	-0.6 to +6.25	°C
$V_{I/O}$	Input/Output Voltage [2]	-0.6 to +6.25	V

CAPACITANCE [3]: T_A = 25°C, F = 1.0MHz				
Symbol	**Parameter**	**Max.**	**Unit**	**Condition**
C_{CE}	Chip Enable	20	pF	V_{IN} = 0V
C_{ADR}	Address Input	50		
C_{WE}	Write Enable	50		
C_{OE}	Output Enable	50		
$C_{I/O}$	Data Input/Output	60		

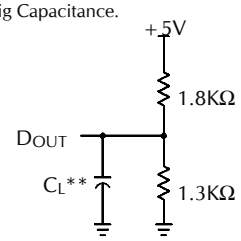
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

* Transition between 0.8V and 2.2V.

OUTPUT LOAD		
Load	**C_L**	**Parameters Measured**
1	100pF	except t_{DF}
2	5pF	t_{DF}

Figure 1. Output Load

** Including Probe and Jig Capacitance.



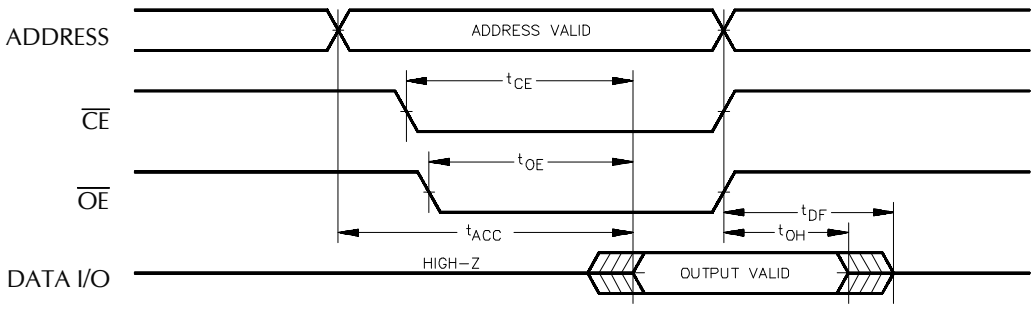
DC OPERATING CHARACTERISTICS: Over operating ranges					
Symbol	**Characteristics**	**Test Conditions**	**X8**		**Unit**
			Min.	**Max.**	
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} Max.	-40	+40	µA
I_{OUT}	Output Leakage Current	V_{OUT} = V_{DD} Max.	-40	+40	µA
I_{CC}	Operating Supply Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, all I/O = 0mA, f = 5MHz		90	mA
I_{SB1}	V_{DD} Standby Current (TTL)	$\overline{CE}$ = V_{IH}		12	mA
I_{SB2}	V_{DD} Standby Current (CMOS)	$\overline{CE}$ = V_{DD} -0.3Vdc		1.2	mA
V_{IL}	Input Voltage Low			0.8	V
V_{IH}	Input Voltage High		2.0		V
V_{OL}	Output Voltage Low	I_{OUT} = 2.1mA		0.45	V
V_{OH}	Output Voltage High	I_{OUT} = -400µA	2.4		V

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges											
No.	Symbol	Parameter	135ns		170ns		250ns		300ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	135		170		250		300		ns
2	t_{CE}	Chip Enable to Output Valid		135		170		250		300	ns
3	t_{ACC}	Address Access Time		135		170		250		300	ns
4	t_{OE}	Output Enable Access Time		50		55		55		55	ns
5	t_{DF}	Chip Enable or Output Enable to Output Float [3]	0	60	0	65	0	65	0	65	ns
6	t_{OH}	Output Hold from Chip Enable, Output Enable, or Address, Whichever Occurs First	0		0		0		0		ns

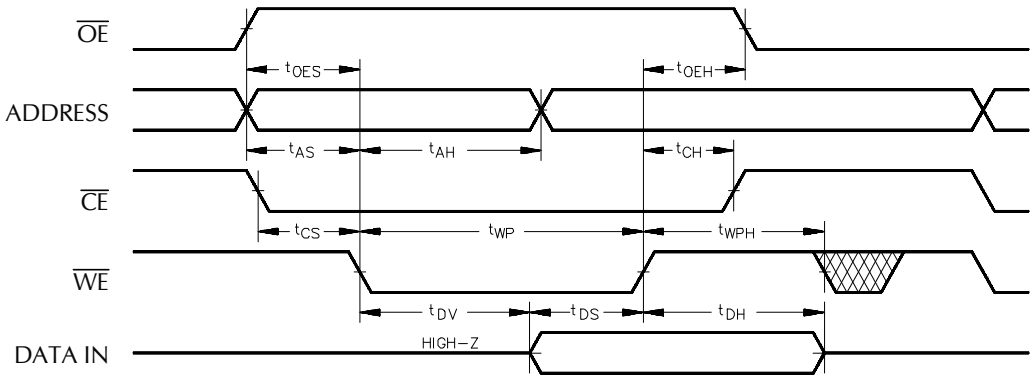
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [5, 6]					
No.	Symbol	Parameter	Min.	Max.	Unit
7	t_{WC}	Write Cycle Time		10	ms
8	t_{AS}	Address Set-up Time *	10		ns
9	t_{AH}	Address Hold Time	100		ns
10	t_{CS}	Chip Select Set-up Time	0		ns
11	t_{CH}	Chip Select Hold Time	0		ns
12	t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150		ns
13	t_{DS}	Data Set-up Time	100		ns
14	t_{DH}	Data Hold Time	10		ns
15	t_{OES}	Output Enable Set-up Time	10		ns
16	t_{OEH}	Output Enable Hold Time	10		ns
17	t_{WPH}	Write Pulse Width High	50		ns
18	t_{BLC}	Byte Load Cycle Time		150	µs
19	t_{WR}	Write Recovery Time	0		ns

* Valid for both Read and Write Cycles.

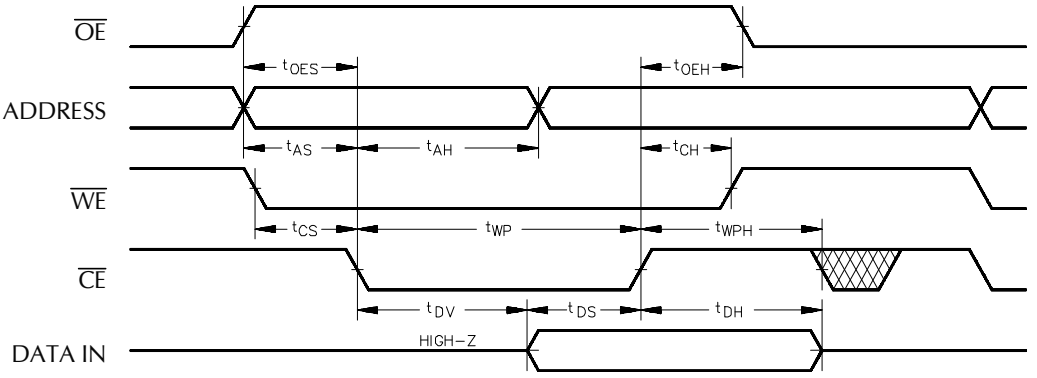
READ CYCLE



WRITE CYCLE 1: $\overline{WE}$ Controlled.



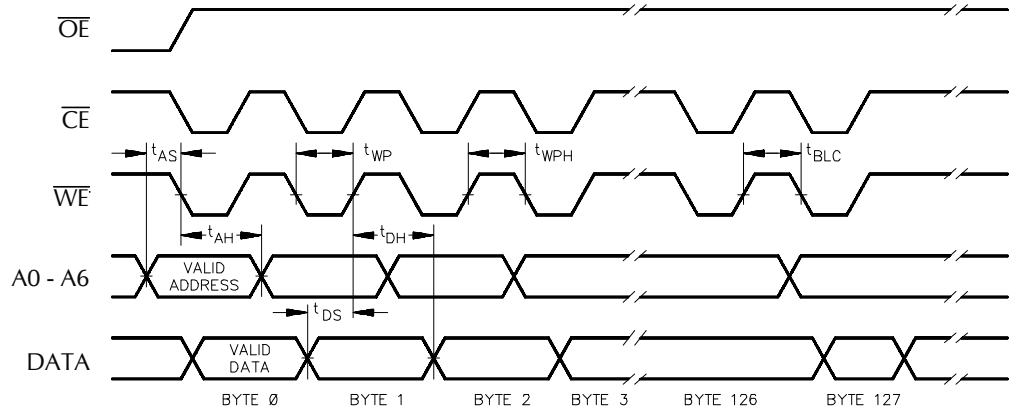
WRITE CYCLE 2: $\overline{CE}$ Controlled.



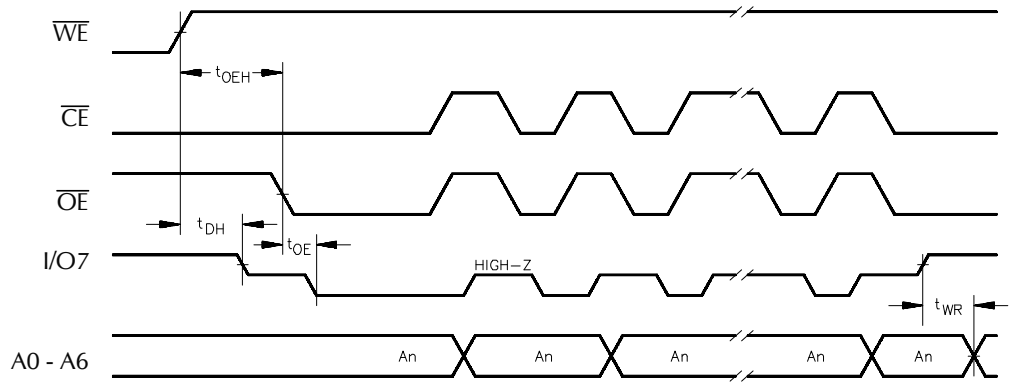
WAVEFORM KEY

Data Valid	Transition from HIGH to LOW	Transition from LOW to HIGH	Data Undefined or Don't Care

PAGE MODE WRITE WAVEFORM



DATA POLLING WAVEFORM



DEVICE OPERATION

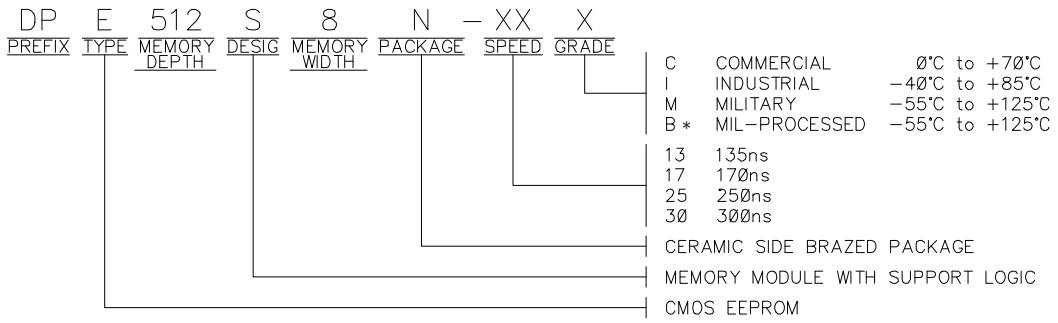
READ: The DPE512S8N is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$. Once a byte Write has been started it will automatically time itself to completion.

PAGE WRITE: The page write operation of the DPE512S8N allows 1 to 128 bytes of data to be loaded into the device and then simultaneously written during the internal programming period. After the first byte of data has been loaded into the device, successive bytes may be loaded in the same manner. Each new byte to be written must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A18 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 are used to specify which byte within the page are to be written. The bytes may loaded in any order and may be changed within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: Write cycles typically are completed in less time than the maximum write cycle time of 10ms. To determine when the write is completed, a method called $\overline{DATA}$ Polling is utilized. If a read is performed on the address of the last byte written to the DPE512S8N while a write cycle is in progress, the one's compliment of the most significant bit (I/O7) will appear on the output. When the write is completed, a read from the last address written will return valid data. A $\overline{DATA}$ Polling may begin at any time during the Write Cycle.

ORDERING INFORMATION

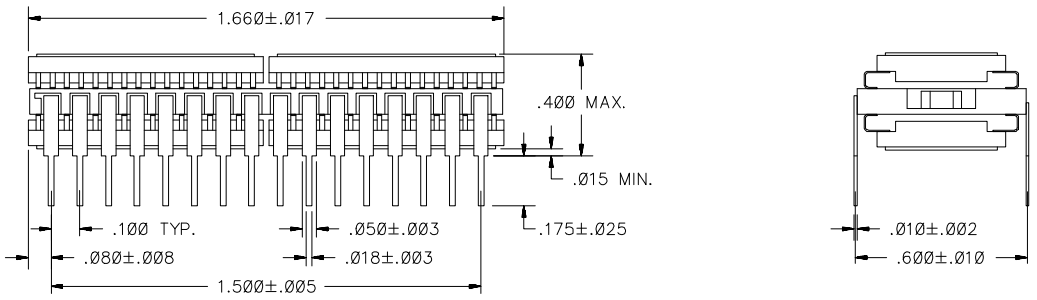


* B grade modules are constructed with 883 devices.

NOTES:

1. All voltages are with respect to V_{SS}.
2. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
3. This parameter is guaranteed and not 100% tested.
4. Address hold time is with respect to the falling edge of the control signal $\overline{WE}$ or $\overline{CE}$.
5. $\overline{WE}$ and $\overline{CE}$ are noise protected. Less than a 15ns write pulse will not activate a write cycle.

MECHANICAL DIAGRAM



Dense-Pac Microsystems, Inc.
7321 Lincoln Way ◆ Garden Grove, California 92841-1428
(714) 898-0007 ◆ (800) 642-4477 (Outside CA) ◆ FAX: (714) 897-1772 ◆ http://www.dense-pac.com