DENSE-PAC MICROSYSTEMS

4 Megabit CMOS EEPROM

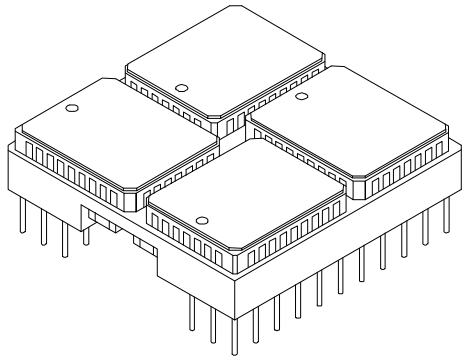
DPE128X32V

DESCRIPTION:

The DPE128X32V is a high-performance Electrically Erasable and Programmable Read Only Memory (EEPROM) module and may be organized as 128K X 32, 256K X 16 or 512K X 8.

The module is built with four low-power CMOS 128K X 8 EEPROMs. The four chip enables are used for individual BWDW* selection. The DPE128X32V is ideally suited for those computer systems having 16-bit or 32-bit architectures.

The DPE128X32V contains a 128-BWDW page register to allow writing of up to 128 BWDWs simultaneously. During a write cycle, the address and 1 to 128 BWDWs of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the module will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ Polling of the most significant data bit in each byte. Once the end of a write cycle has been detected, a new access for a read or write can begin.

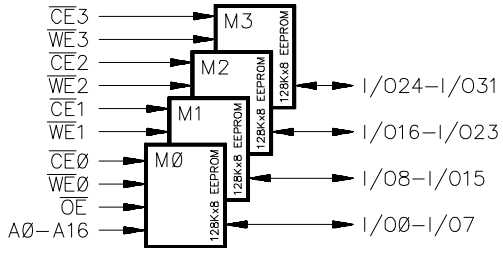


FEATURES:

- Fast Access Times: 120, 150, 200, 250ns
- Organizations Available:
  128K X 32, 256K X 16 or 512K X 8
- Automatic Page Write Operation
  Internal Address and Data Latches
  Internal Control Timer
- Fast Write Cycle Times
  Page Write Cycle Time: 10ms maximum
  1 to 128 BWDW* Page Write Operation
- $\overline{\text{DATA}}$ Polling for END of Write Detection
- High Reliability CMOS Technology
  Endurance: 10^4 Cycles
  Data Retention: 10 years
- Single +5V Power Supply, ±10% Tolerance
- CMOS and TTL Compatible Inputs and Outputs
- Available with All Semiconductor Components used to Construct the Module Compliant to MIL-STD-883; Class B
- 66-Pin PGA (Grid Array) Package
- Same Package as other Versapac Versions (SRAMs, EPROMs, and Mixed)

* Byte, Word or Double Word (BWDW).

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O31	Data In/Out
$\overline{\text{CE}}$0 - $\overline{\text{CE}}$3	Chip Enables
$\overline{\text{WE}}$0 - $\overline{\text{WE}}$3	Write Enables
$\overline{\text{OE}}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

PIN-OUT DIAGRAM

1	I/O8	12	$\overline{\text{WE}}$1	23	I/O15				34	I/O24	45	VDD	56	I/O31
2	I/O9	13	$\overline{\text{CE}}$1	24	I/O14				35	I/O25	46	$\overline{\text{CE}}$3	57	I/OØ
3	I/OØ	14	VSS	25	I/O13				36	I/O26	47	$\overline{\text{WE}}$3	58	I/O29
4	A13	15	I/O11	26	I/O12				37	A6	48	I/O27	59	I/O28
5	A14	16	AØ	27	$\overline{\text{OE}}$				38	A7	49	A3	60	AØ
6	A15	17	A11	28	N.C.		(TOP VIEW)		39	N.C.	50	A4	61	A1
7	A16	18	A12	29	$\overline{\text{WE}}$Ø				40	A8	51	A5	62	A2
8	N.C.	19	VDD	30	I/O7				41	A9	52	$\overline{\text{WE}}$2	63	I/O23
9	I/OØ	20	$\overline{\text{CE}}$Ø	31	I/O6				42	I/O16	53	$\overline{\text{CE}}$2	64	I/O22
10	I/O1	21	N.C.	32	I/O5				43	I/O17	54	VSS	65	I/O21
11	I/O2	22	I/O3	33	I/O4				44	I/O18	55	I/O19	66	I/O20

This document contains information on a product that is currently released to production at Dense-Pac Microsystems, Inc. Dense-Pac reserves the right to change products or specifications herein without prior notice.

RECOMMENDED OPERATING RANGE [1]						
Symbol	**Characteristic**		**Min.**	**Typ.**	**Max.**	**Unit**
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
T_A	Operating Temperature	C	0	+25	+70	°C
		I	-40	+25	+85	
		M/B	-55	+25	+125	

TRUTH TABLE				
Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	**I/I Pin**
Standby	H	X	X	HIGH-Z
Read	L	L	H	D_{OUT}
Write	L	H	L	D_{IN}
Write Inhibit	X	L	X	HIGH-Z
Write Inhibit	X	X	H	HIGH-Z

L = LOW H = HIGH X = Don't Care

ABSOLUTE MAXIMUM RATINGS [1]			
Symbol	**Parameter**	**Value**	**Unit**
T_{STG}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
V_{DD}	Supply Voltage [2]	-0.6 to +6.25	°C
$V_{I/O}$	Input/Output Voltage [2]	-0.6 to +6.25	V

CAPACITANCE [3]: T_A = 25°C, F = 1.0MHz				
Symbol	**Parameter**	**Max.**	**Unit**	**Condition**
C_{CE}	Chip Enable	30	pF	V_{IN} = 0V
C_{ADR}	Address Input	70		
C_{WE}	Write Enable	70		
C_{OE}	Output Enable	70		
$C_{I/O}$	Data Input/Output	30		

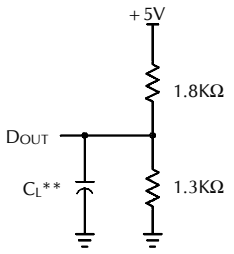
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

* Transition between 0.8V and 2.2V.

OUTPUT LOAD		
Load	**C_L**	**Parameters Measured**
1	100pF	except t_{DF}
2	5pF	t_{DF}

Figure 1. Output Load

** Including Probe and Jig Capacitance.



DC OPERATING CHARACTERISTICS: Over operating ranges									
Symbol	**Characteristics**	**Test Conditions**	**X32**		**X16**		**X8**		**Unit**
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} Max.	-40	+40	-40	+40	-40	+40	µA
I_{OUT}	Output Leakage Current	V_{OUT} = V_{DD} Max.	-10	+10	-20	+20	-40	+40	µA
I_{CC}	Operating Supply Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, all I/O = 0mA, f = 5MHz		320		170		90	mA
I_{SB1}	V_{DD} Standby Current (TTL)	$\overline{CE}$ = V_{IH}		12		12		12	mA
I_{SB2}	V_{DD} Standby Current (CMOS)	$\overline{CE}$ = V_{DD} -0.3Vdc		1.2		1.2		1.2	mA
VIL	Input Voltage Low			0.8		0.8		0.8	V
VIH	Input Voltacge High		2.0		2.0		2.0		V
V_{OL}	Output Voltage Low	I_{OUT} = 2.1mA		0.45		0.45		0.45	V
V_{OH}	Output Voltage High	I_{OUT} = -400µA	2.4		2.4		2.4		V

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges										
No.	Symbol	Parameter	120ns		150ns		200ns		250ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	120		150		200		250		ns
2	t_{CE}	Chip Enable to Output Valid		120		150		200		250	ns
3	t_{ACC}	Address Access Time		120		150		200		250	ns
4	t_{OE}	Output Enable Access Time		50		55		55		55	ns
5	t_{DF}	Chip Enable or Output Enable to Output Float [3]		50		55		55		55	ns
6	t_{OH}	Output Hold from Chip Enable, Output Enable, or Address, Whichever Occurs First	0		0		0		0		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [5, 6]					
No.	Symbol	Parameter	Min.	Max.	Unit
7	t_{WC}	Write Cycle Time		10	ms
8	t_{AS}	Address Set-up Time *	0		ns
9	t_{AH}	Address Hold Time	50		ns
10	t_{CS}	Chip Select Set-up Time	0		ns
11	t_{CH}	Chip Select Hold Time	0		ns
12	t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
13	t_{DS}	Data Set-up Time	50		ns
14	t_{DH}	Data Hold Time	0		ns
15	t_{OES}	Output Enable Set-up Time	0		ns
16	t_{OEH}	Output Enable Hold Time	0		ns
17	t_{WPH}	Write Pulse Width High	50		ns
18	t_{BLC}	Byte Load Cycle Time		150	µs
19	t_{WR}	Write Recovery Time	0		ns

* Valid for both Read and Write Cycles.

READ CYCLE

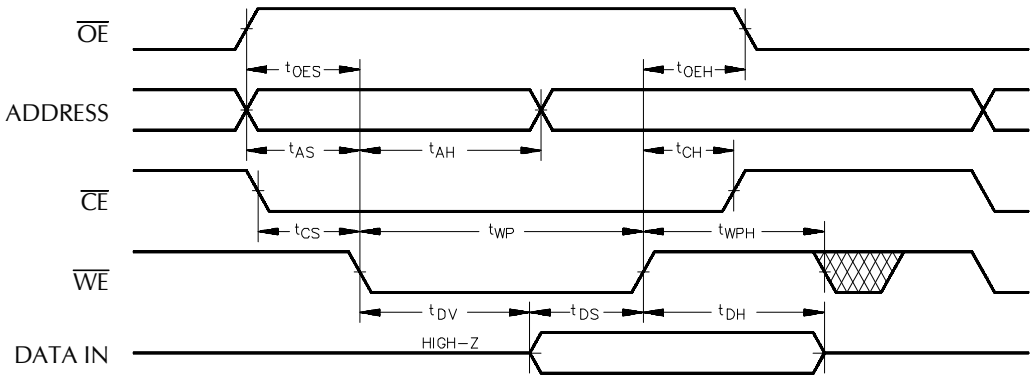
ADDRESS

$\overline{CE}$

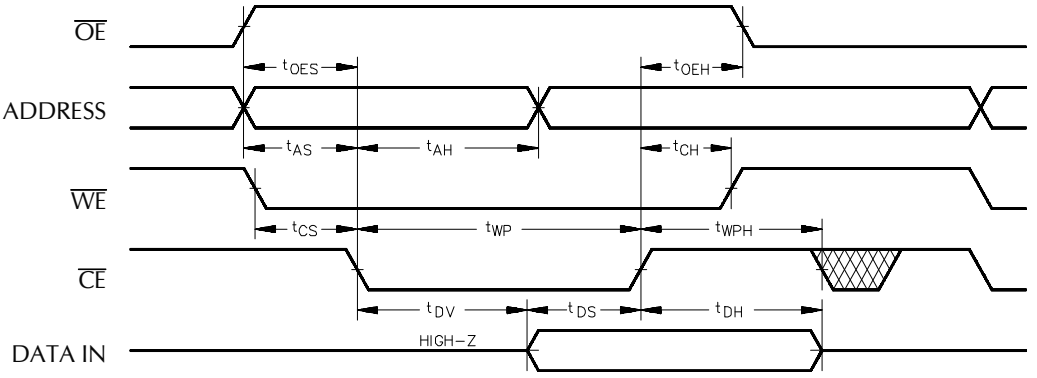
$\overline{OE}$

DATA I/O

WRITE CYCLE 1: $\overline{WE}$ Controlled.



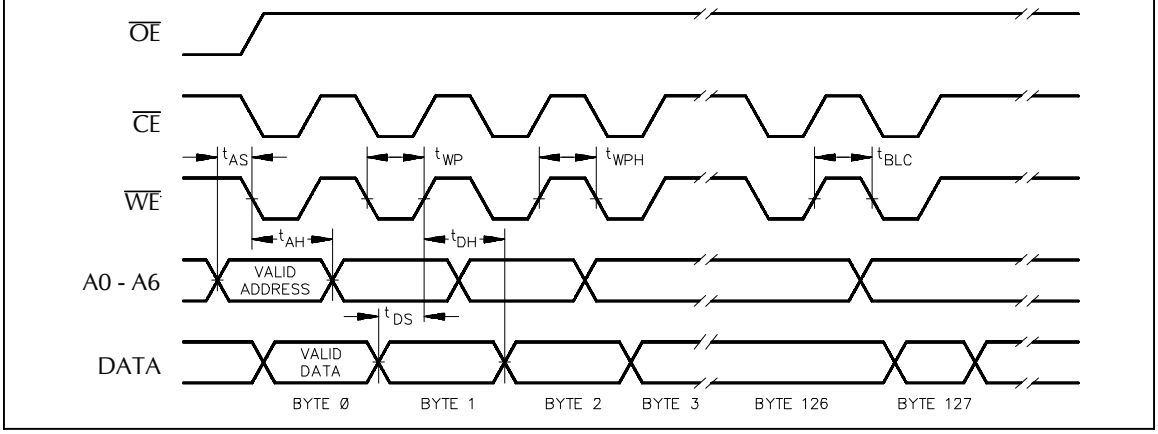
WRITE CYCLE 2: $\overline{CE}$ Controlled.



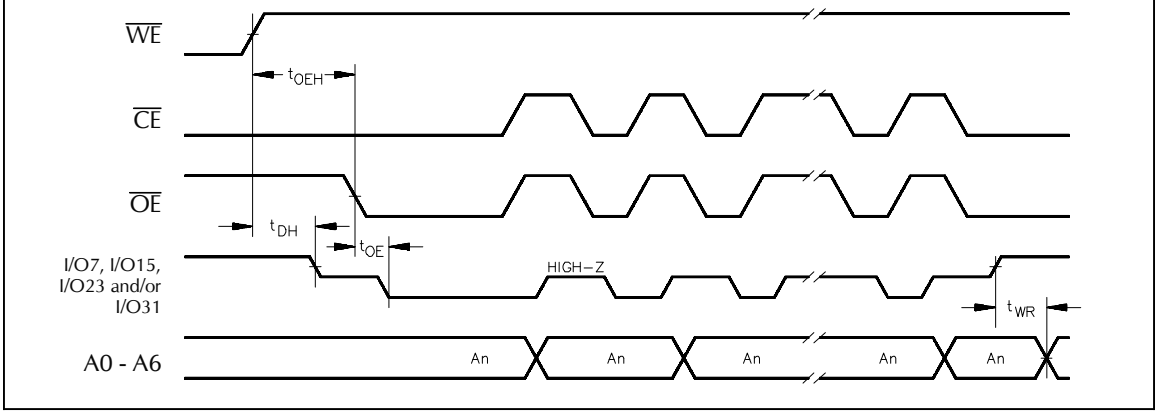
WAVEFORM KEY

Data Valid	Transition from HIGH to LOW	Transition from LOW to HIGH	Data Undefined or Don't Care

PAGE MODE WRITE WAVEFORM



DATA POLLING WAVEFORM



DEVICE OPERATION

READ: The DPE12832V is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$. Once a **BWDW Write has been started it will automatically time itself to completion.

PAGE WRITE: The page write operation of the DPE12832V allows 1 to 128 BWDWs of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data BWDW has been loaded into the device, successive BWDWs may be loaded in the same manner. Each new BWDW to written must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding BWDW. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A16 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 are used to specify which BWDW within the page are to be written. The BWDWs may loaded in any order and may be changed within the same load period. Only BWDWs which are specified for writing will be written; unnecessary cycling of other BWDWs within the page does not occur.

DATA POLLING: Write cycles typically are completed in less time than the maximum write cycle time of 10ms. To determine when the write is completed, a method called DATA Polling is utilized. If a read is performed on the address of the last BWDW written to the DPE12832V while a write cycle is in progress, the one's compliment of data most significant bit (I/O7, I/O15, I/O23 and I/O31) will appear on the output. When the write is completed, a read from the last address written will return valid data. A DATA Polling may begin at any time during the Write Cycle.

** Byte, Word, or Double Word.

ORDERING INFORMATION

DP E 128 X 32 V – XX X

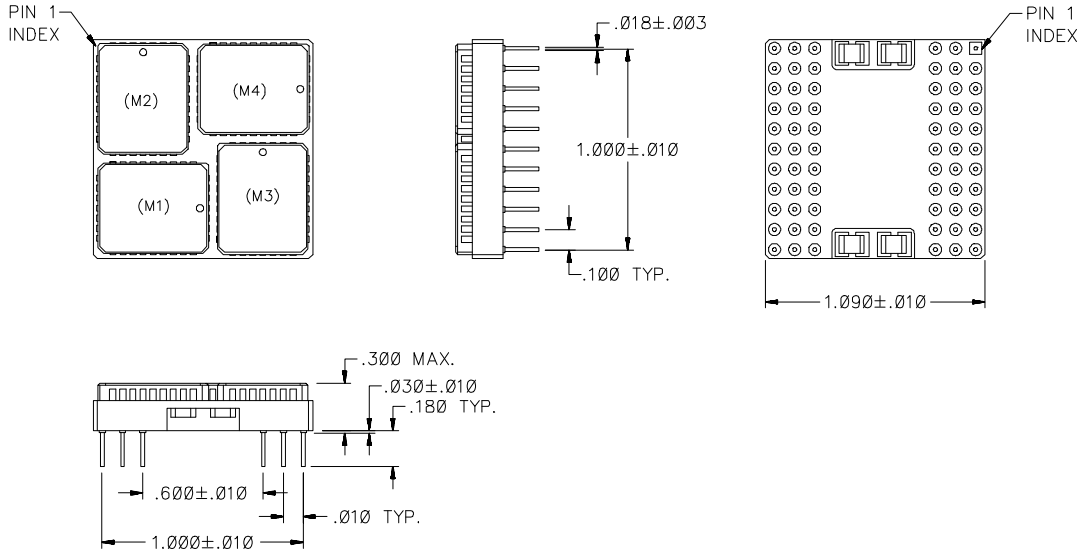
PREFIX			
TYPE			
MEMORY DEPTH			
DESIG			
MEMORY WIDTH			
PACKAGE			
SPEED			
GRADE			
	C	COMMERCIAL	0°C to +70°C
	I	INDUSTRIAL	–40°C to +85°C
	M	MILITARY	–55°C to +125°C
	B*	MIL–PROCESSED	–55°C to +125°C
	12	120ns	
	15	150ns	
	20	200ns	
	25	250ns	
		66–PIN PGA VERSAPAC	
		MODULE WITHOUT SUPPORT LOGIC	
		CMOS EEPROM	

* B grade modules are constructed with 883 devices.

NOTES:

1. All voltages are with respect to V_{SS}.
2. Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
3. This parameter is guaranteed and not 100% tested.
4. Address hold time is with respect to the falling edge of the control signal $\overline{WE}$ or $\overline{CE}$.
5. $\overline{WE}$ and $\overline{CE}$ are noise protected. Less than a 15ns write pulse will not activate a write cycle.

MECHANICAL DIAGRAM



Dense-Pac Microsystems, Inc.
7321 Lincoln Way ◆ Garden Grove, California 92841-1428
(714) 898-0007 ◆ (800) 642-4477 (Outside CA) ◆ FAX: (714) 897-1772 ◆ http://www.dense-pac.com