Device Engineering Incorporated

2102 E. Fifth St.
Tempe, AZ 85281
Phone: (480) 303-0822
Fax: (480) 303-0824
E-mail: admin@deiaz.com

DEI1044
ARINC 429 QUAD LINE RECEIVER

Features:

- Converts ARINC 429 levels to TTL/CMOS digital data.
- Meets requirements of ARINC 429 digital information transfer system standards.
- Inputs internally protected to Lightning requirements of DO-160D level A3.
- Operates at data rates beyond ARINC 429 specifications to 5MHz.
- 5 Volt or 3.3 Volt operation.
- 20L 4.4mm TSSOP Package. Contact factory for additional package options.
- One-half volt receiver hysteresis.
- Operates within ±5 volts common mode input voltage range.
- BiCMOS process
- TTL/CMOS test inputs.

Functional Description:

The DEI1044 is a BICMOS device which contains four differential line receivers. Each receiver channel translates incoming ARINC 429 data bus signals to a pair of TTL/CMOS outputs. Each receiver operates independently, is lightning protected, and meets all requirements of the *ARINC 429 Digital Information Transfer Standard*.

TEST inputs are provided for built in system test. They force the outputs of all receivers to the specified ZERO, ONE or NULL state. The ARINC inputs are ignored when the device is in test mode.

The DEI1044 Quad Line Receiver can be used in conjunction with Device Engineering's family of avionics products in interfacing the ARINC 429 data bus.

Figure 1: DEI1044 Block Diagram – Typical Channel

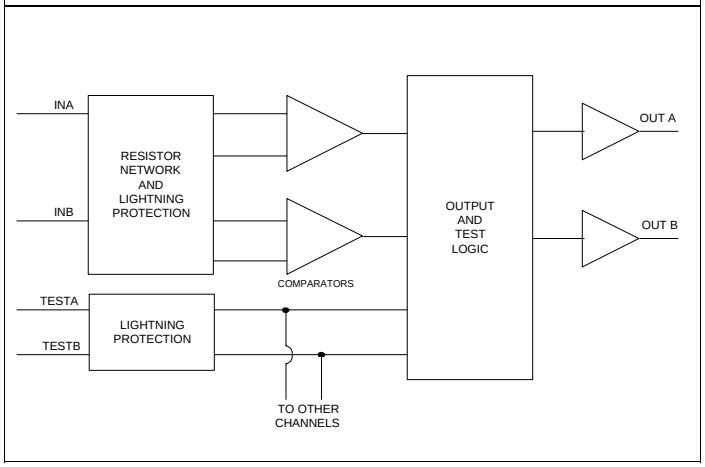


Table 1: DEI1044 Truth Table

INPUTS			OUTPUTS		
TEST INPUTS (TTL/CMOS)		ARINC INPUTS	TTL/CMOS		
TEST A	TEST B	$A_{IN} - B_{IN}$ V	OUT A	OUT B	Logic
0	0	ONE (+10V)	1	0	ONE
0	0	ZERO (-10V)	0	1	ZERO
0	0	NULL (0V)	0	0	NULL
0	1	X	0	1	ZERO
1	0	X	1	0	ONE
1	1	X	0	0	NULL

DS-MP-01044 Rev. C
05/25/01

Table 2: Absolute Maximum Ratings			
PARAMETER	**MIN**	**MAX**	**UNITS**
Supply Voltage (with respect to V_{SS})	-0.3	7.0	V
Operating Frequency		5	MHz
Operating Temperature	-40	+85	°C
Storage Temperature	-55	+150	°C
Input Voltage (ARINC Inputs)	-30	+30	V
Input Voltage (Test Inputs)	V_{SS} – 0.3	V_{DD}+0.3	V
Power Dissipation @ 85 °C		350	mW
Lead Soldering Temperature (10 sec duration)		280	°C
Lightning Protection (ARINC 429 Channel Inputs and TESTA/TESTB Inputs) Waveform 3* Waveform 4 and 5* *Per DO160D level 3A See figures 7-9.	 -600 -300	 +600 +300	 V V
Caution: Stresses above these limits can cause permanent damage.			
The DEI1044 contains circuitry to protect inputs against damage due to high voltage static discharge. It has been characterized per JEDEC A114-A Human Body Model to Level 1 (1KV ioimmunity). Observe precautions for handling and storing Electrostatic Sensitive Devices.			

Table 3: Recommended Operating Conditions		
PARAMETER	**SYMBOL**	**CONDITIONS**
Supply Voltage	Vcc	+5V ± 10% +3.3V ± 10%
Logic Input Levels	$V_{TESTA,B}$	0 to Vcc

Table 4: Package Thermal Characteristics	
20 TSSOP: Theta JC Theta JA—Four Layer PCB w/ Solid Plane per JEDEC JC15.1	 17 °C/W 90 °C/W

20 TSSOP
TOP VIEW

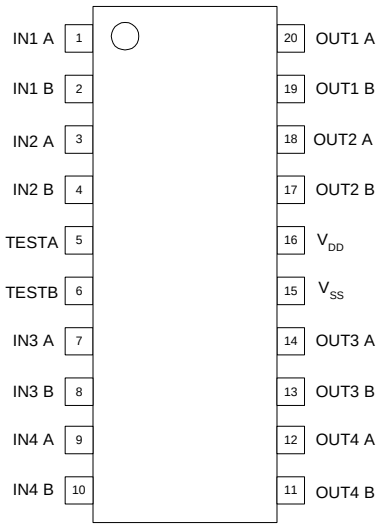


Figure 2: DEI1044 Pinout

Electrical Characteristics:

Table 5: Electrical Characteristics						
Conditions: Temperature: -40°C to +85°C; V_{DD} = +5V ± 10% or 3.3V ± 10%						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN**	**NOM**	**MAX**	**UNITS**
ARINC INPUTS						
$V_A - V_B$	OUT A = 1	V_{HI}	6.5	10	13	V
$V_A - V_B$	OUT B = 1	V_{LO}	-6.5	-10	-13	V
$V_A - V_B$	OUT A = 0 OUT B = 0	V_{NULL}	-2.5	0	2.5	V
Input Resistance IN_A to IN_B	V_{DD} open, Shorted to V_{SS} or +5V	R_{IN}	12k			Ω
Input Resistance IN_A or IN_B to V_{SS}	V_{DD} open, Shorted to V_{SS} or +5V	R_S	12k			Ω
Input Hysteresis			0.5	1.0		V
Input Capacitance IN_A to IN_B	V_{DD} open, Shorted to V_{SS} or +5V	C_{IN}			50	pF
Input Capacitance IN_A or IN_B to V_{SS}	V_{DD} open, Shorted to V_{SS} or +5V	C_S			50	pF
Input Common Mode Voltage	V_{HI}, V_{LO}, V_{NULL} Within limits	V_{CM}	-5		+5	V
TEST INPUTS						
Logic 0 Voltage		V_{IL}			0.8	V
Logic 1 Voltage		V_{IH}	2.0			V
Logic 0 Current	V_{IL} = 0.8	I_{IL}			1	µA
Logic 1 Current	V_{IH} = 2.0	I_{IH}			20	µA
OUTPUTS						
OUT A or OUT B	I_{OH} = 5mA, V_{dd}= 5V (1) I_{OH} = 4mA, V_{dd}= 3.3V	V_{OH}	2.4			V
OUT A or OUT B	I_{OL} = 5mA, V_{dd}= 5V (1) I_{OL} = 1.5mA, V_{dd}= 3.3V	V_{OL}			0.4	V
OUT A or OUT B	I_{OH} = 100µA (1) CMOS Compatible	V_{OH}	V_{DD} – 50mV			V
OUT A or OUT B	I_{OL} = 100µA (1) CMOS Compatible	V_{OL}			V_{SS} + 50mV	V
SUPPLY CURRENT						
V_{DD} Current	A/B IN open A/B OUT open	I_{DD}		5.5	11	mA
SWITCHING CHARACTERISTICS (1)						
			Max 3.3V		Max 5V	
Prop Delay IN A/B to OUT A/B	TESTA = TESTB = 0	t_{LH}	95		55	nsec
Prop Delay IN A/B to OUT A/B	TESTA = TESTB = 0	t_{HL}	70		45	nsec
OUT A/B rise time	10% to 90%	t_r	50		35	nsec
OUT A/B fall time	10% to 90%	t_f	25		15	nsec
TESTA/B to OUT A/B Prop delay		t_{TOH}	90		50	nsec
TESTA/B to OUT A/B Prop delay		t_{TOL}	90		50	nsec

1. Parameter guaranteed by design and is not 100% tested.

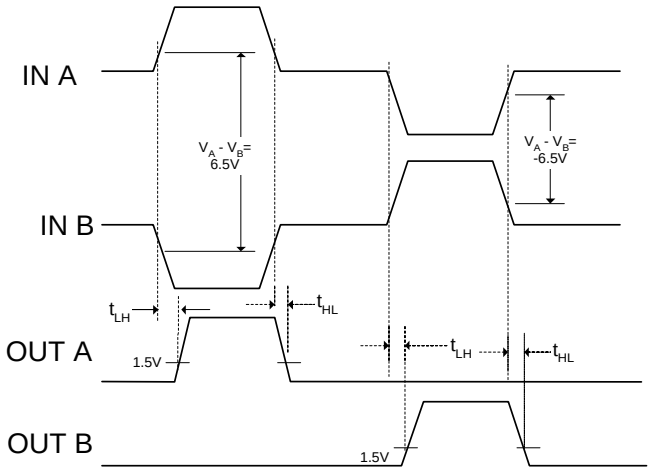


Figure 3: DEI1044 Timing Diagram

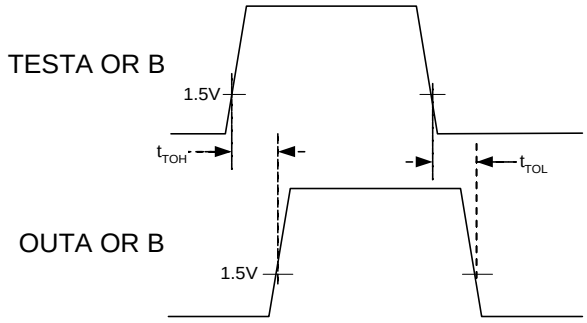


Figure 4: DEI1044 Propagation Delay

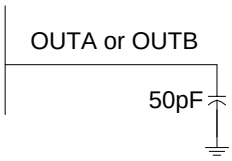


Figure 5: DEI1044 Output Loading

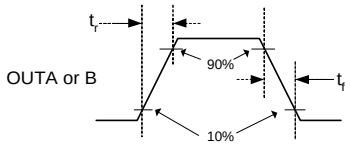


Figure 6: DEI1044 Rise/Fall Time

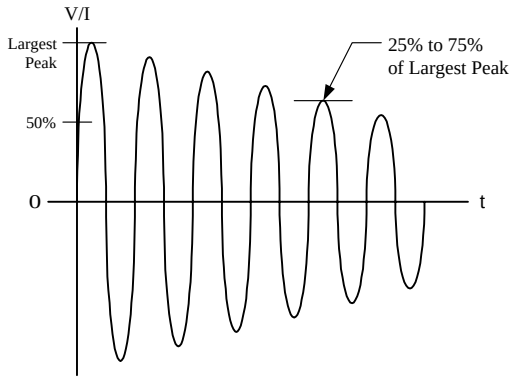


Figure 7: DO160C/D Voltage Waveform #3
V_{OC} = 600V, I_{SC} = 24A, Frequency = 1.0MHZ ±20%

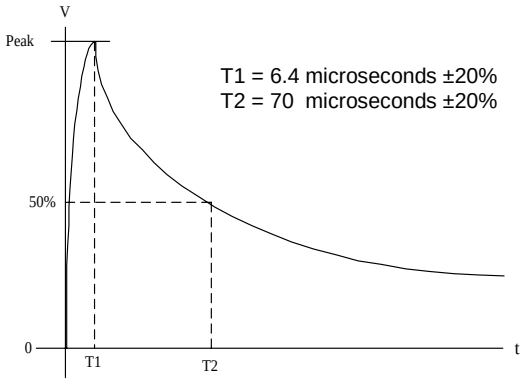


Figure 8: DO160C/D Voltage Waveform #4
V_{OC} = 300V, I_{SC} = 60A

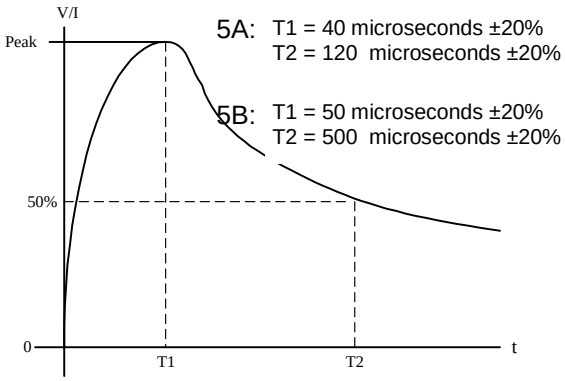
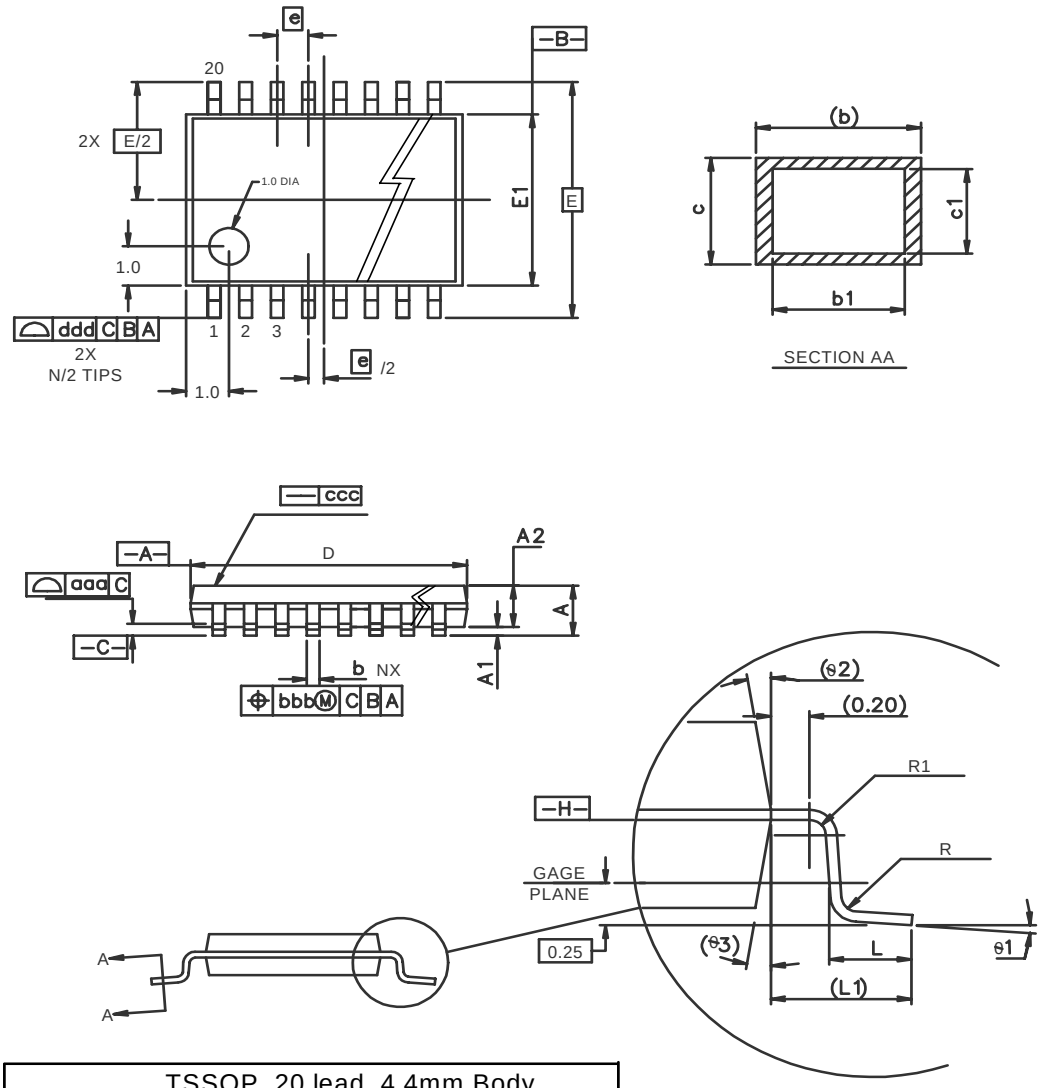


Figure 9: DO160C/D Voltage Waveform #5
V_{OC} = 300V, I_{SC} = 300A

Notes:

1. V_{OC} = Peak Open Circuit Voltage available at the calibration point.
2. I_{SC} = Peak Short Circuit Current available at the calibration point.
3. Amplitude tolerances: +10%, -0%
4. The ratio of V_{OC} to I_{SC} is the generator source impedance to be used for genera-



TSSOP, 20 lead, 4.4mm Body					
SYMBOL	DIMENSION (MILLIMETERS)			SYMBOL	DIMENSION (MILLIMETERS)
	MIN	NOM	MAX		NOM
A	---	---	1.10	L1	1.0 REF
A1	0.05	---	0.15	aaa	0.10
A2	0.85	0.90	0.95	bbb	0.10
L	0.50	0.60	0.75	ccc	0.05
R	0.09	---	---	ddd	0.20
R1	0.09	---	---	e	0.65 BSC
b	0.19	---	0.30	θ2	12° REF
b1	0.19	0.22	0.25	θ3	12° REF
c	0.09	---	0.20		
c1	0.09	---	0.16		
θ1	0°	---	8°	E	6.4 BSC
D	6.40	6.50	6.60	e	0.65 BSC
E1	4.30	4.40	4.50	N	20

Figure 10: DEI 20 Lead TSSOP Package Dimensions
JEDEC MO-153-AC