Direct Rambus™ Clock Generator-Lite

Overview

The Direct Rambus™ Clock Generator-Lite (DRCG-Lite) provides the necessary clock signals to support a Direct Rambus memory subsystem using a low cost crystal input. Contained in a 16-pin TSSOP package, the DRCG-Lite provides an off-the-shelf solution for a broad range of Direct Rambus® memory applications, such as PC and workstation main memory, graphics frame buffers, and communications buffer memory.

Features

- High speed clock support
  300-400 MHz clock source for Direct Rambus memory systems supports up to a 1.6 GB/sec data transfer rate
- Single differential output driver with less than 50ps short term jitter
- 18.75 MHz crystal input
- Supports frequency multipliers: 16 and 64/3.
- Second LVCMOS output (LCLK) which runs at 1/2 the crystal frequency
- Supports independent channel clocking
  Supports systems not requiring synchronization of the Rambus clock to another system clock
- Active power < 350mW; Vdd = 3.3V ± 10%
- Output edge rate control to minimize EMI

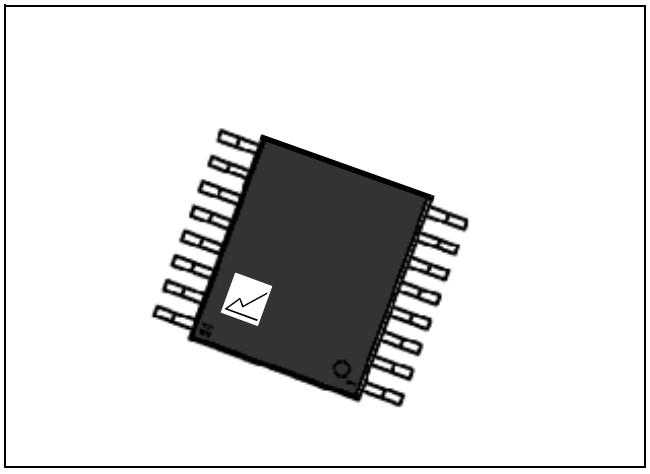

Figure 1: Direct Rambus Clock Generator-Lite Package

Related Documentation

Data sheets for the Rambus memory system components, including the Rambus DRAMs, RIMM™-Module, RIMM connector are available on the Rambus web site at http://www.rambus.com.

The DRCG-Lite is packaged in a 16-pin 225mil TSSOP. Figure 2 shows the pin assignments. Table 1 describes the function and connection of each pin.

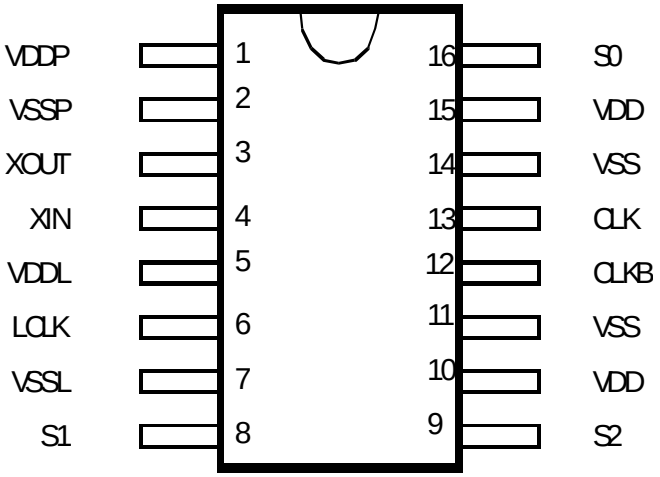

Figure 2: DRCG-Lite Pin-out

Table 1. DRCG-Lite Pin-Out

Pin#	Signal	Type	Function	Notes
1	VDDP	Pwr	Power Supply for PLL	3.3V Supply
2	VSSP	Pwr	Ground for PLL	Ground
3	XOUT	-	Reference Crystal Feedback	
4	XIN	-	Reference Crystal Input	
5	VDDL	Pwr	Power Supply for LCLK	1.8V Supply
6	LCLK	Out	LVCMOS Output	1/2 of Crystal Frequency
7	VSSL	Pwr	Ground for LCLK	Ground
8	S1	I/O	Test	Vendor Specific[a]
9	S2	I/O	Test	Vendor Specific[a]
10	VDD	Pwr	Power Supply	3.3V Supply
11	VSS	Pwr	Ground	Ground
12	CLKB	Out	Output Clock (complement)	Connect to Rambus Channel
13	CLK	Out	Output Clock	Connect to Rambus Channel
14	VSS	Pwr	Ground	Ground
15	VDD	Pwr	Power Supply	3.3V Supply
16	S0	In	PLL Multiplier Select	Pull-up Resistor Inside

a. Test pins S1 and S2 should be left floating during normal operation.

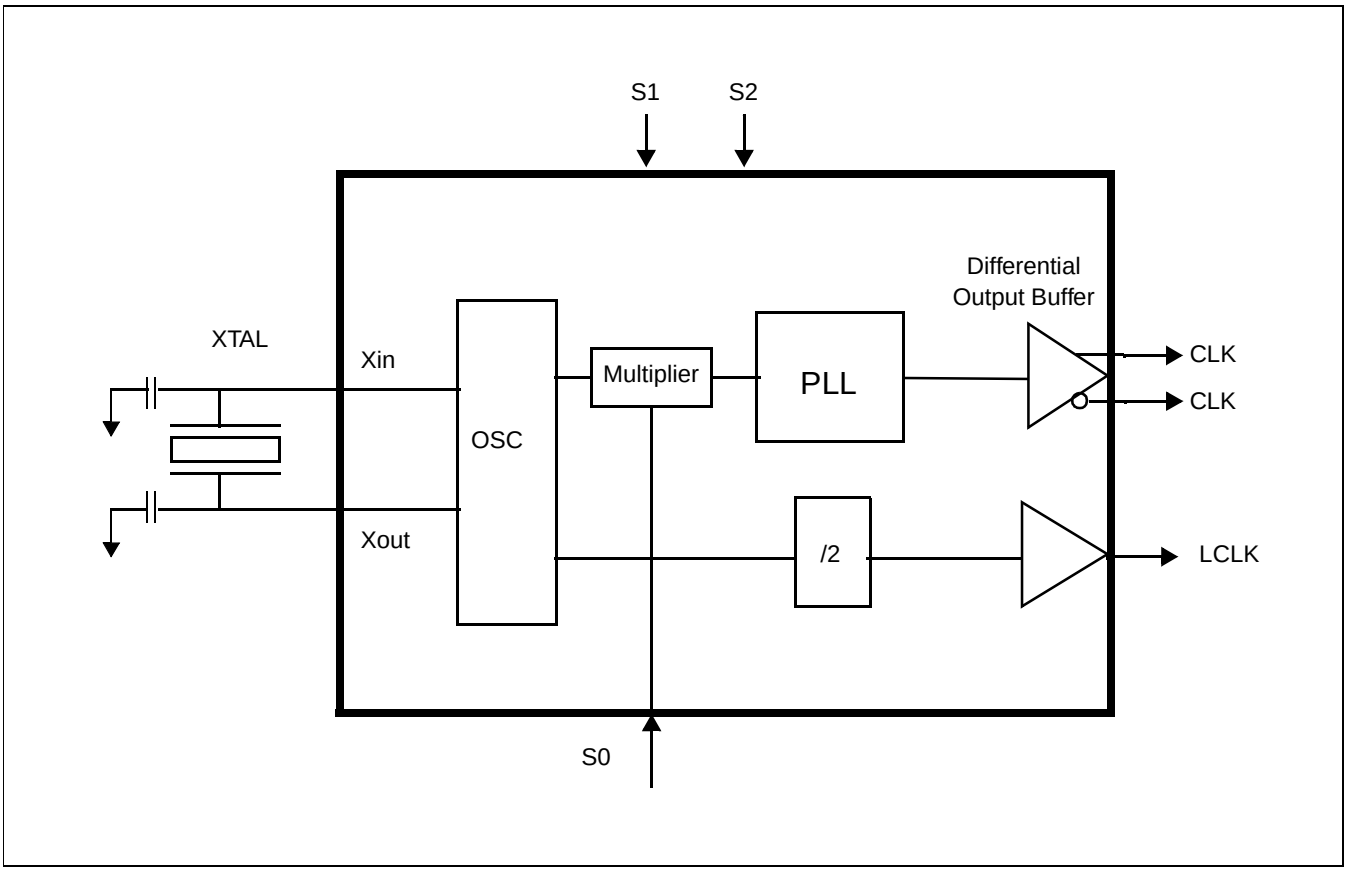

Figure 3: Direct Rambus Clock Generator-Lite Block Diagram

General Description

Figure 3 shows the block diagram of the DRCG-Lite. The major blocks of the DRCG-Lite include a Phase Lock Loop, a Differential Output Buffer, and an LVCMOS output buffer.

The DRCG-Lite receives its reference from an external crystal. Pin XIN is the reference crystal input, and pin XOUT is the reference crystal feedback. As the capacitor is external, please contact crystal manufacturer for the specific capacitor value. The S0 pin controls the multiply ratio for the PLL. The multiply ratio values for S0 are shown in Table 2 and described in the PLL Multiplier section.

The Differential Output Buffer (CLK and CLKB) supplies the 300-400 MHz clock for the Rambus system and is impedance matched to the Rambus Channel transmission line.

The LVCMOS output buffer (LCLK) is a reference clock that operates at 1/2 the crystal input frequency and can be used by other parts of the system. It is not used in the Rambus memory system.

The S1 and S2 input pins are used for test mode purposes only. Please contact the specific DRCG-Lite manufacturer for further information on how the S1 and S2 pins should be used.

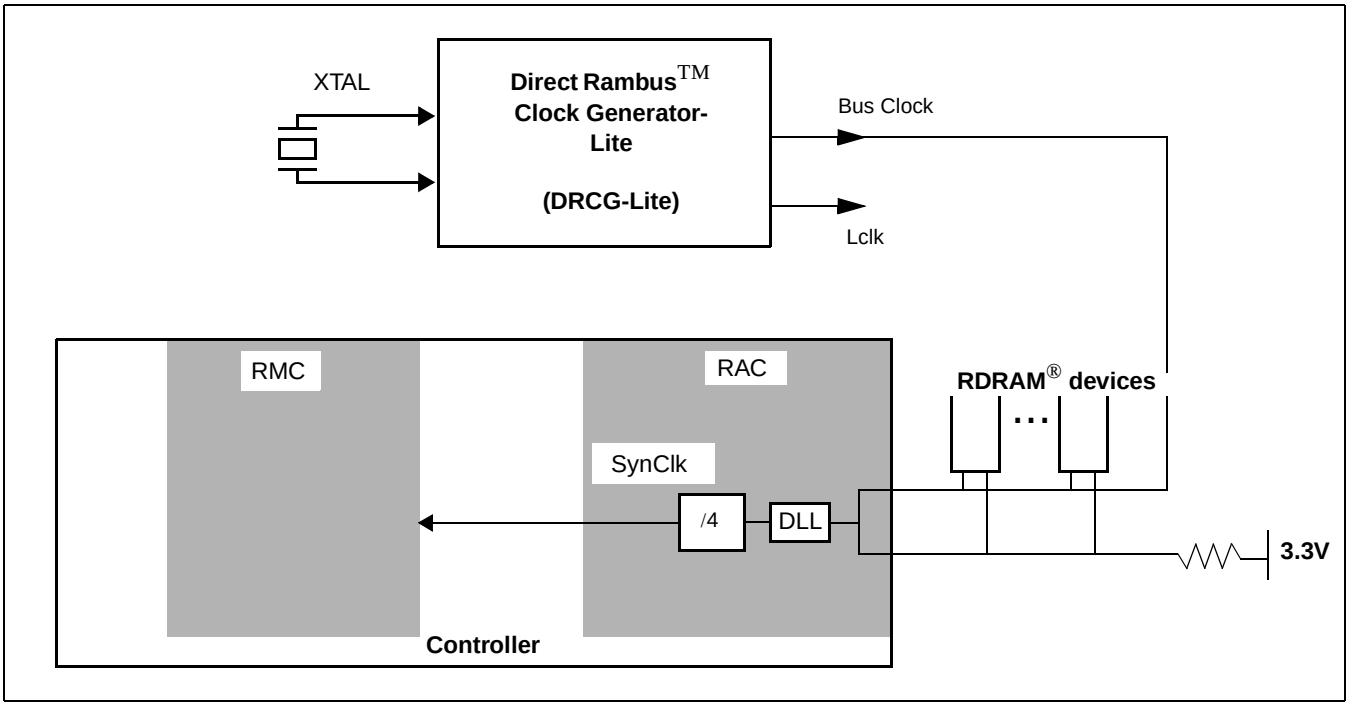

Figure 4: System Clock Architecture

Example System Clock Configuration

Figure 4 shows the clocking configuration for an example single channel Direct Rambus DRAM subsystem. The configuration shows the interconnection of the system clock source, the Direct Rambus Clock Generator-Lite (DRCG-Lite), and the clock signals of a memory controller. The controller contains the Rambus ASIC Cell (RAC) and the Rambus Memory Controller (RMC). (The diagram represents the differential clock outputs. CLK and CLKB, as a single Bus Clock wire.)

A crystal is used as the input reference frequency. A PLL inside the DRCG-Lite generates the desired frequency for Bus Clock. Bus Clock is driven on the Rambus Channel through a terminated transmission line. At the mid-point of the Channel, the RAC senses Bus Clock using its own DLL for clock alignment, followed by a fixed divide-by-4 circuit that generates SynClk. SynClk is the clock used at the ASIC interface of the RAC.

The DRCG-Lite also contains an additional LVCMOS output, Lclk, which provides a reference clock at 1/2 of the crystal frequency. This clock can be used by other blocks in a system, but is not used in the memory subsystem.

PLL Multiplier

Table 2 shows the frequency multipliers in the PLL, selected via the S0 input. The S0 pin is a standard 3.3v LVCMOS input with an internal pullup resistor.

Table 2. PLL Multiplier Selection

S0	M (PLL Multiplier)
0	16
1 or open	64/3

Test Modes

The select bits, S1 and S2, control the selection of test modes. These modes are vendor specific. Please contact vendor for information. S1 and S2 are left floating during normal operation.

State Transition Latency

Table 3 specifies the maximum settling time of the CLK, CLKB and LCLK outputs from device power-up.

For VDD, VDDP and VDDL, any sequence is allowed to power-up and power-down the DRCG-Lite.

Table 3. State Transition Latency

From	To	Transition Latency	Description
VDD/VDDL/VDDP on	CLK/CLKB/LCLK Normal	3 mS	Time from VDD/VDDL/VDDP is applied and settled to CLK/CLKB/LCLK outputs settled.

Device Parameters

This section specifies the numerical values of the physical parameters described earlier in this data sheet.

The DRCG clock source meets the device characteristics listed in Table 7 and Table 10 when characterized under the operating conditions listed in Table 6 and Table 8, and when using the components shown in Figure 5, and the corresponding component values given in Table 11.

Only the DC specifications of Table 7 apply while in Test mode. The AC specifications of Table 10 (see Logical Specification Section for mode descriptions) do not apply while in Test mode unless specified.

Absolute Maximums

Table 4 represents stress ratings only, and functional operation at the maximum settings is not guaranteed.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{DD,ABS}$	Max voltage on V_{DD} with respect to ground	-0.5	4.0	V
$V_{I,ABS}$	Max voltage on any pin with respect to ground	-0.5	V_{DD}+ 0.5	V
$V_{iL,ABS}$	Max voltage on LCLK with respect to ground	-0.5	V_{DD}+ 0.5	V

Supply Current Characteristics

The current drawn through the V_{DD} pins is specified in Table 5. This includes the total current through all V_{DD}, V_{DD}P, and V_{DD}L pins.

Table 5. Supply Current Characteristics

Symbol	Parameter	Min	Max	Unit
I_{NORMAL}	Current in Normal state		100	mA

DC Operating Conditions

This section specifies input conditions for operating the device. When operated outside these limits, device characteristics are undefined.

Table 6. DC Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage	3.04	3.56	V
V_{DDL}	LCLK Supply voltage[a]	1.7	2.1	V
T_A	Ambient operating temperature	0	70	°C
V_{IL}	Input signal low voltage at pin S	-	0.35	V_{DD}
V_{IH}	Input signal high voltage at pin S	0.65	-	V_{DD}
R_{PUP}	Internal pull-up resistance	10	100	kΩ

a VDDL should be tied to ground if LCLK is not used

DC Characteristics

This section specifies the device characteristics when using the external circuits as shown in Figure 5 with component values listed in Table 11.

Table 7. DC Device Characteristics

Symbol	Parameter	Min	Max	Unit
V_X	Differential output crossing-point voltage	1.3	1.8	V
V_{COS}	Output voltage swing (p-p single-ended)[a]	0.4	0.7	V
V_{OH}	Output high voltage	-	2.1	V
V_{OL}	Output low voltage	1.0	-	V
r_{OUT}	Output dynamic resistance (at pins)[b]	12	50	Ω
V_{LOH}	LCLK Output high voltage at IOH = -10mA	VDDL - 0.45V	VDDL	V
V_{LOL}	LCLK Output low voltage at IOL = 10mA	0	0.45V	V

a. $V_{COS} = V_{OH} - V_{OL}$. Measured on external divider shown in Figure 5.
b. $r_{OUT} = DV_O / DI_O$. This is defined at the output pins.

AC Operating Conditions

This section specifies input AC conditions for operating the device. When operated outside these limits, device characteristics are undefined.

Table 8. AC Operating Conditions

Symbol	Parameter	Min	Max	Unit
$f_{XTAL,IN}$	Input frequency at crystal input[a]	14.0625	18.75	MHz
$C_{IN,CMOS}$	Input capacitance at S0 pin[b]	-	10	pF

a. Nominal condition with 18.75MHz crystal
b. Capacitance measured at Frequency= 1MHz, DC bias = 0.9V, and V_{AC} < 100mV

Crystal Requirements

Table 9 Gives the specifications of the recommended crystal to be used with the DRCG-Lite clock source. The mode of oscillation is fundamental.

Table 9. Crystal Specifications

Symbol	Parameter	Min	Max	Unit
X_F	Frequency	14.0625	18.75	MHz
X_{FTOL}	Frequency Tolerance[a]	-100	100	ppm
X_{EQRES}	Equivalent Resistance[b]		100	Ω
X_{TEMP}	Temperature Drift[c]		10	ppm
X_{DRIVE}	Drive Level	0.01	1500	uW
X_{MI}	Motional Inductance	20.7	25.3	mH
X_{IR}	Insulation Resistance	500		MΩ
X_{SAR}	Spurious Attenuation Ratio[d]	3		dB
X_{OS}	Overtone Spurious	8		dB

a. At 25^oC + / - 3^oC
b. CL = 10pF
c. -10^oC to 75^oC
d. At X_F + / - 500 kHz

AC Characteristics

Table 10 gives the AC characteristics for device operation using the external circuits as shown in Figure 5 with component values listed in Table 11.

Table 10. AC Device Characteristics

Symbol	Parameter	Min	Max	Unit
t_{CYCLE}	Clock cycle time	2.5	3.33	ns
t_J	Jitter over 1-6 clock cycles at 400MHz[a]	-	50	ps
	Jitter over 1-6 clock cycles at 300MHz[a]	-	70	ps
t_{JL}	Long-term Jitter at 400MHz	-	300	ps
	Long-term Jitter at 300MHz	-	400	ps
DC	Long-term average output duty cycle	40%	60%	t_{CYCLE}
$t_{DC,ERR}$	Cycle-to-cycle duty cycle error at 400MHz	-	50	ps
	Cycle-to-cycle duty cycle error at 300MHz	-	70	ps
t_{CR}, t_{CF}	Output rise and fall times (measured at 20% - 80% of output voltage)	120	400	ps
$t_{CR,CF}$	Difference between output rise and fall times on the same pin of a single device (20% - 80%)	-	100	ps
BW_{LOOP}	PLL Loop Bandwidth	50 kHz (-3dB)	8 MHz (-20dB)	
$t_{CYCLE,L}$	LCLK Clock cycle time	106.6	142.2	ns
t_{LR}, t_{LF}	LCLK output rise and fall time	-	1	ns
$t_{JC,L}$	LCLK cycle jitter[b]	-0.8	0.8	ns
DC_L	LCLK output duty cycle	40%	60%	$t_{CYCLE,L}$

a. Output short-term jitter spec is the absolute value of the worst case +/- deviation and is defined in the Jitter section.
b. LCLK cycle jitter is defined as the difference between the *measured* period and the nominal period as defined in the Jitter section.

Clock Output Driver

Figure 5: Example System Clock Driver Equivalent Circuit

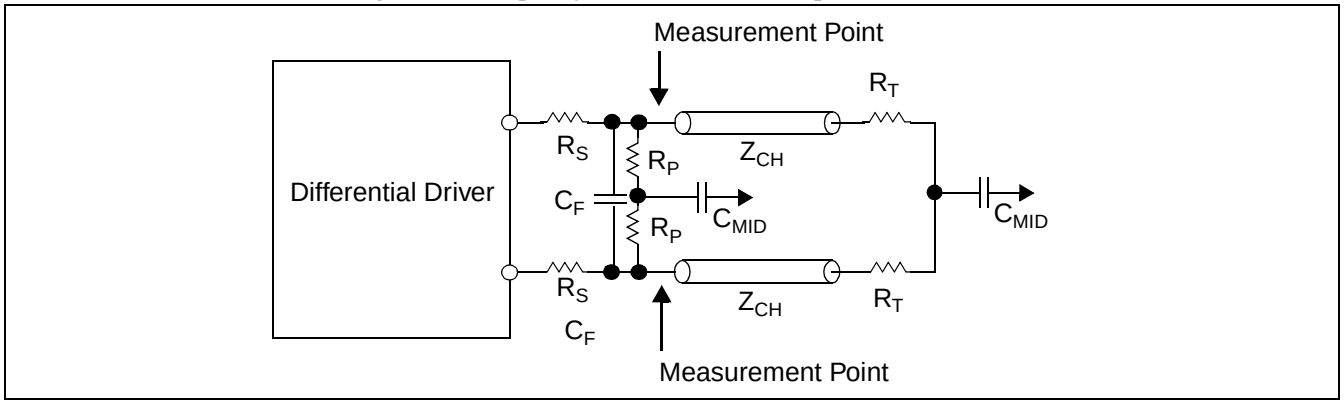

Figure 5 shows the clock driver equivalent circuit. The differential output clock driver of the DRCG has a low output impedance in the range of about 20 ohms. The driver produces the specified voltage swing on the channel, and also matches the channel impedance. The nominal value of the channel impedance, Z_{CH}, is expected to be 28-40 ohms for a Rambus memory subsystem. External series resistors R_S and parallel resistors R_P are used to set the voltage swing on the channel. The driver output characteristics are defined together with the external components, and the output clock is specified at the measurement point indicated in Figure 5. The complete set of external components for the output driver circuit, including edge-rate filter capacitors is also shown in the figure and example values for the external components are shown in Table 11.

The clock driver is specified as a black-box at the package pins. The output characteristics are measured after the series resistance, R_S. The outputs are terminated differentially at the end of the transmission line, with no applied termination voltage.

The clock driver's output impedance, r_{OUT}, is in series with R_S, and the combination is in parallel with R_P. The resulting effective impedance must match the channel impedance in order to minimize secondary reflections. To accomplish this, each of the four CMOS output devices is designed to have an r_{OUT} of about 20 ohms when fully turned on. r_{OUT} is the dynamic output resistance. Since r_{OUT} is in series with R_S, and that combination is in parallel with R_P, the effective output impedance is given by:

$$R_P (R_S + r_{OUT}) / (R_P + R_S + r_{OUT})$$

This calculation results in an effective output impedance of about 27 ohms for the example values listed in Table 11. Since the total impedance is dominated by the external resistors, a large variation in the on-chip value of r_{OUT} is allowed. When the output is transitioning, the impedance of the CMOS devices increases dramatically. The purpose of R_P is to limit the maximum output impedance during output transitions.

In order to control signal attenuation and EMI, clock signal rise / fall times are tightly controlled. External filter capacitors C_F could be used to control the output slew rate. In addition, the capacitor C_{MID} is used to provide AC ground at the mid-point of the R_P and the R_T resistors.

Table 11 gives the nominal values of the external components and their maximum acceptable tolerance, assuming Z_{CH} = 28 ohms for the example Rambus memory subsystem. These values apply to DRCG testboards. For motherboard values, see the system physical design guide.

Table 11. Example External Component Values

Symbol	Parameter	Value	Tolerance	Unit
R_T	Termination resistor	28	± 1%	Ω
R_S	Series resistor	68	± 5%	Ω
R_P	Parallel resistor	39	± 5%	Ω
C_F	Edge-Rate Filter Capacitor[a]	4-10	± 10%	pF
C_{MID}	AC Ground Capacitor	100	± 20%	pF

a: C_F is optional and can be used to control output slew rate and EMI if necessary. For the DRCG-Lite characterization board, no discrete capacitor filter is used.

Output Driver Characteristics

Table 12 gives example V/I characteristics for the differential clock output drivers at the pins of the DRCG-Lite. The sign on all current parameters (direction of current flow) is referenced to a ground inside the component; i.e. positive currents flow into the component. These example V/I characteristics can be used for generating simulation models of the DRCG-Lite (such as IBIS models). Table 12 provides examples values and does not represent additional specifications.

Table 12. Output Buffer V/I Characteristics

Voltage (V)	Pull-Down			Pull-Up		
	I (mA)	I (mA)	I (mA)	I (mA)	I (mA)	I (mA)
	Min	Typ	Max	Min	Typ	Max
0	0	0	0	-35	-55	-91
0.2	8.3	11.9	17.6	-34	-55	-90
0.4	15.8	22.8	33.6	-34	-54	-89
0.6	22.5	32.5	47.9	-33	-53	-87
0.8	28.3	41.0	60.3	-33	-52	-86
1.0	33	48	71	-32	-51	-84
1.2	37	54	79	-31	-50	-82
1.4	41	59	85	-30	-48	-79
1.6	43	62	90	-28	-46	-77
1.8	44	64	92	-27	-43	-73
2.0	45	65	93	-24	-40	-68
2.2	45	66	94	-21	-36	-62
2.4	46	66	95	-17.7	-31.1	-55.0
2.6	46	67	95	-13.6	-25.4	-46.7
2.8	46	67	95	-8.9	-19.0	-37.6
3.0	46	67	96	-3.7	-11.9	-27.4
3.135	46	67	96	0	-6.7	-19.9
3.3		67	96		0	-10.3
3.465			96			0

Signal Waveforms

A physical signal which appears at the pins of a device is deemed valid or invalid depending on its voltage and timing relations with other signals. Input and output voltage waveforms are defined as shown in Figure 6. Both rise and fall times are defined between the 20% and 80% points of the voltage swing, with the swing defined as V_H - V_L. For example, the output voltage swing $V_{COS} = V_{OH} - V_{OL}$

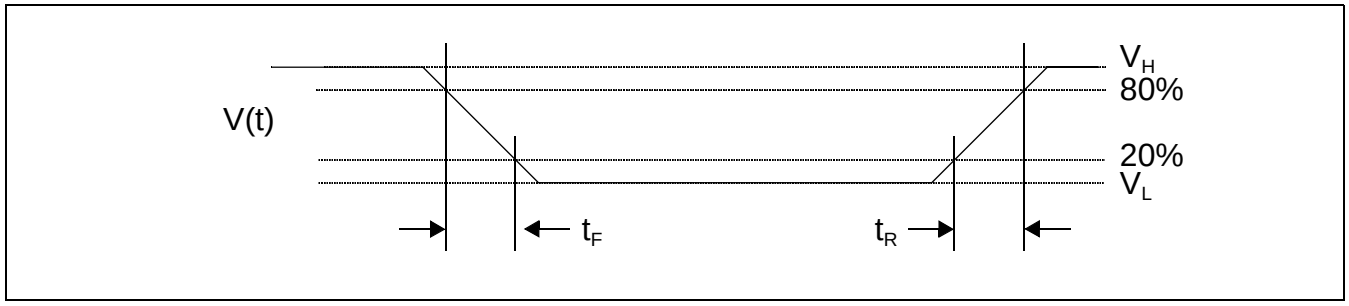

Figure 6: Input and Output Voltage Waveforms

Figure 7 shows the definition of output crossing point. The nominal crossing point between the complementary outputs is defined to be at the 50% point of the DC voltage levels. There are two crossing points defined, Vx+ at the rising edge of CLK and Vx- at the falling edge of CLK. For some clock waveforms, both Vx+ and Vx- might be below Vx,nom (for example, if t_{CR} is larger than t_{CF}).

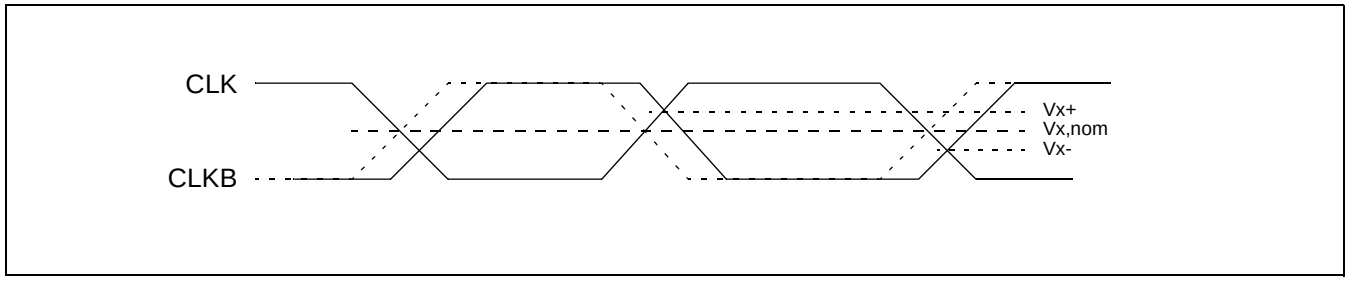

Figure 7: Crossing-point Voltage

Figure 8 shows the definition of long-term duty cycle, which is simply the waveform high-time divided by the cycle time (defined at the crossing point). Long-term duty cycle is the average over many (>10,000) cycles. Short-term duty cycle is defined in Figure 10.

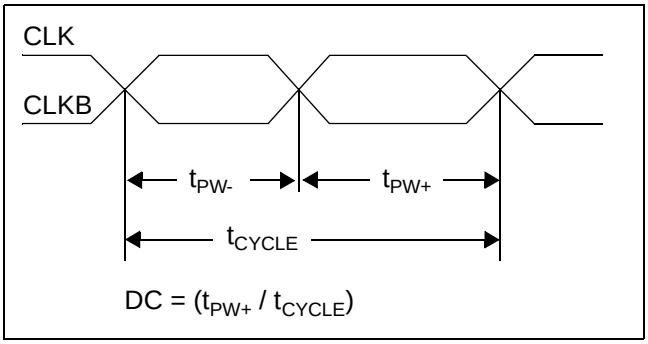

Figure 8: Duty Cycle

Jitter

This section defines the specifications that relate to timing uncertainty (or jitter) of the input and output waveforms. Figure 9 shows the definition of cycle-to-cycle jitter with respect to the falling edge of the CLK signal. Cycle-to-cycle jitter (also called 1-cycle short term jitter) is the difference between cycle times of adjacent cycles. Equal requirements apply for rising edges of the CLK signal.

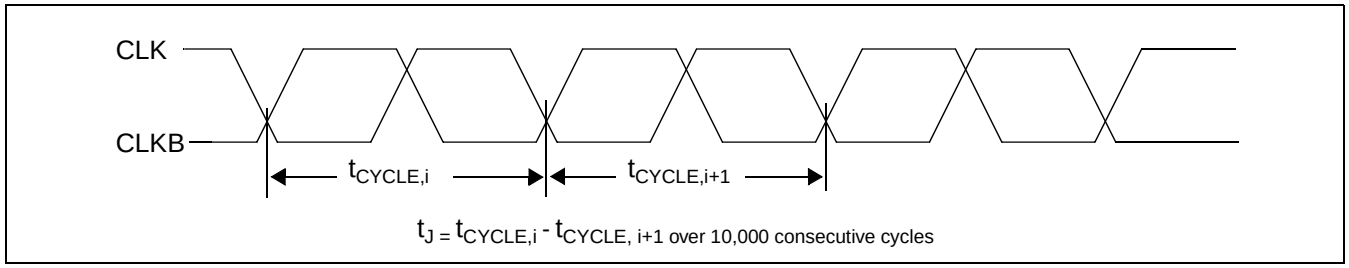

Figure 9: Cycle-to-cycle Jitter

Figure 10 shows the definition of 4-cycle short-term jitter. Short-term jitter is defined with respect to the falling edge of the CLK signal. 4-cycle short-term jitter is the difference between the cumulative cycle times of adjacent 4-cycles. Equal requirements apply for rising edges of the CLK signal. Equal requirements also apply for 2-cycle, 3-cycle, 5-cycle, and 6-cycle short-term jitter.

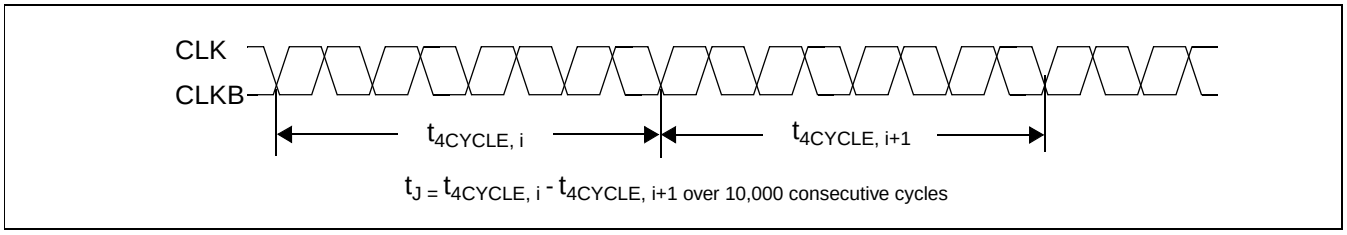

Figure 10: Short-term Jitter

The purpose of this definition of short-term jitter is to define errors in the measured time (for example, $t_{4CYCLE, i}$) vs. the expected time. The purpose for measuring the adjacent time $t_{4CYCLE, i+1}$ is only to help determine the expected time for $t_{4CYCLE, i}$. Alternate methods of determining t_J are possible. However, measuring long-term average jitter instead of short-term jitter would normally give more pessimistic results.

Figure 11 shows the definition of cycle-to-cycle duty cycle error ($t_{DC,ERR}$). Cycle-to-cycle duty cycle error is defined as the difference between t_{PW+} (high-times) of adjacent differential clock cycles. Equal requirements apply to t_{PW-}, low-times of the differential clock cycles.

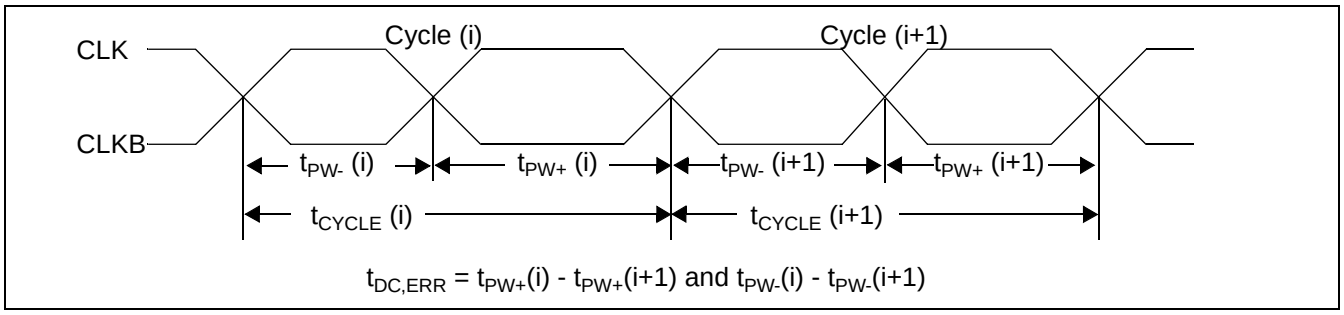

Figure 11: Cycle-to-cycle Duty Cycle Error

Figure 12 shows the definition of LCLK cycle jitter and LCLK 10-cycle jitter. These parameters apply to the LCLK output, and not to the Rambus channel clock outputs.

LCLK cycle jitter is the variation in the clock period, T, over a continuous set of clock cycles. The difference between the maximum period and the nominal period in the set of clock cycles measured would be compared to the max spec in Table 10. LCLK cycle jitter is measured between rising edges at 50% of the output voltage, and is measured continuously over 30,000 cycles.

Figure 11 shows the definition of cycle-to-cycle duty cycle error ($t_{DC,ERR}$). Cycle-to-cycle duty cycle error is defined as the difference between t_{PW+} (high-times) of adjacent differential clock cycles. Equal requirements apply to t_{PW-}, low-times of the differential clock cycles.

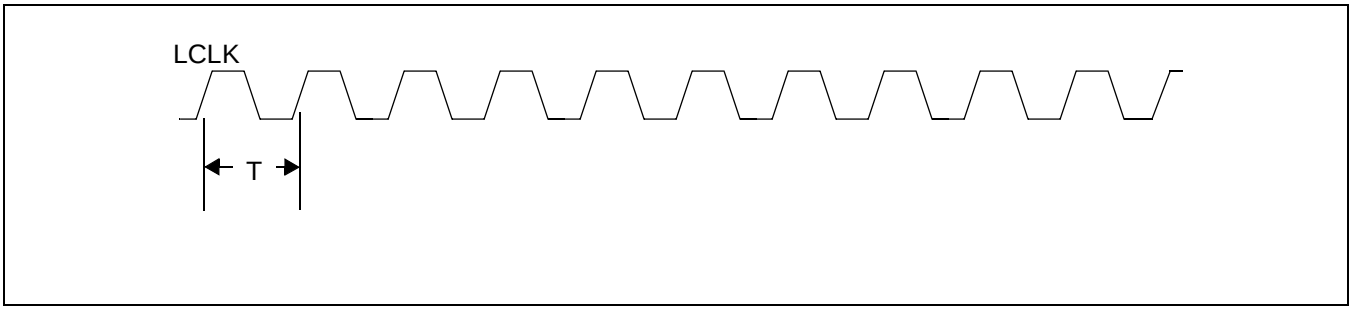

Figure 12: LCLK Jitter

Package Drawing

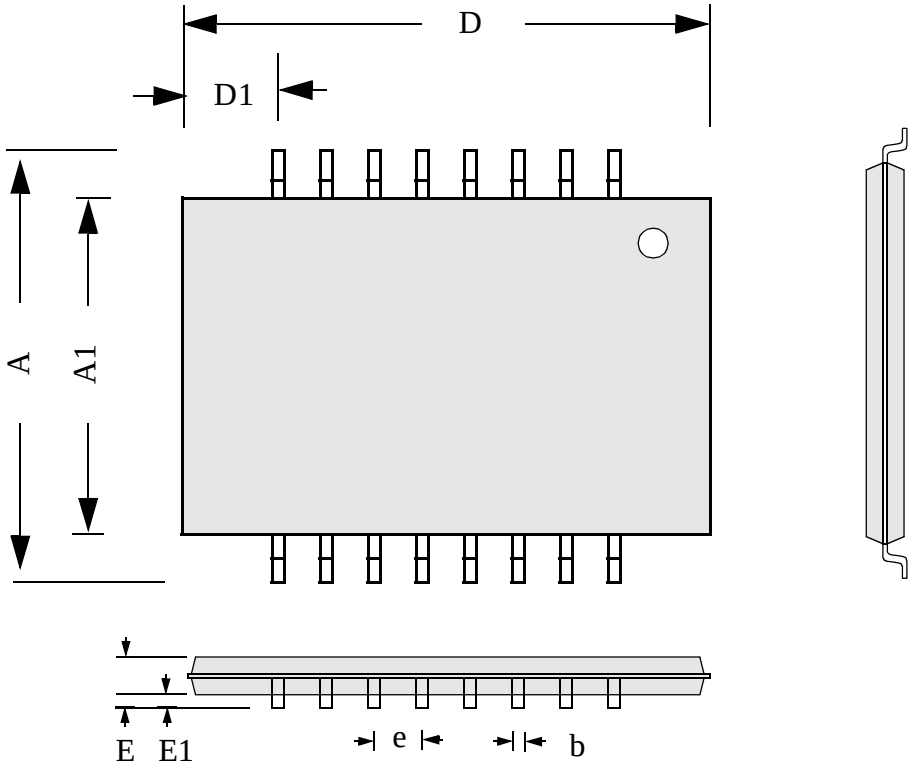

Figure 13: 16-Pin 225mil TSSOP Package Drawing

Table 13. Package Dimensions

Symbol	Parameter	Min	Max	Unit
e	Pin Pitch	0.65	0.65	mm
b	Pin width	0.19	0.30	mm
A	Package total length	6.20	6.60	mm
A1	Package body length	4.30	4.50	mm
D	Package total width	4.90	5.10	mm
D1	Package overhang	0.175	0.275	mm
E	Package total thickness	-	1.20	mm
E1	Space under package	0.05	0.15	mm

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