Direct Rambus® Clock Generator

Overview

The Direct Rambus® Clock Generator (DRCG) provides the necessary clock signals to support a Direct Rambus memory subsystem. It includes signals to synchronize the Direct Rambus Channel clock to an external system clock. Contained in a 24-pin SSOP package, the DRCG provides an off-the-shelf solution for a broad range of Direct Rambus memory applications, such as PC and workstation main memory, graphics frame buffers, and communications buffer memory.

Features

- High Speed Clock Support
  267-400 MHz clock source for Direct Rambus memory systems supports up to a 1.6 GB/sec data transfer rate
- Single differential output driver with less than 50ps short term jitter
- Synchronization Flexibility
  Includes signals to synchronize clock domains of the Rambus Channel with an external system or processor clock
- Supports frequency multipliers: 8, 6, 4, 8/3
- Power Management Support
  Two power management modes, Clk Stop and Powerdown minimizes power for mobile and other power-sensitive applications
  - In Clk Stop mode, the DRCG remains activated while the output buffer is disabled, allowing fast transitions between the clock-off and clock-on states. This mode can be used in conjunction with the Nap mode of the RDRAMs and Rambus ASIC Cell (RAC).
  - In Powerdown mode, the DRCG is completely powered down for minimum power dissipation. This mode is used in conjunction with the power down modes of the RDRAMs and RAC.
- Supports Independent Channel Clocking
  Supports systems not requiring synchronization of the Rambus clock to another system clock
- Active power < 350mW; Vdd = 3.3V ± 5%
- Supports Spread Spectrum Clocking (SSC) for EMI suppression and minimization

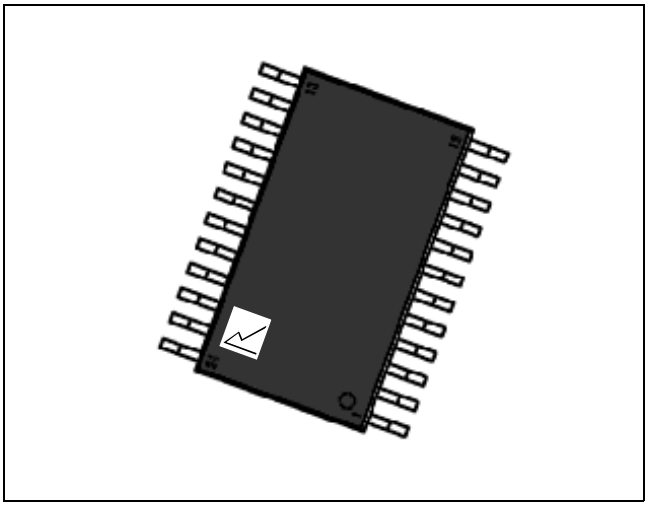

Figure 1: Direct Rambus Clock Generator Package

Related Documentation

Data sheets for the Rambus memory system components, including the Rambus DRAMs, RIMM Module, RIMM connector are available on the Rambus web site at http://www.rambus.com.

The DRCG is packaged in a 24-pin 150 mil SSOP. Figure 2 shows the pin assignments. Table 1 describes the function and connection of each pin.

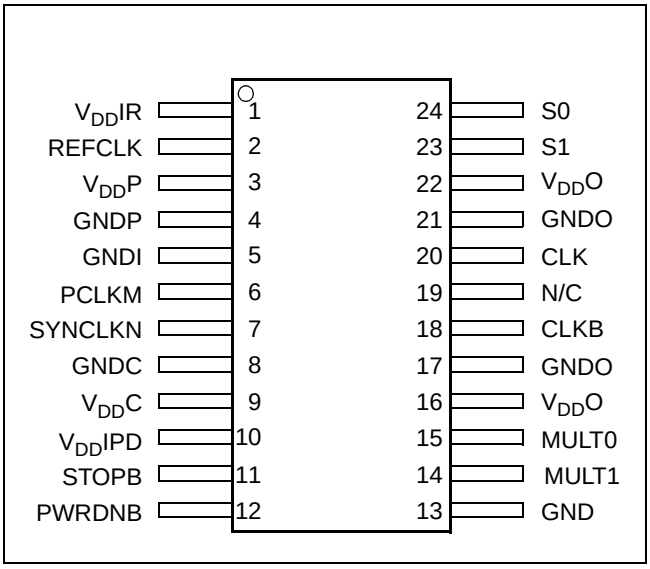

Figure 2: DRCG Pin-outs

Table 1. DRCG Pin-Out

Pin#	Signal	Type	Function	Notes
1	V_{DD}IR	RefV	Reference for REFCLK	Connect to Clock Source Supply
2	REFCLK	I	Reference clock	Connect to Clock Source
3	V_{DD}P	P	V_{DD} for PLL	3.3V Supply voltage
4	GNDP	G	Ground for PLL	Ground reference
5	GNDI	G	Ground for control inputs	Ground reference
6	PCLKM	I	Phase Detector input	Connect to Controller
7	SYNCLKN	I	Phase Detector input	Connect to Controller
8	GNDC	G	Ground for Phase Aligner	Ground reference
9	V_{DD}C	P	V_{DD} for Phase Aligner	3.3V Supply voltage
10	V_{DD}IPD	RefV	Reference for Phase Detector inputs & STOPB	Connect to Controller Supply
11	STOPB	I	Active Low clock output disable	Connect to Controller
12	PWRDNB	I	Active Low power down input	3.3V CMOS input signal
13	GND	I	Ground	Connect to Ground
14	MULT1	I	PLL multiplier select	3.3V CMOS input signal
15	MULT0	I	PLL multiplier select	3.3V CMOS input signal
16	V_{DD}O	P	V_{DD} for clock output	3.3V Supply voltage
17	GNDO	G	Ground for clock output	Ground reference
18	CLKB	O	Output Clock (complement)	Connect to Rambus Channel
19	N/C	N/C	Not used	Not connected (floating pin)
20	CLK	O	Output Clock	Connect to Rambus Channel
21	GNDO	G	Ground for clock output	Ground reference
22	V_{DD}O	P	V_{DD} for clock output	3.3V Supply voltage
23	S1	I	Mode Control	3.3V CMOS input signal
24	S0	I	Mode Control	3.3V CMOS input signal

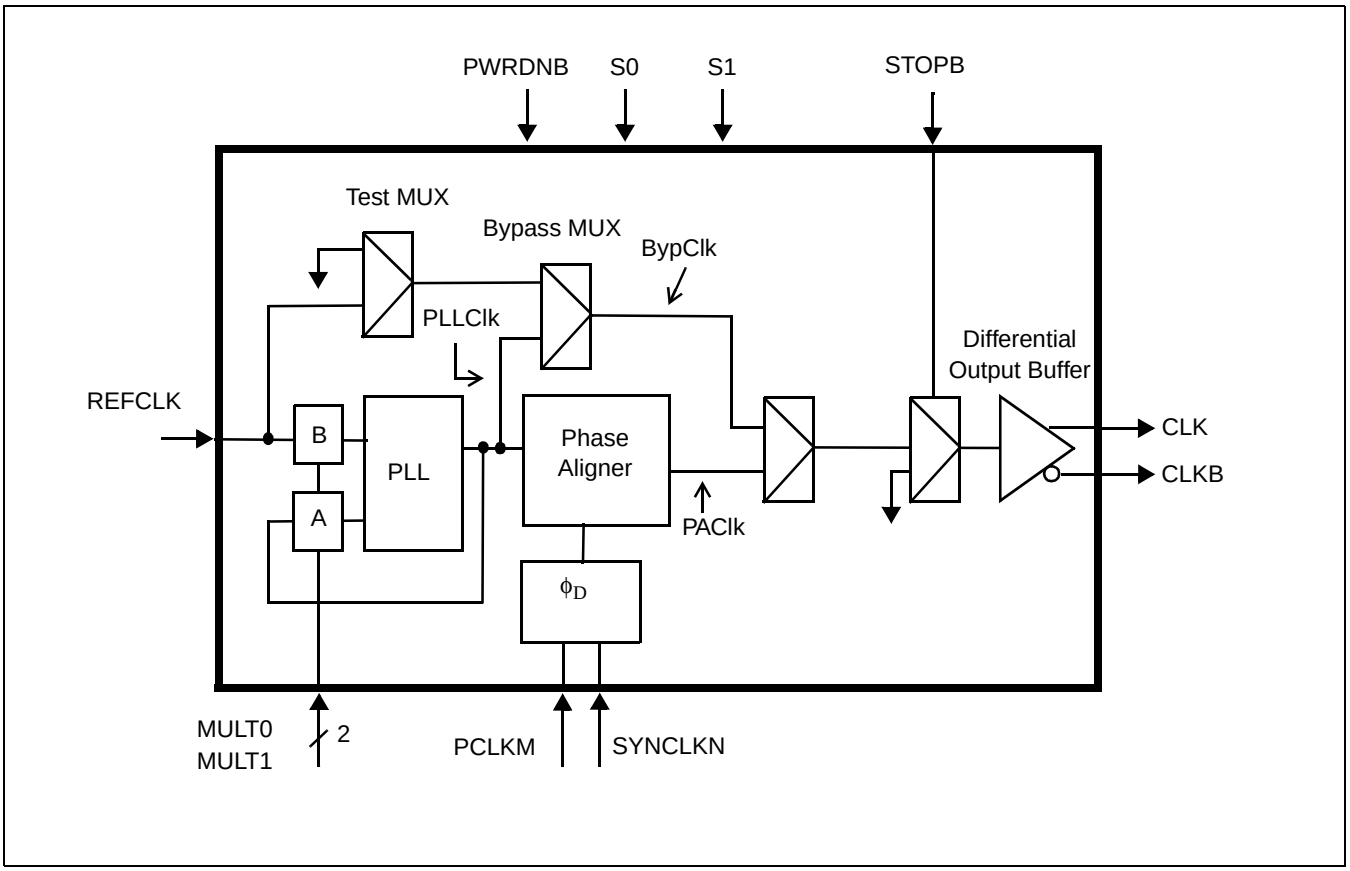

Figure 3: Direct Rambus Clock Generator Block Diagram

General Description

Figure 3 shows the block diagram of the DRCG. The major blocks of the DRCG include a Phase Lock Loop, a Phase Aligner, a Phase Detector, and a Differential Output Buffer.

The DRCG's input clock signal, REFCLK is fed to prescaler B of the PLL. Divider A is used in the PLL's feedback path, generating an intermediate output clock, PLLClk = REFCLK * A / B. The MULT0 and MULT1 pins control the multiply ratio for the PLL. The multiply ratio values for A and B are shown in Table 8 and described in the PLL Multiplier section.

The Phase Aligner is used to delay the PLL output by an arbitrary amount of phase, without modifying the output frequency. The Phase Aligner is controlled by the Phase Detector (ϕ_D). The Phase Aligner delays the output of the PLL by the amount of phase required to align PCLKM and SYNCLKN at the inputs of the Phase Detector. The Phase Aligner output clock is labeled PAClk, and is the clock that normally drives the DRCG output buffer.

Under Normal operation mode the Differential Output Buffer receives the input clock signal from the Phase Aligner, it buffers the signal and drives a differential clock output. The Differential Output Buffer is impedance matched to the Rambus Channel transmission line.

The S0 and S1 input pins control the Bypass and Test mode selection. The Bypass mode selects the output of the PLL (PLLClk), bypassing the Phase Aligner, and can be used in applications that do not require Gear Ratio Logic in the controller (or phase alignment of external clocks). The Test mode routes the input clock, REFCLK, bypassing both the PLL and the Phase Aligner circuits to the differential output buffer.

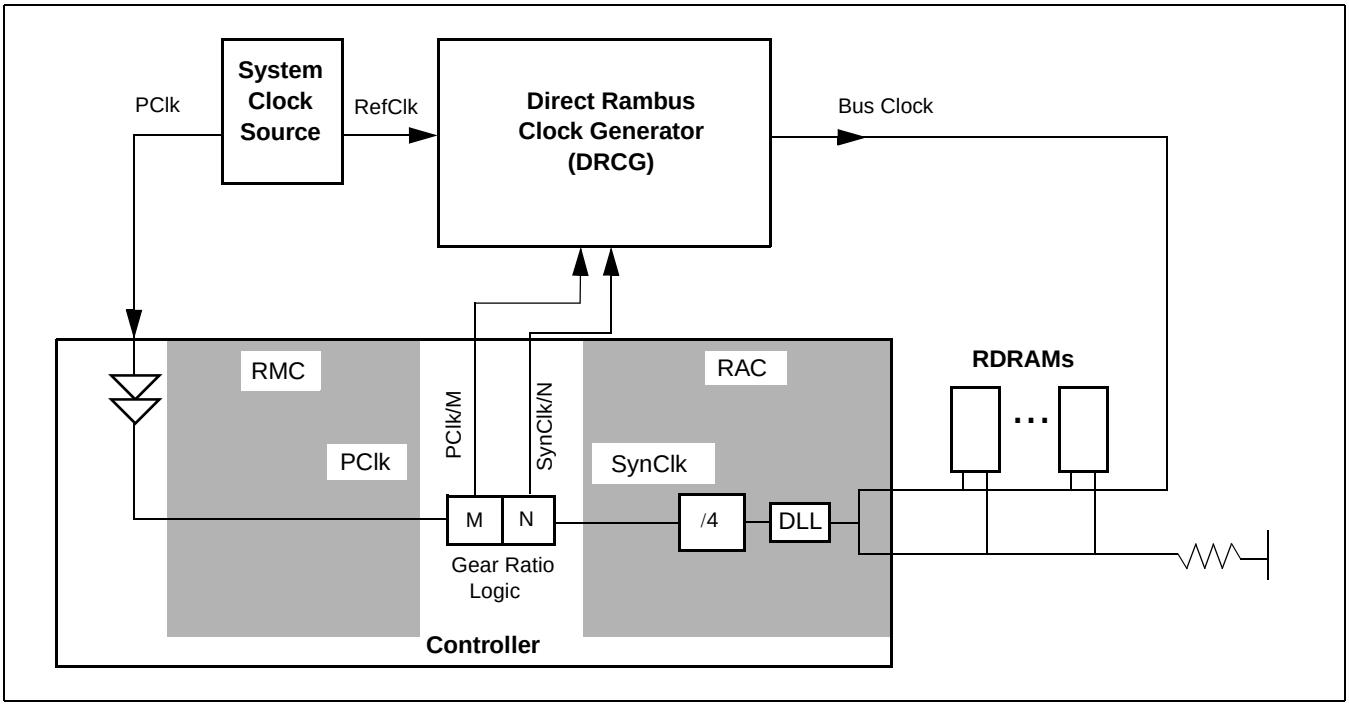

Figure 4: System Clock Architecture

Example System Clock Configuration

Figure 4 shows the clocking configuration for an example Direct Rambus DRAM subsystem. The configuration shows the interconnection of the system clock source, the Direct Rambus Clock Generator (DRCG), and the clock signals of a memory controller ASIC. The ASIC contains the Rambus Access Cell (RAC), the Rambus Memory Controller (RMC), and logic to support synchronizing the Channel Bus Clock with the controller clock. (The diagram represents the differential clock outputs as a single Bus Clock wire.) This configuration achieves frequency-lock between the controller and Rambus Channel clocks (PClk and SynClk). These clock signals are matched and phase-aligned at the RMC / RAC boundary in order to allow data transfers to occur across this boundary without additional latency.

The main clock source drives the system clock (PClk) to the ASIC, and also drives the reference clock (RefClk) to the DRCG. PClk and RefClk must have a rational frequency relationship, even if the frequencies are not equal; but, there is no phase relationship requirement whatsoever. A PLL inside the DRCG multiplies the DRCG's REFCLK input to generate the desired frequency for Bus Clock. Bus Clock is driven on the Rambus Channel through a terminated transmission line. At the mid-point of the Channel, the RAC senses Bus Clock using its own DLL for clock alignment, followed by a fixed divide-by-4 circuit that generates SynClk.

PClk is the clock used by the RMC in the ASIC. SynClk is the clock used at the ASIC interface of the RAC. The DRCG together with the Gear Ratio Logic in the ASIC enables the controller to exchange data directly from the PClk domain to the SynClk domain without incurring additional latency for synchronization. In general, PClk and SynClk can run at different frequencies, so the Gear Ratio Logic must select the appropriate M and N dividers such that the frequencies of PClk / M and SynClk / N are equal. For example, if PClk=133MHz and Bus Clock=400MHz, SynClk=100MHz, and M=4 while N=3, giving PClk / M = SynClk / N = 33MHz.

Figure 5 shows an example of the clock waveforms generated with the Gear Ratio Logic.

The ASIC drives the output clocks, PClk / M and SynClk / N from the Gear Ratio Logic to the DRCG Phase Detector inputs. The routing of the PClk / M and SynClk / N signal traces must be matched both in impedance and propagation delay on the ASIC as well as on the board. These signals are not part of the Rambus Channel and their routing must be matched by board designers.

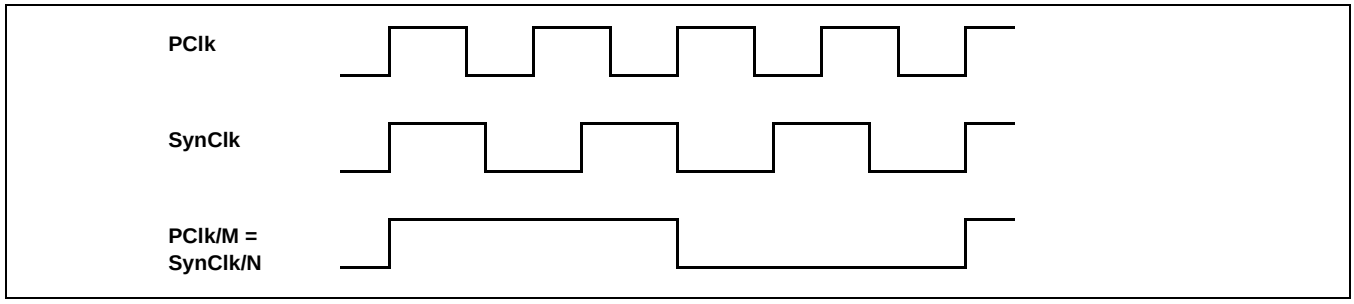

Figure 5: Gear Ratio Timing Diagram

After comparing the phases of PClk / M and SynClk / N, the DRCG Phase Detector drives a phase aligner that adjusts the phase of the DRCG output clock, Bus Clock. Since the other elements in the distributed loop have a fixed delay, adjusting Bus Clock adjusts the phase of SynClk and thus the phase of SynClk / N. In this manner, the distributed loop adjusts the average phase of SynClk / N to match the average phase of PClk / M, eliminating the average phase error at the input of the DRCG Phase Dectector. When the clocks are aligned, data can be exchanged directly from the PClk domain to the SynClk domain.

If the ASIC stops the SynClk / N clock (for example, in a power saving mode), the DRCG phase aligner freezes and holds it state. The phase aligner resumes normal operation when SynClk / N resumes.

The Gear Ratio Logic supports four clock ratios (2.0, 1.5, 1.33, and 1.0), where the ratio is defined as the ratio of PClk / SynClk. Since Bus Clock = 4*SynClk, this ratio also is equal to 4*PClk / Bus Clock. Other ratios could be used, depending on particular system implementations. Table 2 shows several supported gear ratios, together with the corresponding M and N dividers in the gear ratio logic, and the corresponding A and B dividers required and designed into the DRCG PLL. The Ratio column gives the Gear Ratio as defined by PClk / SynClk (same as M / N). The ***f***@PD column lists the divided down frequency (in MHz) at the Phase Detector input, where f@PD = PClk / M = SynClk / N.

Table 2. Frequencies, Dividers, and Gear Ratios

Bus Clock	P Clk	Syn Clk	A	B	M	N	Ratio	*f*@ PD
267	67	67	8	1	2	2	1.0	33
300	100	75	6	1	8	6	1.33	12.5
400	100	100	8	1	4	4	1.0	25
267	133	67	4	1	4	2	2.0	33
400	133	100	6	1	8	6	1.33	16.7

System Architecture without Gear Ratio Logic

Figure 6 shows how a DRCG can be used in a system that does not use Gear Ratio Logic. The DRCG is used to generate Bus Clock, as before, but the Phase Aligner part of the DRCG is not used. In this configuration, the Phase Aligner inputs (PCLKM and SYNCLKN) must be tied to ground and not left floating. Since the resulting SynClk and PClk signals are not aligned, the data must be retimed (for example, using FIFOs) at the PClk / SynClk boundary.

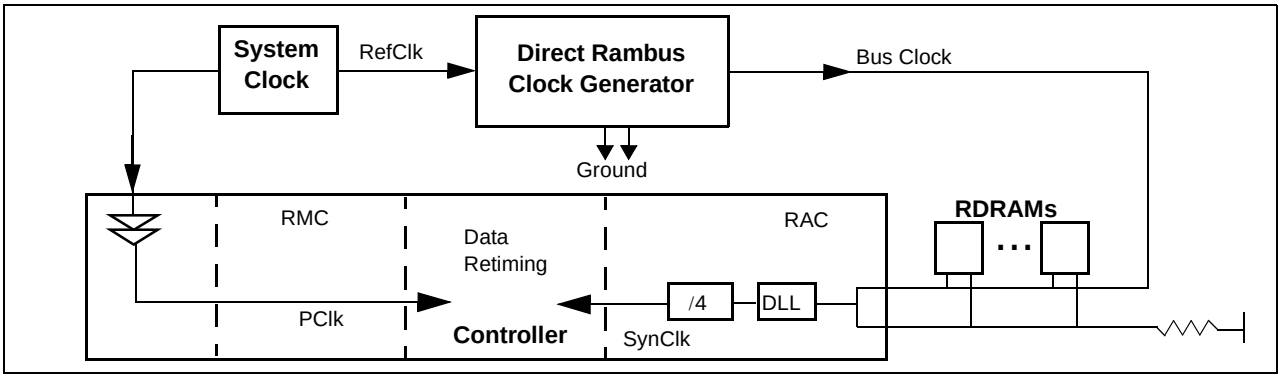

Figure 6: DRCG In System without Gear Ratio Logic

Logical Specification

The DRCG clock source has three fundamental operating states. Figure 7 shows the state diagram with each transition labeled A through N. Note that the clock source output need NOT be glitch-free during state transitions.

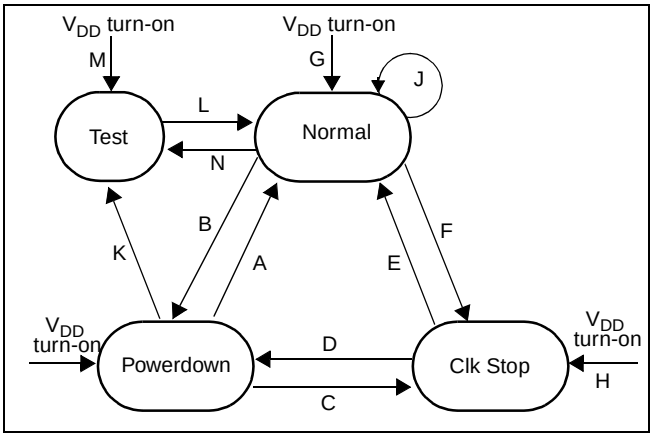

Figure 7: DRCG State Diagram

Upon powering up the DRCG, the device can enter any state, depending on the settings of the control signals PWRDNB and STOPB.

In Powerdown mode (PWRDNB = 0), the DRCG clock source is powered down with the control signal, PWRDNB. The reference inputs, V_{DD}IR and V_{DD}IPD, may remain ON or may be grounded while in Powerdown mode. The PWRDNB signal dominates all other DRCG control signals. If PWRDNB is enabled (PWRDNB = 0), the device should enter the Powerdown mode no matter what other signals are driving or controlling the DRCG. The device should not exit the Powerdown mode until PWRDNB is disabled (PWRDNB = 1). Transition timing is shown in Table 5.

The control signals S0 and S1 may be changed to take the DRCG from Test mode to Normal mode or Normal mode to Test mode, as shown in Figure 10.

The MULT0 and MULT1 control signals can be used in two ways. If they are changed during Powerdown mode, then the Powerdown transition timings determine the settling time of the DRCG.

However, the MULT0 and MULT1 control signals can also be changed during Normal mode. When the MULT control signals are “hot swapped” in this manner, the MULT transition timings determine the settling time of the DRCG. The MULT0 and MULT1 control signals must be stable during Test mode.

In Clk Stop mode (STOPB = 0, PWRDNB = 1), the clock source is ON, but the clock output is disabled. The reference inputs V_{DD}IR and V_{DD}IPD must remain ON during the Clk Stop mode.

In Normal mode (STOPB = 1, PWRDNB = 1), the clock source is ON, and the Differential Output Buffer is enabled.

The SYNCLKN input, controls the update of the phase aligner logic. If the SYNCLKN input stops toggling, whether in Normal mode or Clk Stop mode, the phase aligner will stop advancing and will hold its state. The maximum time that SYNCLKN can be frozen is the same as the maximum assertion time for STOPB, shown as a parameter tSTOP in Table 4. When the SYNCLKN input resumes toggling, the phase aligner logic should continue being updated according to the phase difference at the phase detector inputs, PCLKM and SYNCLKN.

Table 3. Control Signals for Clock Source States

STATE	PWRDNB	STOPB	Clock Source	Output Buffer
Powerdown	0	X	OFF	Ground
Clk Stop	1	0	ON	Disabled
Normal	1	1	ON	Enabled

Transition Timings

The following figures show the timing diagrams for the various transitions between states.

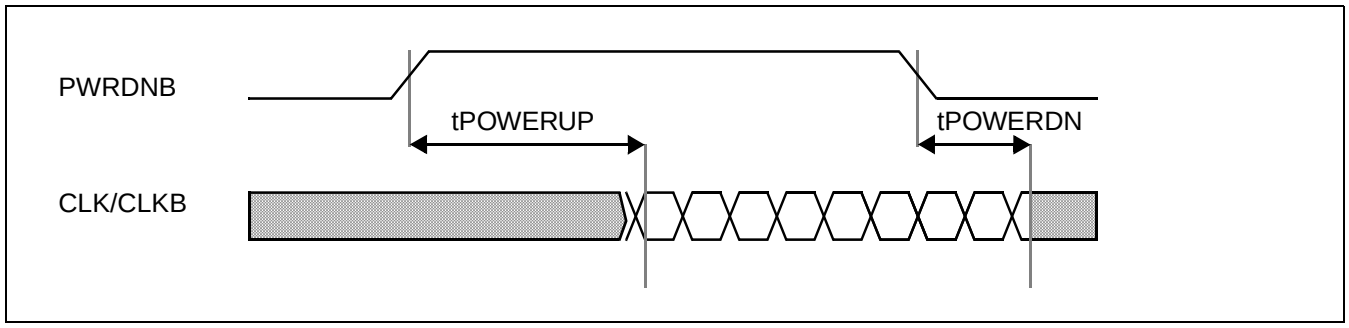

Figure 8: PWRDNB Transition Timings

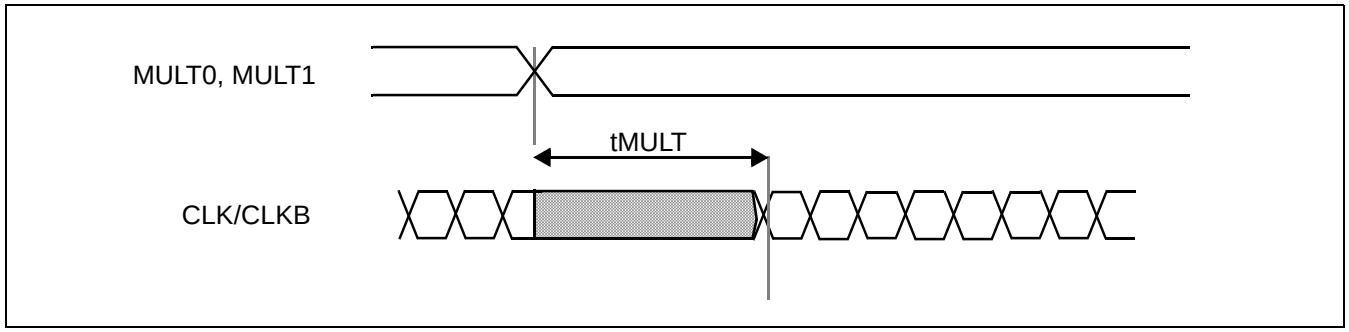

Figure 9: MULT Transition Timings

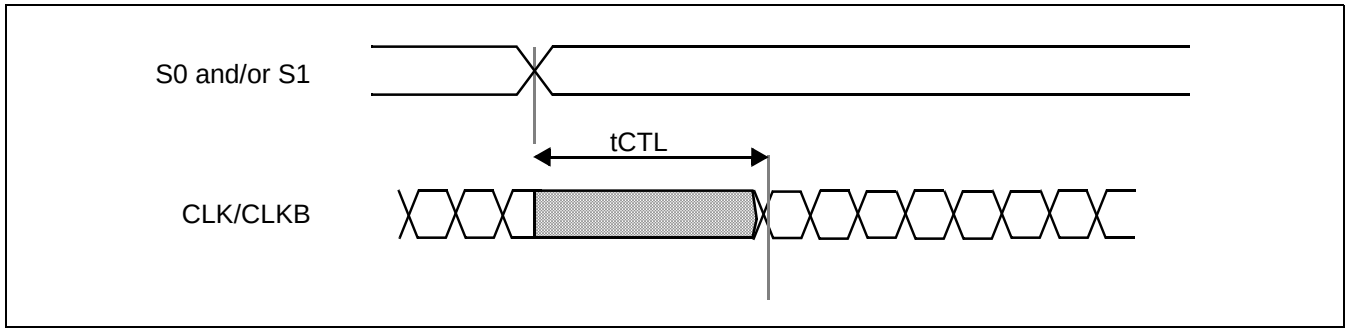

Figure 10: S0 and S1 Transition Timings

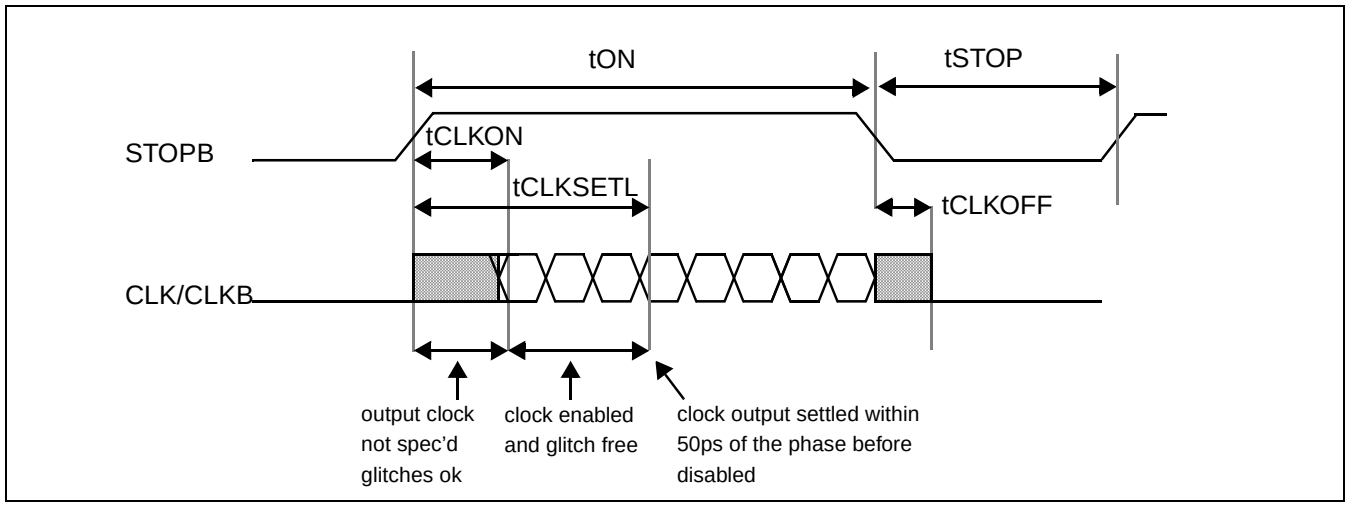

Figure 11: StopB Transition Timings

Figure 11 shows that the Clk Stop to Normal transition goes through three phases. During tCLKON, the clock output is not specified and can have glitches. For the time period tCLKON < t < tCLKSETL, the clock output is enabled and is glitch-free. For the time period t > tCLKSETL, the clock output phase settles to within 50 ps of the phase before the clock output was disabled. At this time, the clock output must also meet the voltage and timing specifications listed in the Device Parameters. The outputs are in a high impedance state during the Clk Stop mode. The above specifications apply when the output has been held in the Clk Stop state for less than tSTOP listed in Table 4.

Table 4. STOPB Control Timing

Symbol	Min	Max	Unit	Description
tSTOP		100	µs	Max time in Clk Stop (STOPB=0) before re-entering Normal mode (STOPB=1).
tON	100		ns	Min time in Normal mode (STOPB=1) before re-entering Clk Stop (STOPB=0).

Table 5 specifies the latencies of each state transition. Note that these transitions need not be glitch free. Also the transition latencies assume the following:

- RefClk input has settled and meets DC and AC operating conditions shown in Table 14 and Table 16.
- S0 and S1 control signals are stable, except for the timing tCTL.
- MULT0 and MULT1 are stable, except for the timing for tMULT.

Table 5. State Transition Latency Specifications

Transition	From	To	Transition Latency		Description
			Symbol	Max	
A	Power-down	Normal	tPOWERUP	3 ms	Time from PWRDNB ↑ to CLK/CLKB output settled (excluding tDISTLOCK).
C	Power-down	Clk Stop	tPOWERUP	3 ms	Time from PWRDNB ↑ until the internal PLL and clock has turned ON and settled.
K	Power-down	Test	tPOWERUP	3 ms	Time from PWRDNB ↑ to CLK/CLKB output settled (excluding tDISTLOCK).
G	V_{DD} ON	Normal	tPOWERUP	3 ms	Time from when V_{DD} is applied and settled until CLK/CLKB output is settled (excluding tDISTLOCK).
H	V_{DD} ON	Clk Stop	tPOWERUP	3 ms	Time from when V_{DD} is applied and settled until the internal PLL and clock has turned ON and settled.
M	V_{DD} ON	Test	tPOWERUP	3 ms	Time from when V_{DD} is applied and settled until the output clock has turned ON and settled.
J	Normal	Normal	tMULT	1 ms	Time from when MULT0 or MULT1is changed until CLK/CLKB output has re-settled (excluding tDISTLOCK).
E	Clk Stop	Normal	tCLKON	10 ns	Time from STOPB ↑ until CLK/CLKB provides glitch-free clock edges.
E	Clk Stop	Normal	tCLKSETL	20 cycles	Time from STOPB ↑ to CLK/CLKB output settled to within 50ps of the phase before CLK/CLKB was disabled.
F	Normal	Clk Stop	tCLKOFF	5 ns	Time from STOPB ↓ to CLK/CLKB output disabled.
L	Test	Normal	tCTL	3 ms	Time from when S0 or S1 is changed until CLK/CLKB output has re-settled (excluding tDISTLOCK).
N	Normal	Test	tCTL	3 ms	Time from when S0 or S1 is changed until CLK/CLKB output has re-settled (excluding tDISTLOCK).
B,D	Normal or Clk Stop	Power-down	tPOWERDN	1 ms	Time from PWRDNB ↓ to the device in Powerdown Mode.

Power Saving Modes

Table 6 shows the logic for enabling the clock outputs, using the STOPB input signal. When STOPB is high, the DRCG is in its Normal mode, and CLK and CLKB are complementary outputs following the Phase Aligner output (PAClk in Figure 3). When STOPB is low, the DRCG is in Clk Stop mode, the output driver transistors are both disabled and the CLK and CLKB outputs are set by internal resistor dividers to voltage $V_{X,STOP}$.

Table 6. Clk Stop Mode Selection

Mode	STOPB	PWRDNB	CLK	CLKB
Normal	1	1	PAClk	PAClkB
Clk Stop	0	1	$V_{X,STOP}$	$V_{X,STOP}$

Table 7 shows the logic for selecting the Powerdown mode, using the PWRDNB input signal. PWRDNB is active low (enabled when = 0). When PWRDNB is disabled, the DRCG is in its Normal mode. When PWRDNB is enabled (PWRDNB = 0), the DRCG is put into a powered-off state, and the CLK and CLKB outputs are both low (ground). The internal resistor dividers are disconnected during Powerdown mode in order to save power. This is true both for the resistor dividers used to set $V_{X,STOP}$ during Clk Stop mode, and for the resistor dividers used to set the trip points for the input clocks.

Table 7. Powerdown Mode Selection

Mode	PWRDNB	STOPB	CLK	CLKB
Normal	1	1	PAClk	PAClkB
Power-down	0	X	Gnd	Gnd

PLL Multiplier

Table 8 shows the logic for selecting the PLL prescaler and feedback dividers to determine the multiply ratio for the PLL from the REFCLK input. Divider A sets the feedback and Divider B sets the prescaler, so the PLL output clock (PLLClk in Figure 3) is set by: PLLClk = REFCLK * A / B.

Table 8. PLL Divider Selection

MULT0	MULT1	A	B
0	0	4	1
0	1	6	1
1	1	8	1
1	0	8	3

Distributed Loop Lock Time

After the DRCG PLL has settled, the distributed loop containing the Phase Aligner must also settle. This settling time depends on components in the distributed loop which are outside of the clock source. Therefore, this system settling time is not a component specification.

The maximum lock time for the distributed loop is specified in Table 9. Note that the total time for the output clock to settle from the Powerdown state to the Normal state is the sum of tPOWERUP plus tDISTLOCK. Similarly, if MULT0 and MULT1 control signals are changed while the DRCG is in the Normal state, the total time for the output clock to re-settle is the sum of tMULT plus tDISTLOCK.

Table 9. Distributed Loop Lock Time Specification

Symbol	Min	Max	Unit	Description
tDISTLOCK		2.5	ms	Time from when CLK / CLKB output is settled to when the phase error between SYNCLKN and PCLKM falls within the t_{ERR-PD} spec in Table 17.

The above specification is the maximum possible lock time for the distributed loop. The actual lock time depends on the cycle time of the phase detector input clocks ($t_{CYCLE,PD}$), the amount of initial phase error at the phase detector inputs ($t_{ERR,INIT}$), and the phase detector step size per update (t_{STEP}) shown in Table 17. The lock time is given by:

$$tDISTLOCK = t_{CYCLE,PD} * t_{ERR,INIT} / t_{STEP}.$$

Using the values given in Table 16 and Table 17, this reduces to:

$$tDISTLOCK = 0.5 * (t_{CYCLE,PD})^2 / 2ps.$$

The resulting lock time, therefore, strongly depends on the phase detector input cycle time. For the maximum cycle time of 100ns (10MHz), this gives 2.5ms as shown in Table 9. For a cycle time of 80ns (12.5MHz), the lock time drops to 1.6ms. And for a faster cycle time of 40ns (25MHz), the lock time drops to 0.4ms.

Test Modes

Table 10 shows the logic for selecting the Bypass and Test modes. The select bits, S0 and S1, control the selection of these modes. The Bypass mode selects and outputs the full speed PLL output clock (PLLClk) to the CLK / CLKB outputs bypassing the Phase Aligner. The Test mode selects the REFCLK input and outputs it to the CLK / CLKB outputs bypassing both the PLL and the Phase Aligner.

In the Output Test mode (OE), both the CLK and CLKB outputs are put into a high-impedance state (Hi-Z). This mode can be used for component testing and for board-level testing. The internal resistor dividers used

to set $V_{X,STOP}$ during Clk Stop mode are disconnected during Output Test mode.

Table 10: Bypass and Test Mode Selection

Mode	S0	S1	CLK	CLKB
Normal	0	0	PAClk	PAClkB
Bypass	1	0	PLLClk	PLLClkB
Test	1	1	RefClk	RefClkB
Output Test (OE)	0	1	Hi-Z	Hi-Z

Device Parameters

This chapter specifies the numerical values of the physical parameters described earlier in this data sheet.

The DRCG clock source meets the device characteristics listed in Table 15 and Table 17 when characterized under the operating conditions listed in Table 14 and Table 16, and when using the components shown in Figure 13, and the corresponding component values given in Table 18.

Only the DC specifications of Table 15 apply while in Test mode. The AC specifications of Table 17 (see Logical Specification Section for mode descriptions) do not apply while in Test mode unless specified.

Absolute Maximums

Table 11 represents stress ratings only, and functional operation at the maximum settings is not guaranteed.

Table 11. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{DD,ABS}$	Max voltage on V_{DD} with respect to ground	-0.5	4.0	V
$V_{I,ABS}$	Max voltage on any pin with respect to ground	-0.5	V_{DD}+ 0.5	V

Supply Current Characteristics

The current drawn through the V_{DD} pins is specified in Table 12. This includes the total current through all V_{DD}C, V_{DD}P, and V_{DD}O pins.

Table 12. Supply Current Characteristics

Symbol	Parameter	Min	Max	Unit
$I_{POWER-DOWN}$	Current in Power-down state (PWRDNB = 0)		200	µA
$I_{CLKSTOP}$	Current in Clk Stop state (STOPB = 0)		50	mA
I_{NORMAL}	Current in Normal state (STOPB = 1)		100	mA

The current drawn through the V_{DD}IR and the V_{DD}IPD reference pins is specified in Table 13. These specs are for each pin individually, and not for their sum. The maximum total current for the reference pins would be two times the numbers below. The maximum total current would be 2mA for the REFCLK reference input (V_{DD}IR) plus 2mA more for the complete voltage reference circuit (on pin V_{DD}IPD) used for both Phase Detector input pins.

Table 13. Reference Current Characteristics

Symbol	Parameter	Min	Max	Unit
IREF,PWDN	Reference Current in Powerdown state (PWRDNB = 0)		50	µA
IREF,NORM	Reference Current in Normal or Clk Stop state (PWRDNB=1)		2	mA

DC Operating Conditions

This section specifies input conditions for operating the device. When operated outside these limits, device characteristics are undefined.

Table 14 gives the DC operating characteristics.

Table 14. DC Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage	3.135	3.465	V
T_A	Ambient operating temperature	0	70	°C
V_{IL}	Input (scalable CMOS) signal low voltage	-	0.3	V_{DD}
V_{IH}	Input (scalable CMOS) signal high voltage	0.7	-	V_{DD}
$V_{IL,R}$	REFCLK input low voltage	-	0.3	V_{DD}IR
$V_{IH,R}$	REFCLK input high voltage	0.7	-	V_{DD}IR
$V_{IL,PD}$	Input signal low voltage for PD inputs and STOPB	-	0.3	V_{DD}IPD
$V_{IH,PD}$	Input signal high voltage for PD inputs and STOPB	0.7	-	V_{DD}IPD
V_{DDIR}	Input supply reference for REFCLK	1.235	3.465	V
V_{DDIPD}	Input supply reference for PD inputs	1.235	2.625	V
I_{IN}	Input leakage current spec for REFCLK input, Phase Detector inputs, and all scalable CMOS inputs[a]	-50	50	uA

a. For $V_{DDx} \geq$ input ≥ 0 , where V_{DDx} is the relevant supply (V_{DDIR} for REFCLK, V_{DDIPD} for the Phase Detector inputs, and other CMOS inputs)

DC Characteristics

Table 15. DC Device Characteristics

Symbol	Parameter	Min	Max	Unit
$V_{X,STOP}$	Output voltage during Clk Stop (STOPB=0)	1.1	2.0	V
V_X	Differential output crossing-point voltage	1.3	1.8	V
V_{COS}	Output voltage swing (p-p single-ended)[a]	0.4	1.0	V
V_{OH}	Output high voltage	-	2.35	V
V_{OL}	Output low voltage	1.0	-	V
r_{OUT}	Output dynamic resistance (at pins)[b]	12	50	Ω
I_{OZ}	Output current during Hi-Z (S0=0, S1=1)	-	50	µA
$I_{OZ,STOP}$	Output current during Clk Stop (STOPB=0)	-	500	µA

a. $V_{COS} = V_{OH} - V_{OL.}$
b. $r_{OUT} = DV_O / DI_O$. This is defined at the output pins.

AC Operating Conditions

This section specifies input AC conditions for operating the device. When operated outside these limits, device characteristics are undefined.

Table 16. AC Operating Conditions

Symbol	Parameter	Min	Max	Unit
$t_{CYCLE,IN}$	REFCLK Input cycle time	10	40[a]	ns
$t_{J,IN}$	Input Cycle-to-cycle jitter[b]	-	250	ps
DC_{IN}	Input duty cycle over 10,000 cycles	40%	60%	t_{CYCLE}
$f_{M,IN}$[c]	Input frequency of modulation	30	33	kHz
$P_{M,IN}$[c]	Modulation index for triangular modulation	-	0.6	%
	Modulation index for non-triangular modulation	-	0.5[d]	%
$t_{CYCLE,PD}$	Phase Detector input cycle time at PCLKM & SYNCLKN	30	100	ns
t_{JPD}	Phase Detector input Cycle-to-cycle jitter[e]		3.5	ns
$t_{ERR,INIT}$	Initial Phase error at Phase Detector inputs (Required range of Phase Aligner)	-0.5	0.5	$t_{CYCLE,PD}$
$DC_{IN,PD}$	Phase Detector input duty cycle over 10,000 cycles	25%	75%	$t_{CYCLE,PD}$
$t_{I,SR}$	Input slew rate (measured at 20% - 80% of input voltage) for PCLKM, SYNCLKN, and REFCLK	1	4	V / ns
$C_{IN,PD}$	Input capacitance at PCLKM, SYNCLKN, and REFCLK[f]	-	7	pF
$\Delta C_{IN,PD}$	Input capacitance matching at PCLKM and SYNCLKN[f]	-	0.5	pF
$C_{IN,CMOS}$	Input capacitance at scalable CMOS pins (excluding PCLKM, SYNCLKN, and REFCLK)[f]	-	10	pF

a. Maximum REFCLK Input cycle time specification does not apply when the DRCG is in Test Mode.
b. RefClk jitter measured at $V_{DDI,R}$(nom) / 2 and is the absolute value of the worst case + / - deviation, not the peak-to-peak jitter.
c. If input modulation is used; input modulation is allowed but not required
d. The amount of allowed spreading for any non-triangular modulation is determined by the induced downstream tracking skew, which cannot exceed the skew generated by the specified 0.6% triangular modulation. Typically, the amount of allowed non-triangular modulation is about 0.5%
e. The input jitter for the Phase Detector inputs is defined from cycle-to-cycle on one input signal (not between the two Phase Detector inputs), and is measured at $V_{DDI,PD}$(nom) / 2. Because the allowable input jitter is large, a non-proportional (bang-bang) phase detector design is used to limit the effect on output clock jitter.
f. Capacitance measured at Frequency = 1MHz, DC bias = 0.9V, and VAC < 100mV

AC Characteristics

Table 17 gives the AC characteristics for device operation.

Table 17. AC Device Characteristics

Symbol	Parameter	Min	Max	Unit
t_{CYCLE}	Clock cycle time	2.5	3.83	ns
t_J	Jitter over 1-6 clock cycles at 400MHz[a]	-	50	ps
	Jitter over 1-6 clock cycles at 300MHz[a]	-	70	ps
	Jitter over 1-6 clock cycles at 267MHz[a]	-	80	ps
t_{STEP}	Phase Aligner phase step size (at CLK / CLKB)	2	-	ps
$t_{ERR,PD}$	Internal Phase Detector phase error between PCLKM and SYNCLKN (rising edges)[b]	- 100	100	ps
$t_{ERR,SSC}$	PLL output Phase error when tracking SSC	- 100	100	ps
DC	Output duty cycle over 10,000 cycles	40%	60%	t_{CYCLE}
$t_{DC,ERR}$	Cycle-to-cycle duty cycle error at 400MHz	-	50	ps
	Cycle-to-cycle duty cycle error at 300MHz	-	70	ps
	Cycle-to-cycle duty cycle error at 267MHz	-	80	ps
t_{CR}, t_{CF}	Output rise and fall times (measured at 20% - 80% of output voltage)	160	400	ps
$t_{CR,CF}$	Difference between output rise and fall times on the same pin of a single device (20% - 80%)	-	100	ps
t_{JT}	Cycle-to-cycle jitter during Test mode[c]	-	500	ps
DC_T	Average Output duty cycle over 10,000 cycles during Test mode[c]	40%	60%	t_{CYCLE}
t_{CRT}, t_{CFT}	Output rise and fall times (measured at 20% - 80% of output voltage) during Test mode[c]	250	900	ps

a. Output short term jitter specification is the absolute value of the worst case measured ± deviation over 10,000 consecutive cycles and is defined in the Jitter section and illustrated in Figure 18.
b. Phase Detector phase error is a component specification that tests the internal DRCG phase detector alignment circuitry and not an external distributed loop in a system. This specification applies to the average phase error and does not include jitter of the input clocks.
c. Specification applies during Test Mode only.

Physical Specification

Input Signals

The DRCG receives a reference clock input (RefClk) and two clock inputs (PCLKM and SYNCLKN) that drive the phase detector. These clock inputs come from circuits that are powered by different supplies than the DRCG, and thus cannot be referenced to the DRCG's 3.3V supply voltage. Reference voltage inputs $V_{DD}IR$ and $V_{DD}IPD$ are provided to enable the DRCG to determine the proper trip-point of the clock inputs.

The Phase Detector signals come from the controller, so the controller output voltage supply is connected to the pin $V_{DD}IPD$ of the DRCG, and is used as the reference for the two phase detector input signals, PCLKM and SYNCLKN. $V_{DD}IPD$ is also used as the reference for the output enable / disable signal, STOPB.

Similarly, the reference clock comes from the main clock source chip, so the main clock source output voltage supply is connected to the pin $V_{DD}IR$ of the DRCG, and is used as the reference for the REFCLK input signal.

The input clock signals must be converted from small swing signals (e.g. 0 to $V_{DD}IR$ or 0 to $V_{DD}IPD$) to full swing signals (0 to V_{DD}). Therefore, the DRCG contains input translator circuits in order to detect the inputs levels accurately. Figure 12 shows an example connection of a clock source (with its $V_{DD}I$) to the DRCG. The figure also shows a resistor divider that conceptually shows how a $V_{DD}I/2$ reference could be developed.

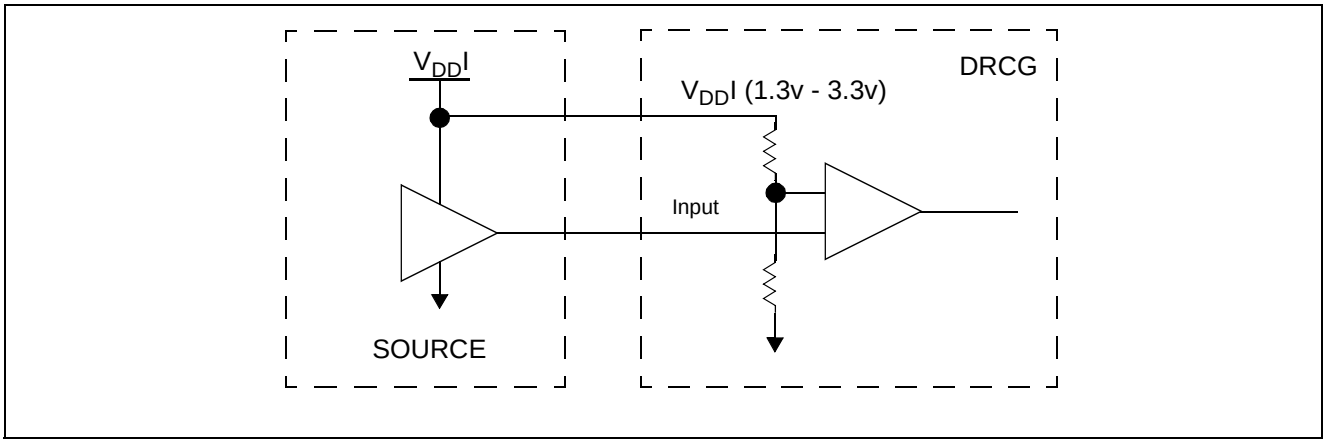

Figure 12: Input Level Translator

Select Inputs

There are several select inputs. The MULT0 and MULT1 inputs are used for selecting the PLL multiplier ratio. The S0 and S1 inputs are used for selecting various modes of operation. And the PWRDNB input is used for controlling powerdown.

All of the select inputs (MULT0, MULT1, S0, S1, and PWRDNB) are normal, 3.3V LCMOS, scalable CMOS inputs signals. No external reference inputs or level translators (such as those used with the clock inputs) are required.

All inputs are active high, except PWRDNB, which is active low. No internal pull-up or pull-down resistors exist inside the DRCG.

The only parameters listed in Table 16 that relate specifically to the select inputs are the input levels (V_{IL} and V_{IH}) and the input capacitance ($C_{IN,CMOS}$).

Clock Output Driver

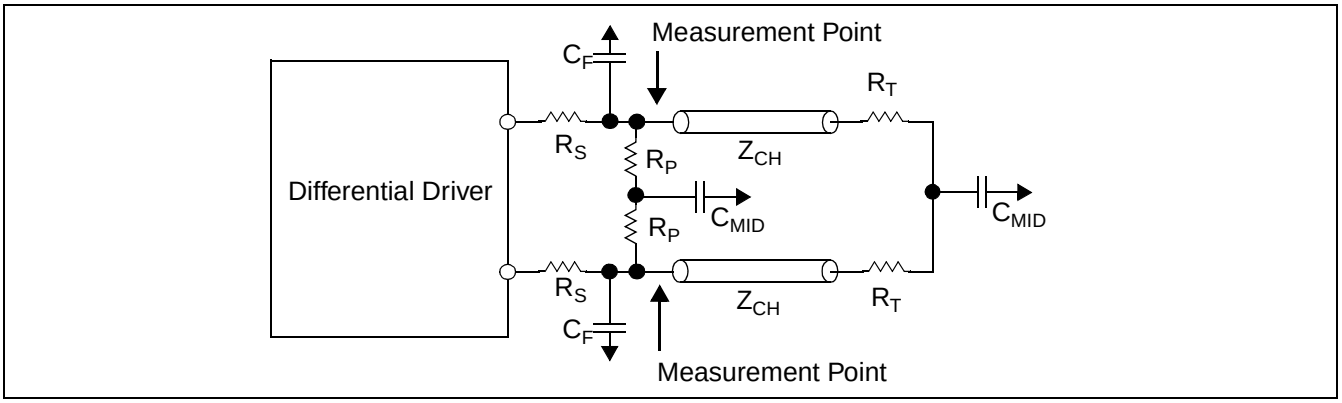

Figure 13: Example System Clock Driver Equivalent Circuit

Figure 13 shows the clock driver equivalent circuit. The differential output clock driver of the DRCG has a low output impedance in the range of about 20 ohms. The driver produces the specified voltage swing on the channel, and also matches the channel impedance. The nominal value of the channel impedance, Z_{CH}, is expected to be 28 ohms for a Rambus memory subsystem. External series resistors RS and parallel resistors RP are used to set the voltage swing on the channel. The driver output characteristics are defined together with the external components, and the output clock is specified at the measurement point indicated in Figure 13. The complete set of external components for the output driver circuit, including edge-rate filter capacitors is also shown in the figure and example values for the external components are shown in Table 18.

The clock driver is specified as a black-box at the package pins. The output characteristics are measured after the series resistance, R_S. The outputs are terminated differentially at the end of the transmission line, with no applied termination voltage.

The clock driver's output impedance, r_{OUT}, is in series with R_S, and the combination is in parallel with R_P. The resulting effective impedance must match the channel impedance in order to minimize secondary reflections. To accomplish this, each of the four CMOS output devices is designed to have an r_{OUT} of about 20 ohms when fully turned on. r_{OUT} is the dynamic output resistance. Since r_{OUT} is in series with R_S, and that combination is in parallel with R_P, the effective output impedance is given by:

$$R_P (R_S + r_{OUT}) / (R_P + R_S + r_{OUT})$$

This calculation results in an effective output impedance of about 27 ohms for the example values listed in Table 18. Since the total impedance is dominated by the external resistors, a large variation in the on-chip value of r_{OUT} is allowed. When the output is transitioning, the impedance of the CMOS devices increases dramatically. The purpose of R_P is to limit the maximum output impedance during output transitions.

In order to control signal attenuation and EMI, clock signal rise / fall times are tightly controlled. External filter capacitors C_F could be used to control the output slew rate. In addition, the capacitor C_{MID} is used to provide AC ground at the mid-point of the R_P and the R_T resistors.

Table 18 gives the nominal values of the external components and their maximum acceptable tolerance, assuming Z_{CH} = 28 ohms for the example Rambus memory subsystem. These values apply only to the DRCG Testboard. For motherboard values, see the System Physical Design Guide..

Table 18. Example External Component Values

Symbol	Parameter	Value	Tolerance	Unit
R_T	Termination resistor	27	± 1%	Ω
R_S	Series resistor	68	± 5%	Ω
R_P	Parallel resistor	39	± 5%	Ω
C_F	Edge-Rate Filter Capacitor	3	± 10%	pF
C_{MID}	AC Ground Capacitor	100	± 20%	pF

Output Driver Characteristics

Table 19 gives example V / I characteristics for the clock output drivers at the pins of the DRCG. The sign on all current parameters (direction of current flow) is referenced to a ground inside the component; i.e. positive currents flow into the component. These example V / I characteristics can be used for generating simulation models of the DRCG (such as IBIS models). Table 19 is given as an example and does not represent additional specifications.

Table 19. Output Buffer V/I Characteristics

Voltage (V)	Pull-Down			Pull-Up		
	I (mA)	I (mA)	I (mA)	I (mA)	I (mA)	I (mA)
	Min	Typ	Max	Min	Typ	Max
0	0	0	0	-35	-55	-91
0.2	8.3	11.9	17.6	-34	-55	-90
0.4	15.8	22.8	33.6	-34	-54	-89
0.6	22.5	32.5	47.9	-33	-53	-87
0.8	28.3	41.0	60.3	-33	-52	-86
1.0	33	48	71	-32	-51	-84
1.2	37	54	79	-31	-50	-82
1.4	41	59	85	-30	-48	-79
1.6	43	62	90	-28	-46	-77
1.8	44	64	92	-27	-43	-73
2.0	45	65	93	-24	-40	-68
2.2	45	66	94	-21	-36	-62
2.4	46	66	95	-17.7	-31.1	-55.0
2.6	46	67	95	-13.6	-25.4	-46.7
2.8	46	67	95	-8.9	-19.0	-37.6
3.0	46	67	96	-3.7	-11.9	-27.4
3.135	46	67	96	0	-6.7	-19.9
3.3		67	96		0	-10.3
3.465			96			0

Signal Waveforms

A physical signal which appears at the pins of a device is deemed valid or invalid depending on its voltage and timing relations with other signals. Input and output voltage waveforms are defined as shown in Figure 14. Both rise and fall times are defined between the 20% and 80% points of the voltage swing, with the swing defined as V_H - V_L. For example, the output voltage swing $V_{COS} = V_{OH} - V_{OL}$

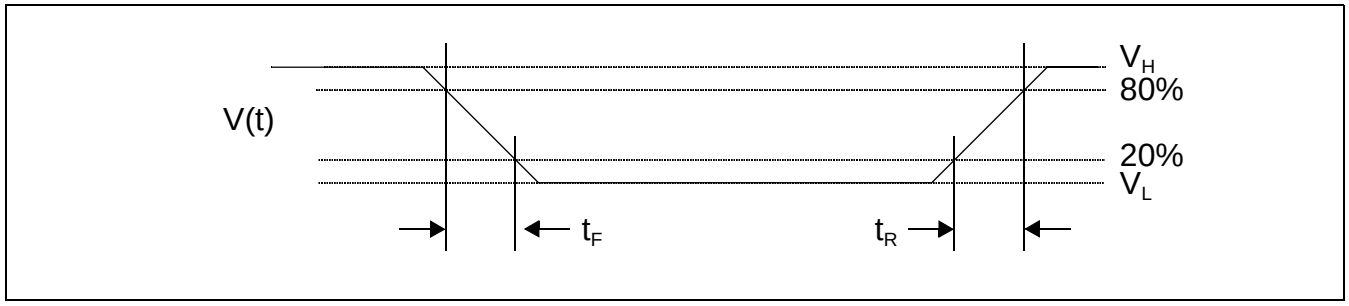

Figure 14: Input and Output Voltage Waveforms

Figure 15 shows the definition of output crossing point. The nominal crossing point between the complementary outputs is defined to be at the 50% point of the DC voltage levels. There are two crossing points defined, Vx+ at the rising edge of CLK and Vx- at the falling edge of CLK. For some clock waveforms, both Vx+ and Vx- might be below Vx,nom (for example, if t_{CR} is larger than t_{CF}).

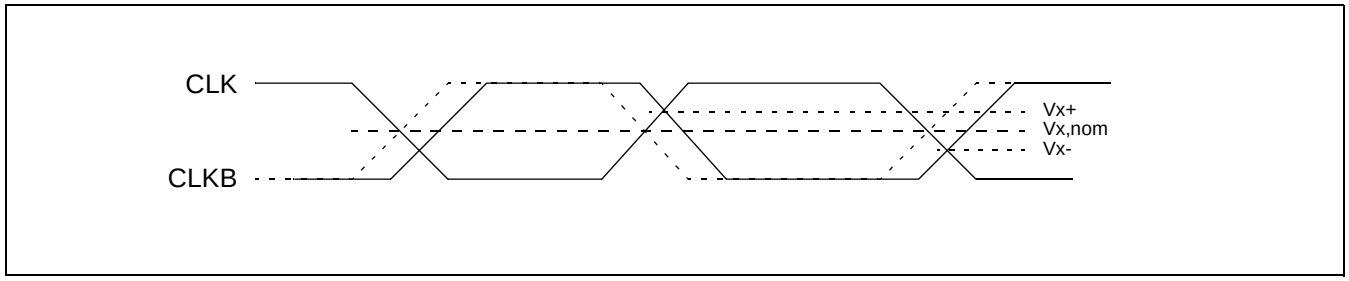

Figure 15: Crossing-point Voltage

Figure 16 shows the definition of long-term duty cycle, which is simply the waveform high-time divided by the cycle time (defined at the crossing point). Long-term duty cycle is the average over many (>10,000) cycles. Short-term duty cycle is defined in the next section.

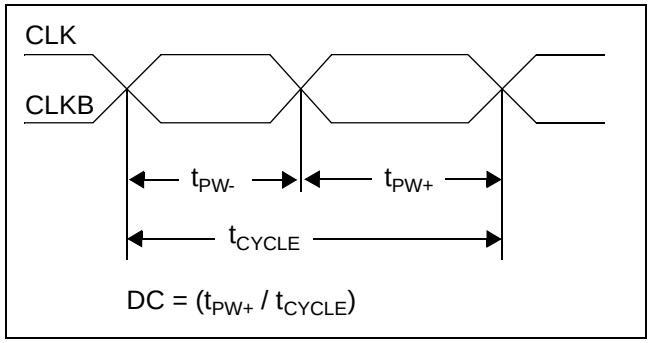

Figure 16: Duty Cycle

Jitter

This section defines the specifications that relate to timing uncertainty (or jitter) of the input and output waveforms. Figure 17 shows the definition of cycle-to-cycle jitter with respect to the falling edge of the CLK signal. Cycle-to-cycle jitter (also called 1-cycle short term jitter) is the difference between cycle times of adjacent cycles. Equal requirements apply for rising edges of the CLK signal.

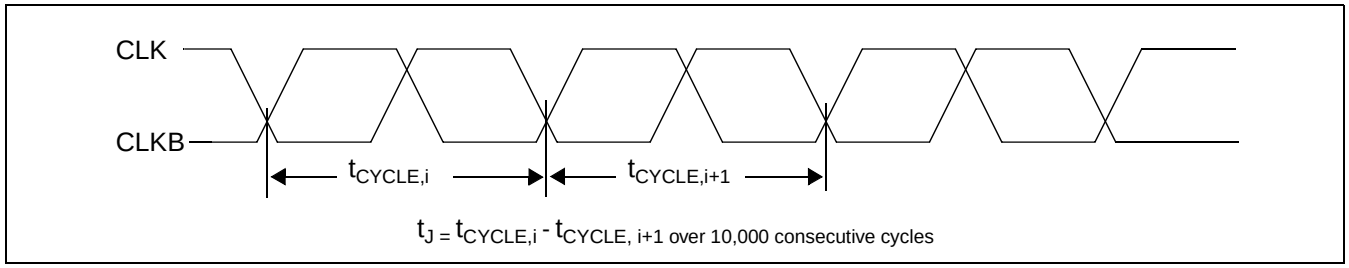

Figure 17: Cycle-to-cycle Jitter

Figure 18 shows the definition of 4-cycle short-term jitter. Short-term jitter is defined with respect to the falling edge of the CLK signal. 4-cycle short-term jitter is the difference between the cumulative cycle times of adjacent 4-cycles. Equal requirements apply for rising edges of the CLK signal. Equal requirements also apply for 2-cycle, 3-cycle, 5-cycle, and 6-cycle short-term jitter.

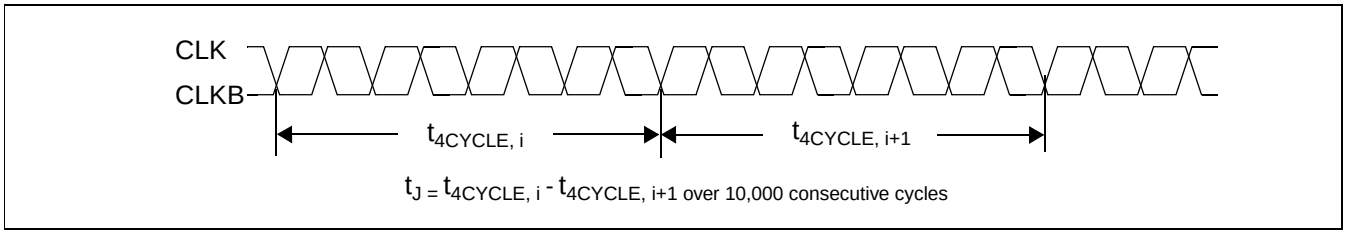

Figure 18: Short-term Jitter

The purpose of this definition of short-term jitter is to define errors in the measured time (for example, $t_{4CYCLE, i}$) vs. the expected time. The purpose for measuring the adjacent time $t_{4CYCLE, i+1}$ is only to help determine the expected time for $t_{4CYCLE, i}$. Alternate methods of determining t_J are possible. However, measuring long-term average jitter instead of short-term jitter would normally give more pessimistic results.

Figure 19 shows the definition of cycle-to-cycle duty cycle error. Cycle-to-cycle duty cycle error is defined as the difference between t_{PW+} (high-times) of adjacent differential clock cycles. Equal requirements apply to t_{PW-} , low-times of the differential clock cycles.

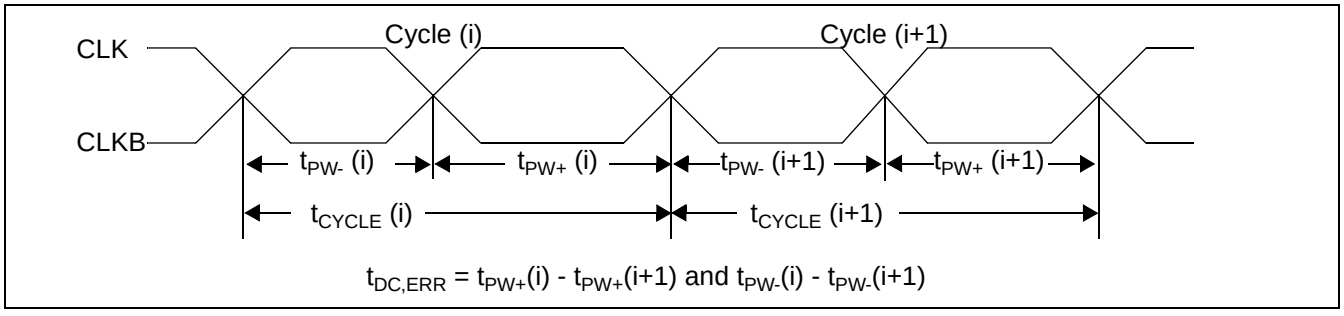

Figure 19: Cycle-to-cycle Duty Cycle Error

Spread Spectrum Clocking

Spread Spectrum Clocking (SSC) can be used to reduce the spectral peaks and help reduce system-level EMI. The DRCG does not contain any functionality to generate SSC. If SSC is used, and the SSC clock input meets operating conditions listed in Table 16, the input clock will be modulated, and the DRCG will track the input modulation. The use of SSC is optional, and the input clocks may or may not be modulated.

The minimum clock period cannot be violated. The preferred method is to adjust the spreading to not allow for modulation above the nominal frequency. This technique is often referred to as "downspreading." An example frequency modulation is shown in Figure 20. The frequency is spread from fNOM down to (1-PM,IN)*fNOM, where fNOM is the inverse of the nominal input cycle time, tCYCLE,IN.

The example in Figure 20 shows triangular frequency modulation. Other types of non-linear modulation are commonly used. The amount of allowed modulation index depends on the type of modulation used. Generally, the amount of non-linear modulation allowed is less than the amount of linear (triangular) modulation allowed. The amount of allowed spreading for any non-triangular modulation is determined by the induced downstream PLL tracking skew, which cannot exceed the amount of skew generated by a triangular modulation of the specified amount.

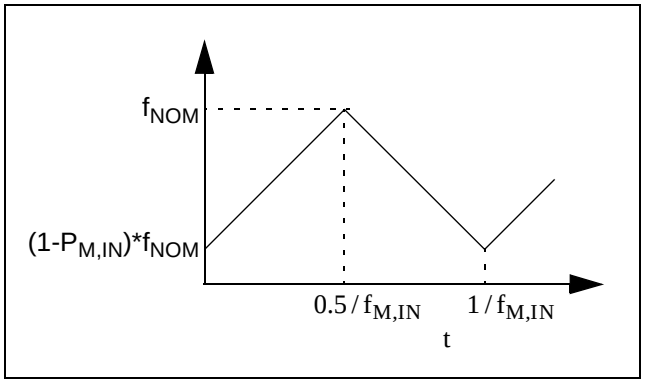

Figure 20: Input Frequency Modulation

Package Drawing

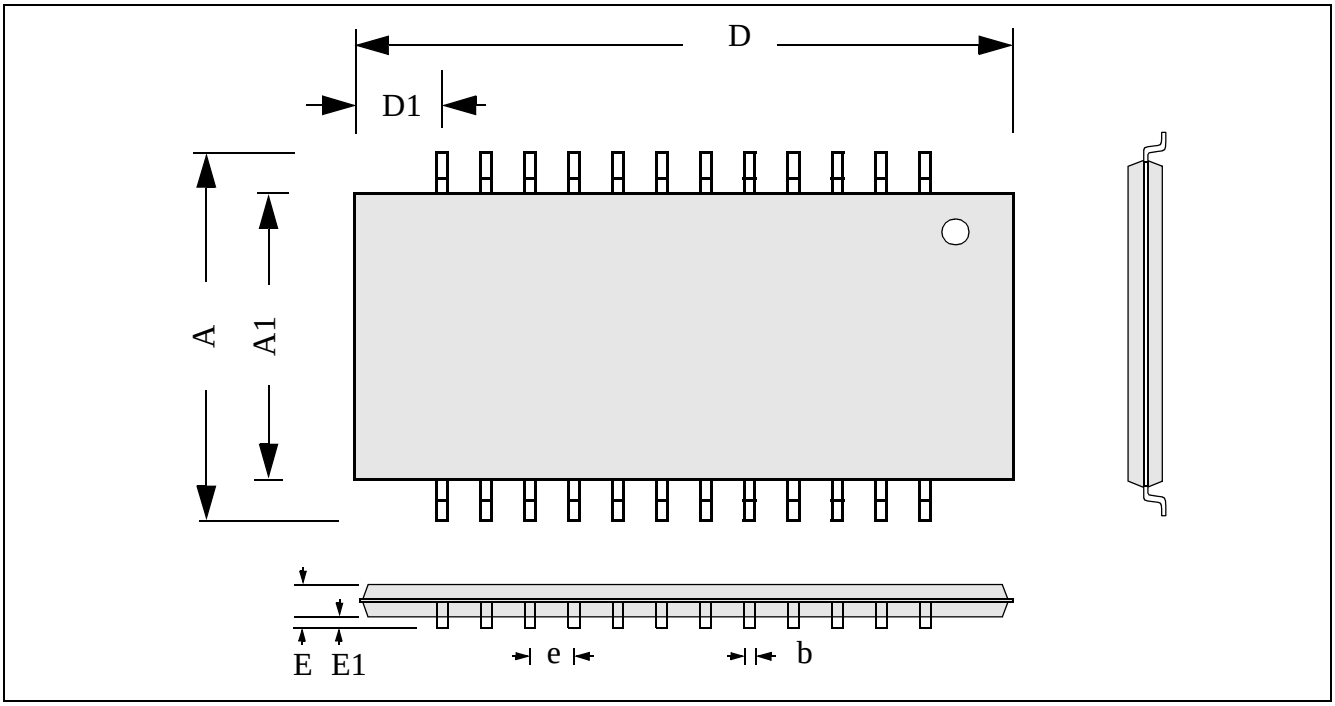

Figure 21: 24-Pin 150mil SSOP Package Drawing

Table 20. Package Dimensions

Symbol	Parameter	Min	Max	Unit
e	Pin Pitch	0.025	0.025	inch
b	Pin width	0.008	0.012	inch
A	Package total length	0.228	0.244	inch
A1	Package body length	0.150	0.157	inch
D	Package total width	0.337	0.344	inch
D1	Package overhang	0.033	0.033	inch
E	Package total thickness	0.053	0.069	inch
E1	Space under package	0.004	0.010	inch

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